Reference Design:

HFRD-22.3

Rev. 4; 03/09

As of March, 2009 this reference design board is no longer available.

Gerber files and schematics are available upon request.

REFERENCE DESIGN

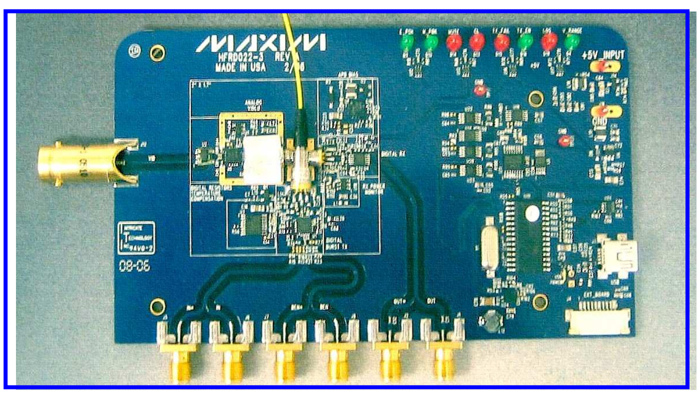
Modular GPON (MOGPON) ONT

maxim integrated™

Table of Contents

Features

- **Excellent Sensitivity, Linearity, Cross-talk Performance and High-Speed Operation**
- **Low-cost design (Bill of Materials and Assembly)**
- **Complete Evaluation Software**
- **Adaptable for Multiple PON Applications / Data Rates including APD applications**
- **Schematics, Bill of Materials, Gerber Files are available**



1 Overview

High Frequency Reference Design (HFRD) 22 is a series of modular GPON (MOGPON) evaluation boards allowing simple evaluation of various configurations and options. They provide a complete reference design to speed and simplify new product development for the entire physical layer design of an ONT / ONU. Schematics, bill of materials, layout files, and typical test data are available by request, however boards are no longer provided. User software is provided that allows configuration, control and monitoring of each HFRD 22 reference design through a windows controlled USB interface.

The HFRD 22.1, 22.2 and 22.3 transceiver reference designs include a burst mode Laser driver, continuous mode APD digital receiver, an analog video amplifier and an optical subassembly including laser, photodiodes and TIA. Each of these designs highlights a different configuration or available option for implementing a GPON ONT. The HFRD 22.7 reference design is a GPON ONT SERDES evaluation board that connects directly to any of the transceiver reference boards mentioned above.

This document details the design and operation of the HFRD 22.3 reference design.

2 Obtaining Additional Information

The GPON ONT transceiver board (HFRD 22.3) is no longer available. For more information about the reference design or to request Gerber files and schematics please email to: https://support.maxim-ic.com/.

3 Reference Design Device Details

HFRD 22.3 was engineered to meet the requirements of GPON ONT / ONU transceiver applications (Figure 1) operating at 1244Mbps burst upstream, 2488Mbps downstream with a 47MHz to 870MHz video overlay. The burst-mode upstream transmitter is implemented using the MAX3643 laser driver and the DS1863 controller. The downstream receiver combines the MAX3747 limiting amplifier, MAX1932 APD bias supply and MAX4007 APD current monitor to produce a high sensitivity 2488Mbps digital receiver. The MAX3654 CATV transimpedance amplifier provides a linear, low noise amplification of the analog video signal. The DS1863 provides laser control, temperature compensation, non-volatile memory, safety features and various monitors. The laser, photodiodes, and TIA are housed in an optical subassembly provided by ExceLight, completing the ONT / ONU transceiver.

3.1 MAX3643 - Laser Driver

The MAX3643 burst-mode laser driver provides bias and modulation current drive for PON burst-mode ONT applications. It is specifically designed for use with a low-cost external controller for the APC (and if desired, AMC) loop. A high-speed differential burst-enable input enables the driver to switch the laser from a dark (output off) condition to full on condition in less than 2ns. When BEN is inactive, typical modulation and bias currents are 5µA each.

Laser modulation current can be set from 10mA to 85mA and bias current can be set from 1mA to 70mA using the MODSET and BIASSET inputs. A sample-and-hold circuit is provided to capture the monitor diode output during short PON bursts, if needed, and the BEN high-speed signal is mirrored on an LVCMOS output to be used by the controller operating the APC/AMC loop.

For additional information see the MAX3643 data sheet available on the web at www.maxim-ic.com.

3.2 MAX3747 - Limiting Amplifier

The MAX3747 multi-rate limiting amplifier functions as a data quantizer for OC-3 through OC-48 synchronous optical network (SONET), Fibre-Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides a constant-level, current-mode logic (CML) output voltage level.

The MAX3747 limiting amplifier features a programmable loss-of-signal detect (LOS) and an optional disable function (DISABLE). Output disable can be used to implement squelch.

For additional information see the MAX3747 data sheet available on the web at www.maxim-ic.com.

3.3 MAX1932 - Digitally Controlled, 0.5% Accurate, Safest APD Bias Supply

The MAX1932 generates a low-noise, high-voltage output to bias avalanche photodiodes (APDs) in optical receivers. Very low output ripple and noise is achieved by a constant-frequency, pulse-width modulated (PWM) boost topology combined with a unique architecture that maintains regulation with an optional RC or LC post filter inside its feedback loop. A precision reference and error amplifier maintain 0.5% output voltage accuracy.

The MAX1932 protects expensive APDs against adverse operating conditions while providing optimal bias. Traditional boost converters measure switch current for protection, whereas the MAX1932 integrates accurate high-side current limiting to protect APDs under avalanche conditions. A current-limit flag allows easy calibration of the APD operating point by indicating the precise point of avalanche breakdown. The MAX1932 control scheme prevents output overshoot and undershoot and provides safe APD operation without data loss.

The output voltage can be accurately set with external resistors, an internal 8-bit DAC, an external DAC, or other voltage source. Output span and offset are independently settable with external resistors. This optimizes the utilization of DAC resolution for applications that may require limited output voltage range, such as 4.5V to 15V, 4.5V to 45V, 20V to 60V, or 40V to 90V

For additional information see the MAX1932 data sheet available on the web at www.maxim-ic.com.

3.4 MAX4007 - High-Accuracy, 76V, High-Side Current Monitors in SOT23

The MAX4007 precision, high-side, high-voltage current monitor is specifically designed for monitoring photodiode current in fiber applications. It offers a connection point for the reference current and a monitor output that produces a current signal proportional to the reference current. The current monitor has six decades of dynamic range and monitors reference currents of 250nA to 2.5mA with better than 5% accuracy. The photodiode current can be monitored from 10nA to 10mA with reduced accuracy.

The MAX4007 accepts a supply voltage of +2.7V to +76V, suitable for APD or PIN photodiode applications. Internal current limiting (20mA, typ) protects the devices against short circuit to ground. A clamp diode protects the monitor output from over-voltage. Additionally, these devices feature thermal shutdown if the die temperature reaches +150°C.

The MAX4007 are available in tiny, space-saving 6-pin SOT23 packages, and operate over the extended temperature range of -40°C to +85°C. For additional information see the MAX4008 data sheet available on the web at www.maxim-ic.com.

3.5 MAX3654 - 47MHz to 870MHz Analog CATV Transimpedance Amplifier

The MAX3654 analog transimpedance amplifier (TIA) is designed for CATV applications in fiber-to-the-home (FTTH) networks. This high-linearity amplifier is intended for 47MHz to 870MHz subcarrier multiplexed (SCM) signals in passive optical networks (PON). A gain-control input supports AGC operation with optical inputs having -6dBm to +2dBm average power. With 62dBΩ maximum gain at 47MHz and 18dB gain control range, the minimum worst case RF output level is 14dBmV/channel at -6dBm optical input. A compact 4mm x 4mm package includes all of the active RF circuitry required to convert analog PIN photocurrent to a 75Ω CATV output.

For additional information see the MAX3654 data sheet available on the web at www.maxim-ic.com.

3.6 DS1863 – Laser Bias APC and Temperature Controlled Modulation DAC with Internally Calibrated Monitors

The DS1863 is a burst-mode controller and monitor that is ideal for PON transceiver designs. It controls laser driver bias and modulation currents via integrated Average Power Control (APC) circuitry and a temperature-controlled current-sink DAC for extinction ratio control, respectively.

Systems diagnostics are provided by monitoring three analog inputs, VCC, and temperature (using an internal temperature sensor). An intelligent maskable fault control system allows any sensed alarm condition to shutdown the laser. Two fault outputs are provided; one functions to shutdown the laser for critical faults and the other can be used as an interrupt to request system attention.

Eye-safety features are integrated via four fast trip comparators that monitor transmit power high, transmit power low, bias current low and bias current high. The fast trip comparators drive a FET driver output to disable the laser in the case of an eye safety violation.

The device also contains 248 bytes of general purpose EEPROM with two-level password protection. Access to the device is provided over an I^2C interface.

With its integrated laser driver control, system diagnostics, eye-safety features, and internal temperature sensor, the DS1863 provides an ideal solution for PON optical transceiver modules by improving system performance, reducing board space, and simplifying design.

For additional information see the DS1863 data sheet available on the web at www.maxim-ic.com.

3.7 ExceLight SXT5241-Q/GP1 Bi-Directional Optical Subassembly

The SXT5241-Q/GPI GPON bi-directional optical subassembly is designed for ONU/ONT applications that operate at gigabit data rates and includes a linear photodiode for video overlay. The triplexer uses a high-speed 1310nm DFB laser source for the 1244Mbps upstream data transmission, an APD and preamplifier to receive the 1490nm downstream digital data at 2488Mbps, and an analog PIN photodiode to receive the 1550 nm downstream video signal. Note: the ExceLight SXT5241 is no longer in production.

For more information regarding the assembly, please call ExceLight at: 919-361-1600, email information@excelight.com or visit their web page (http://www.excelight.com).

4 Functional Diagram

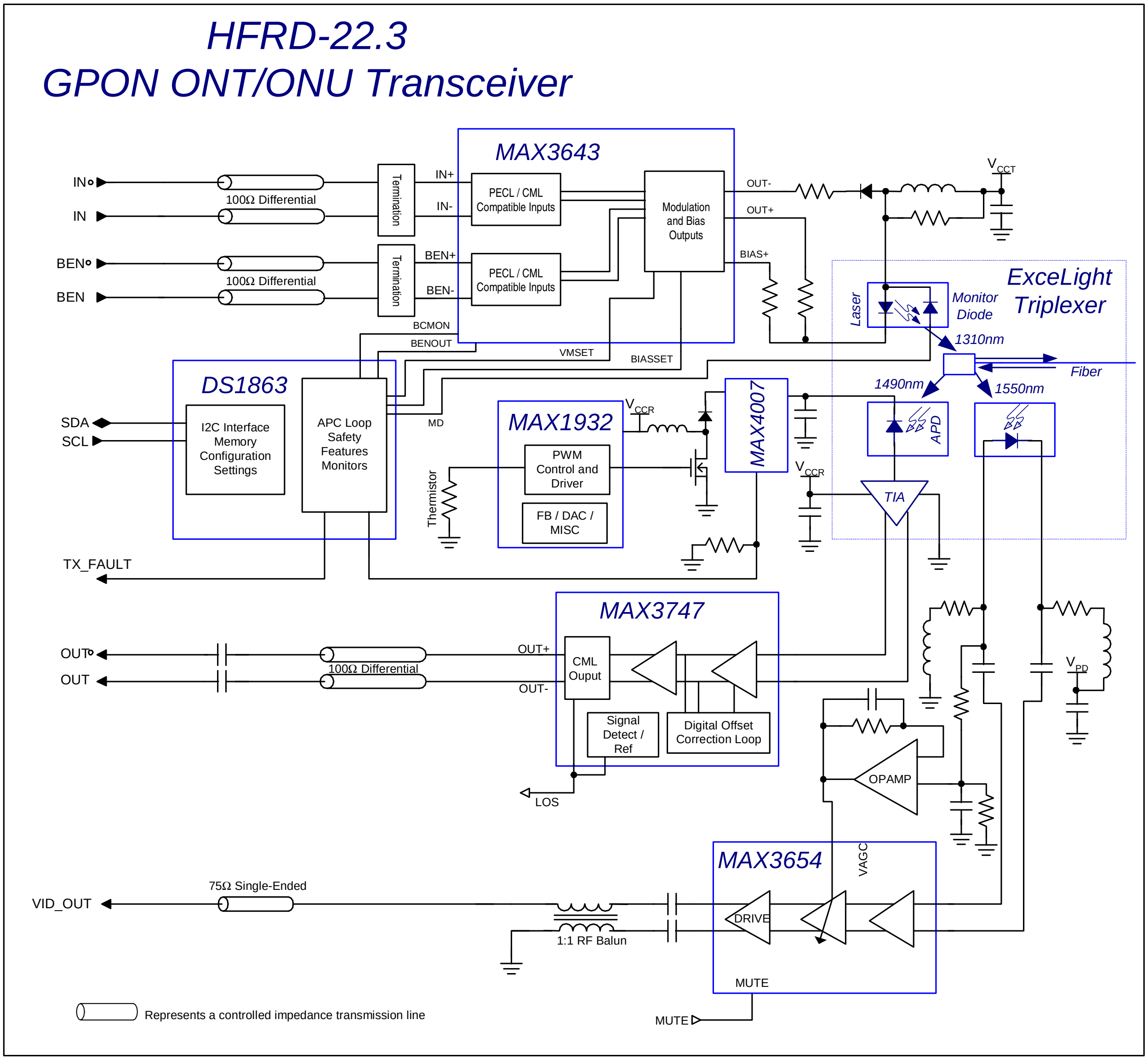


Figure 1: HFRD 22.3 Functional Diagram

5 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature	T_A		-40		+85	^oC
Supply Voltage	V_{CC}	Note 1	4.75	5.0	5.25	V
Transmitter Data Rate				1244		Mbps
Digital Receiver Data Rate				2488		Mbps
Analog Receiver Input Power			-6		+2	dBm
Digital Receiver Input Power		T_A = -20^{o}C to +85^{o}C			-8	dBm
Input DC Bias Voltage		VCC = +3.3V, IN +/-		2.0		V
		VCC = +3.3V, BEN +/-		1.3		
Differential Input Voltage	V_{ID}	IN+/-, BEN+/-	200		1600	mV_{p-p}
Burst On-Time		Note 2	420			ns
Burst Off-Time		155Mbps	96			ns

Note 1: The reference design includes a software adjustable low-drop out regulator for the +3.3V supply needed for the digital transmitter and digital receiver sections. The reference design also includes an adjustable (5V to 15V) DC to DC converter for generating the analog photodiode bias supply voltage and an adjustable APD bias voltage supply (20V to 45V). A third adjustable DC to DC converter is also provided to supply power (up to 1000mA) to an external board if connected.
Note 2: Specification is for consecutive repeating bursts at the given length. Shorter bursts are acceptable but the APC loop will not update for bursts shorter than the value specified.

6 Typical Design Performance Data

6.1 Transmitter Performance Data

(Typical values are measured at: Power Level = 100%, T_A = +25^{o}C, V_{CC} = +3.3V, Average Power = 1dBm)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current		Transmitter Only	74	mA
Average Optical Power	P_{AVG}	Measured @ 1244Mbps (Note 1)	+1	dBm
Extinction Ratio (Note 1)	E_R	Set at +25^{o}C	11	dB
Mask Margin		-40^{o}C to +85^{o}C, 1244Mbps	> 40	%
Burst-Enable Time		Note 3	<4	ns
Burst-Disable Time		Note 4	<3	ns
Center Wavelength			1310	nm

Note 1: Measured using a continuous 2^{23}-1 PRBS input data pattern.
Note 3: Time to reach 90% of steady state value after burst enable is asserted.
Note 4: Time to fall below 10% of steady state value after burst enable is de-asserted.

6.2 Digital Receiver Performance Data

(Typical values are measured at T_A = +25°C, V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current		Digital Receiver Only (TIA, MAX3747, MAX1932, MAX4008)	80	mA
Average Optical Input Power Overload	P_{AVGMAX}	T_A = -20°C to +85°C	-8	dBm
Sensitivity (Notes 1)	P_{AVGMIN}	Data Rate = 2488Mbps	-31	dBm
Loss of Signal (Note 2)	LOS	Assert	-32	dBm
		De-Assert	-30	
Loss of Signal Hysteresis			2	dB
Receiver Wavelength			1490	nm

Note 1: Sensitivity is measured using a 2^{23}-1 PRBS test pattern to a BER of approximately 1E-10.
Note 2: Loss of Signal (LOS) is measured using at 2488Mbps with a 2^7-1 PRBS test pattern.

6.3 Analog Receiver Performance Data

(Typical values are measured at T_A = +25°C, V_{CC} = +3.3V)

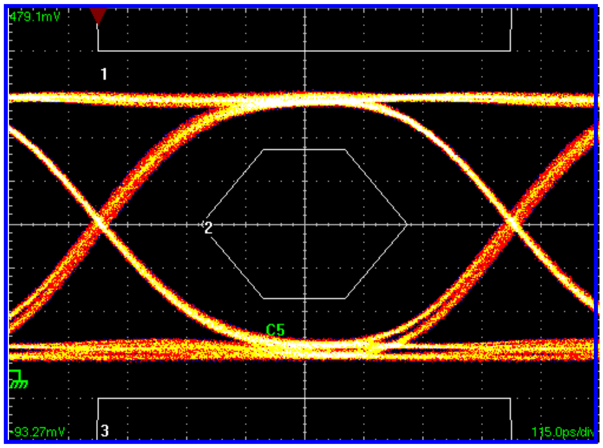
PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current		Analog Receiver Only	136	mA
Input Referred Noise	I_N	Photodiode and Amplifier	6.1	pA/√Hz
Gain Tilt		47MHz to 870MHz	3.75	dB
		47MHz to 1000MHz	4.25	
Gain Flatness (Note 1)		47 to 870MHz	-0.47 / +0.02	dB
		47 to 1000MHz	-0.47 / +0.03	

Note 1: Maximum Deviation from a Straight Line connecting the minimum and maximum frequency.

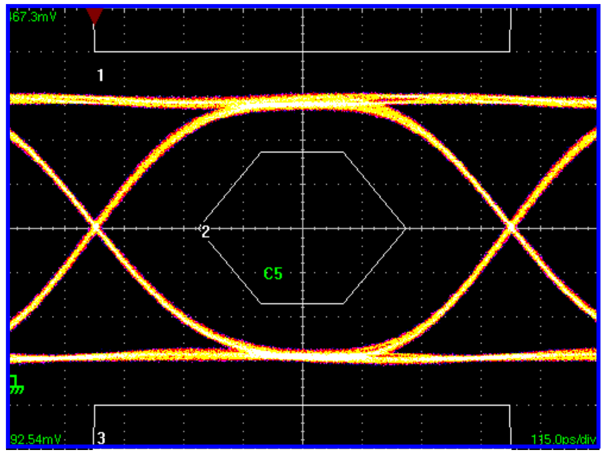
7 Transmitter Characteristic Graphs

(T_A = +25°C, V_{CC} = +3.3V, Data Rate = 1244Mbps, Power Level = 100%, $E_R \approx$ 11dB and P_{AVG} = +0.5 to +2.0dBm unless otherwise noted)

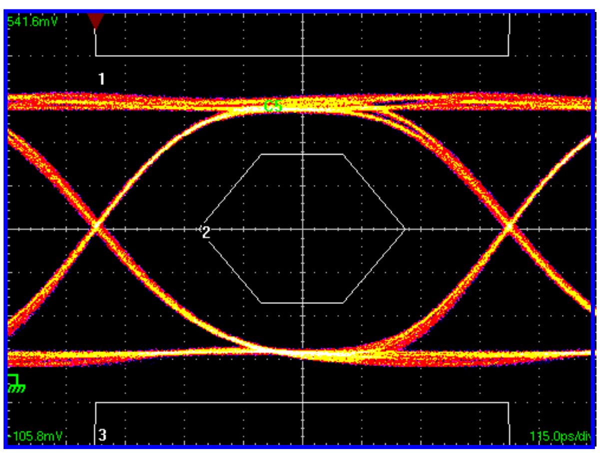
OPTICAL EYE DIAGRAM
(T_A = -40°C)



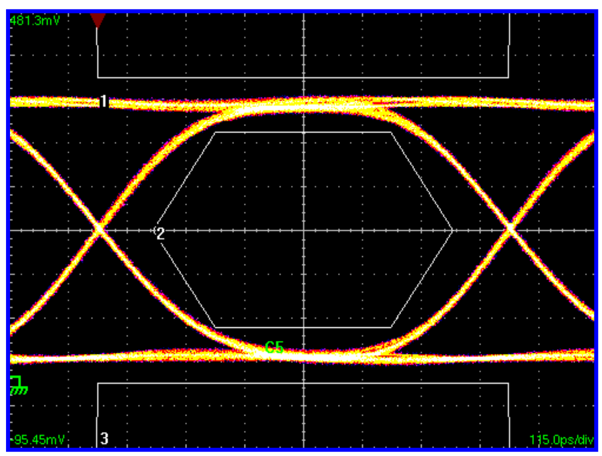
OPTICAL EYE DIAGRAM
(T_A = +20°C)



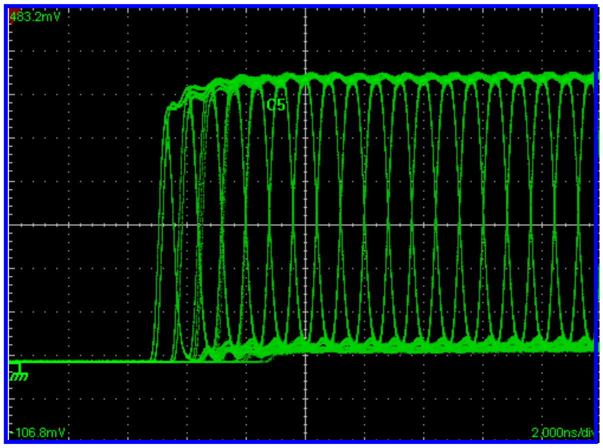
OPTICAL EYE DIAGRAM
(T_A = +85°C)



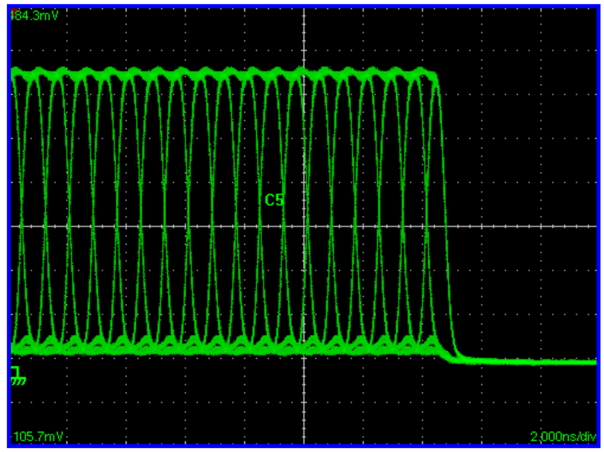
OPTICAL EYE DIAGRAM
(T_A = +25°C, 46% Mask Margin)



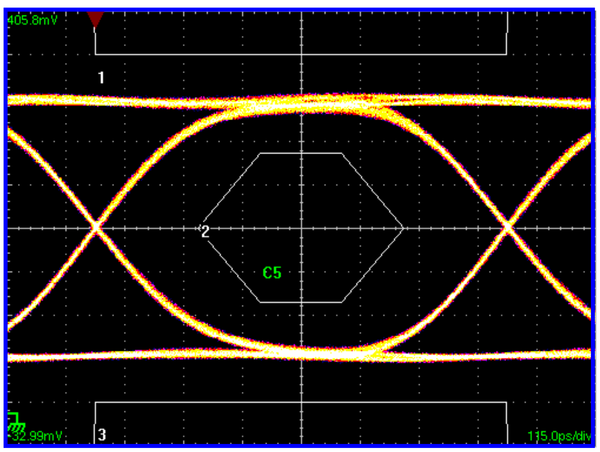
OPTICAL BURST ON DIAGRAM
(2ns/div)



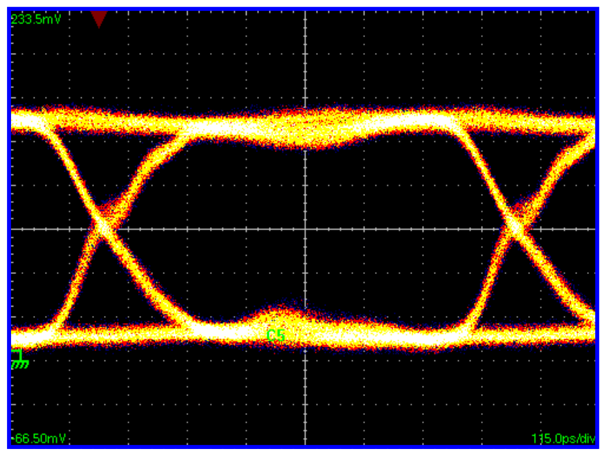
OPTICAL BURST OFF DIAGRAM
(2ns/div)



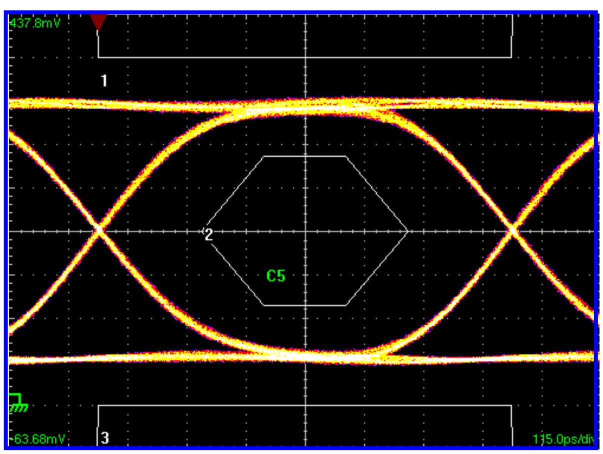
OPTICAL EYE DIAGRAM
(Filtered, Extinction Ratio = 7.1dB)



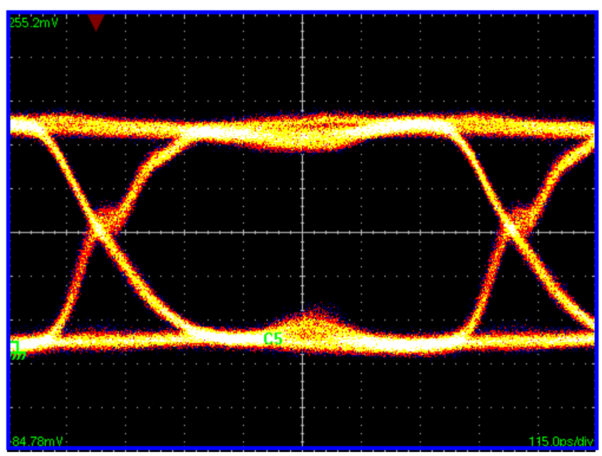
OPTICAL EYE DIAGRAM
(UnFiltered, Extinction Ratio = 7.1dB)



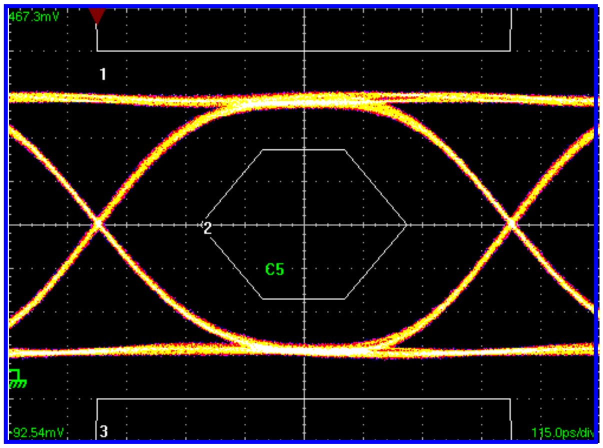
OPTICAL EYE DIAGRAM
(Filtered, Extinction Ratio = 8.9dB)



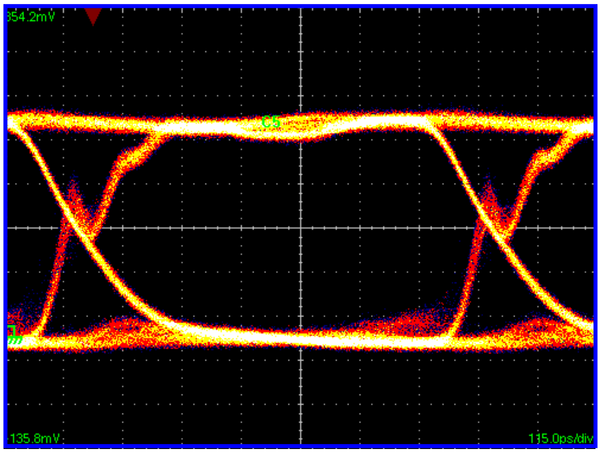
OPTICAL EYE DIAGRAM
(UnFiltered, Extinction Ratio = 8.9dB)



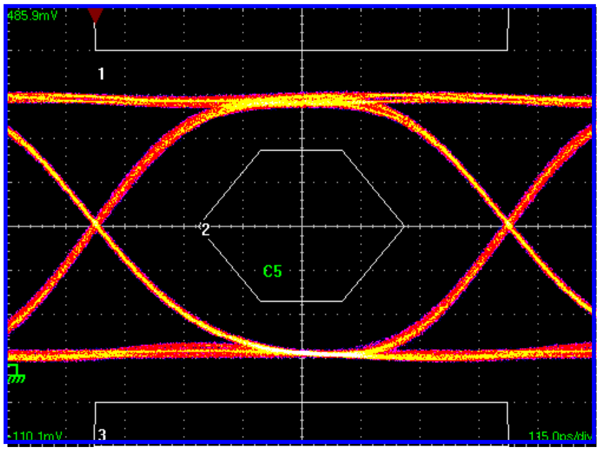
OPTICAL EYE DIAGRAM
(Filtered, Extinction Ratio = 11.2dB)



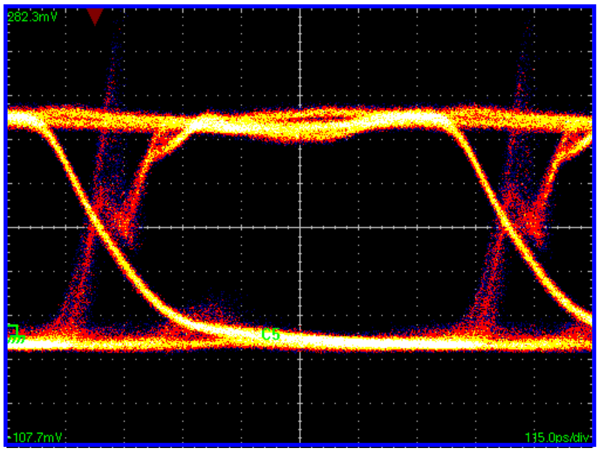
OPTICAL EYE DIAGRAM
(UnFiltered, Extinction Ratio = 11.2dB)



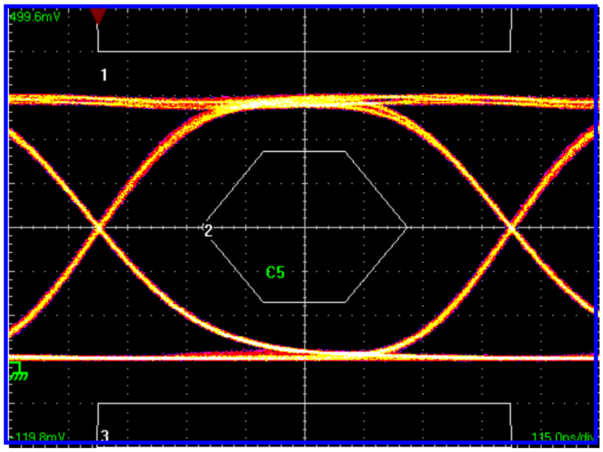
OPTICAL EYE DIAGRAM
(Filtered, Extinction Ratio = 13.3dB)



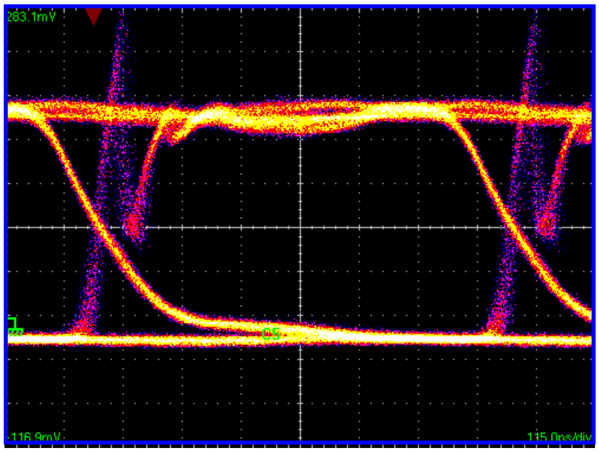
OPTICAL EYE DIAGRAM
(UnFiltered, Extinction Ratio = 13.3dB)



OPTICAL EYE DIAGRAM
(Filtered, Extinction Ratio = 14.9dB)



OPTICAL EYE DIAGRAM
(UnFiltered, Extinction Ratio = 14.9dB)



OPTICAL EYE DIAGRAM
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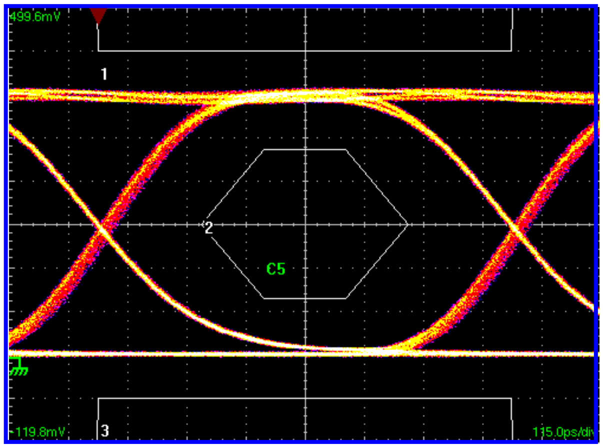
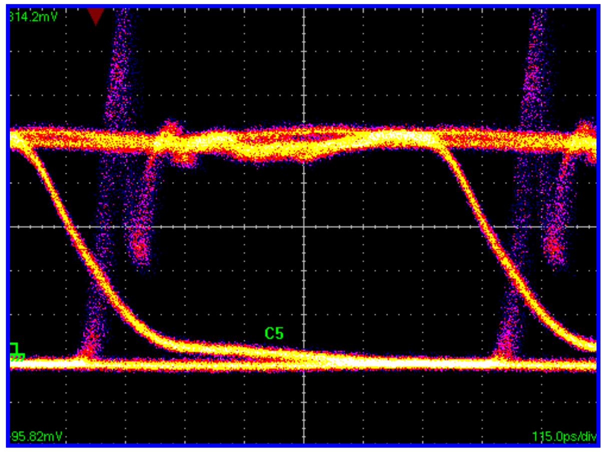
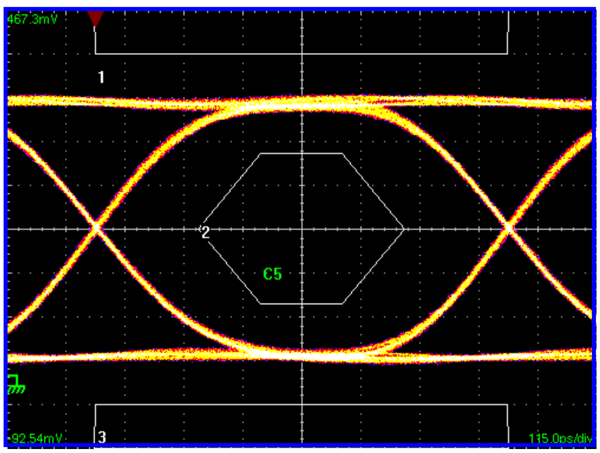


OPTICAL EYE DIAGRAM
(UnFiltered, Extinction Ratio = 15.7dB)



OPTICAL EYE DIAGRAM
(Filtered, Power Level = 100%)



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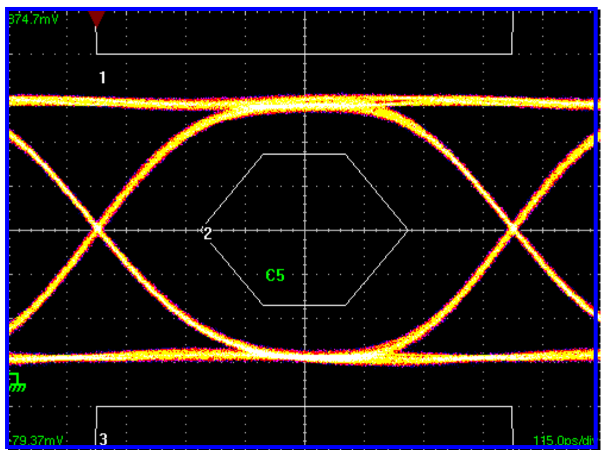
(Filtered, Power Level = 80%)



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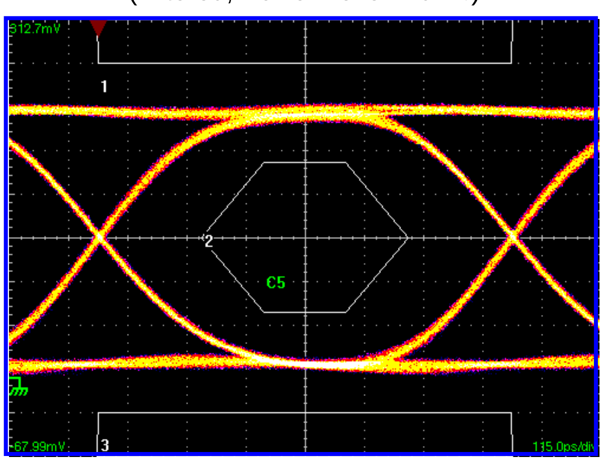
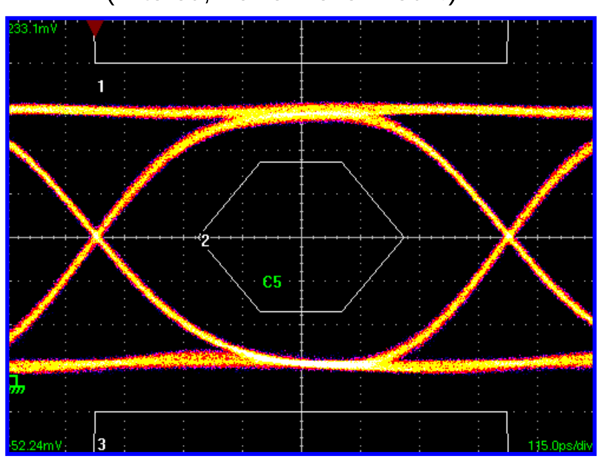
(Filtered, Power Level = 67%)



OPTICAL EYE DIAGRAM
(Filtered, Power Level = 50%)



OPTICAL EYE DIAGRAM
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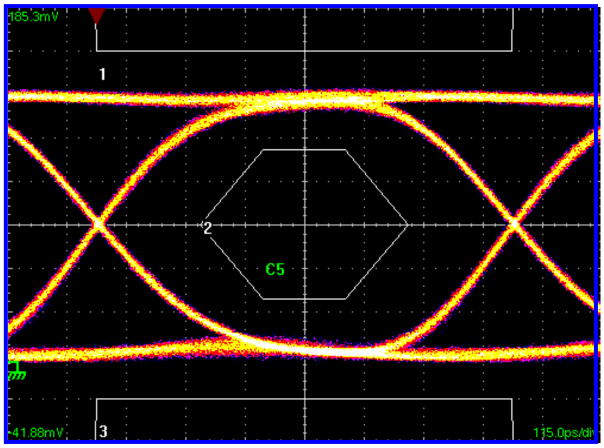

OPTICAL EYE DIAGRAM
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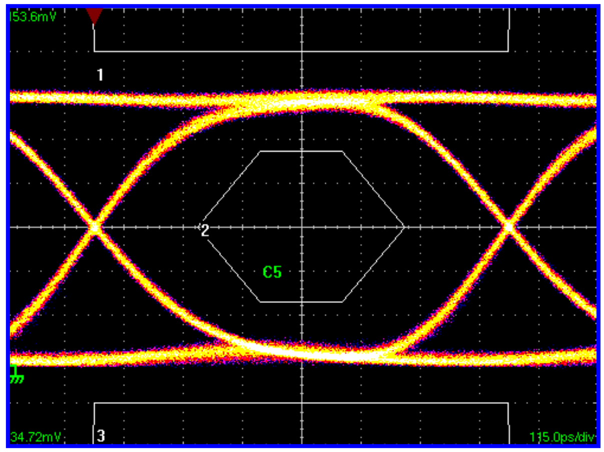
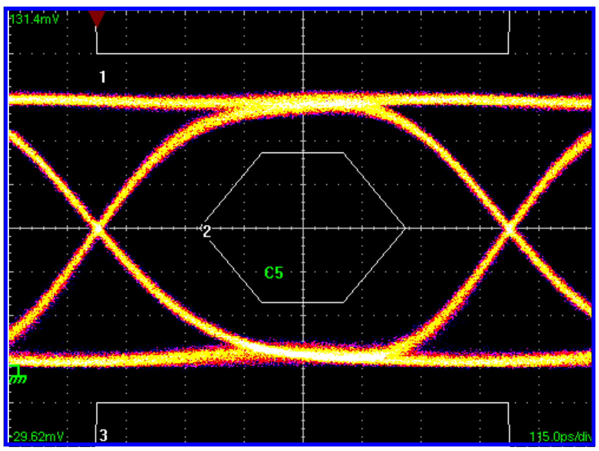


OPTICAL EYE DIAGRAM
(Filtered, Power Level = 28.6%)



OPTICAL EYE DIAGRAM
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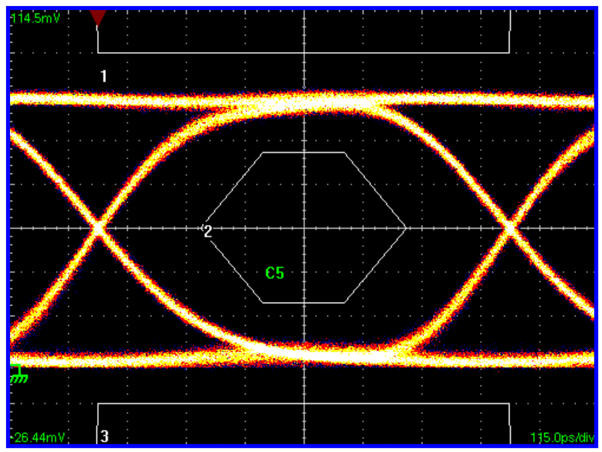
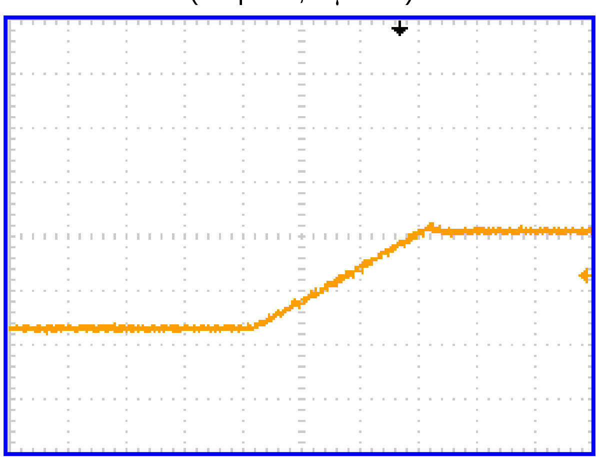


BIAS STARTUP (FROM ENABLE)
(Step = 2, 5 µs/div)



BIAS STARTUP (FROM ENABLE)
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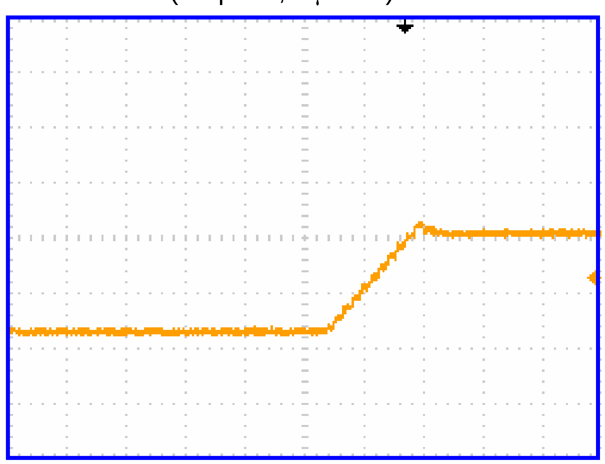
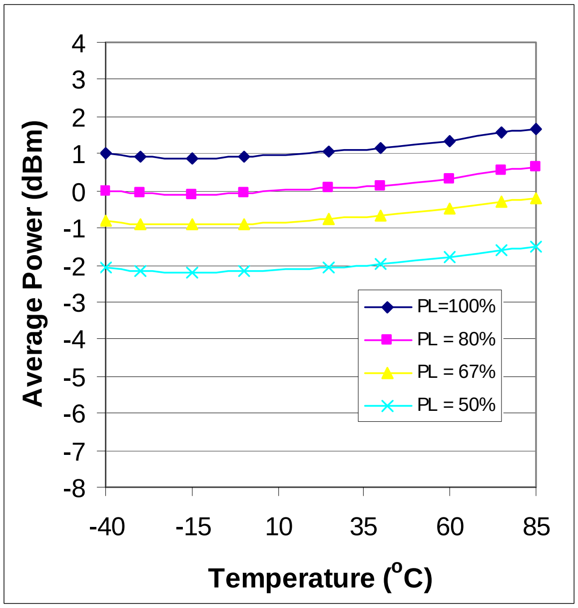
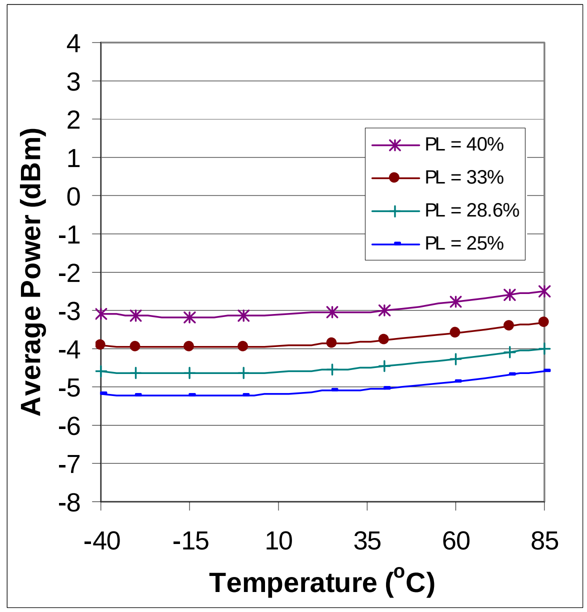


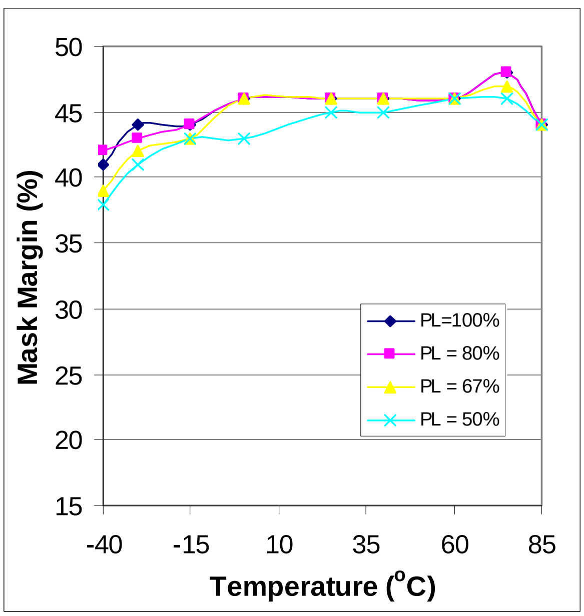
AVERAGE POWER vs. TEMPERATURE



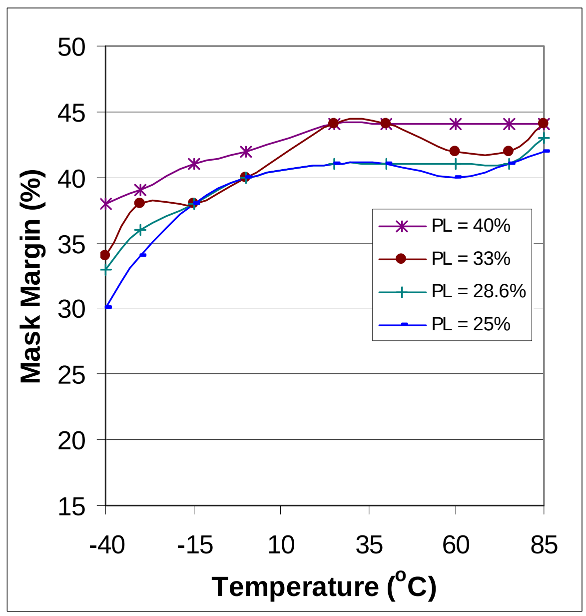
AVERAGE POWER vs. TEMPERATURE



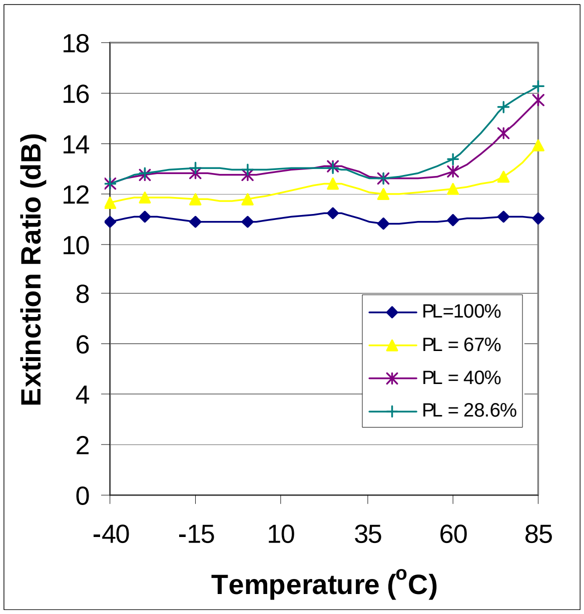
MASK MARGIN vs. TEMPERATURE



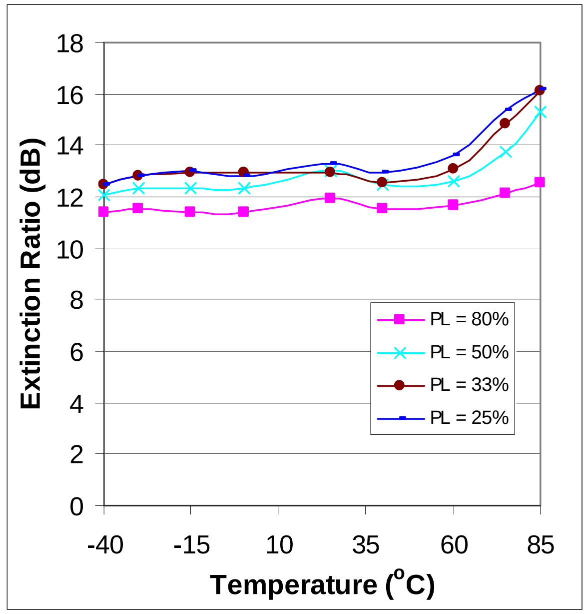
MASK MARGIN vs. TEMPERATURE



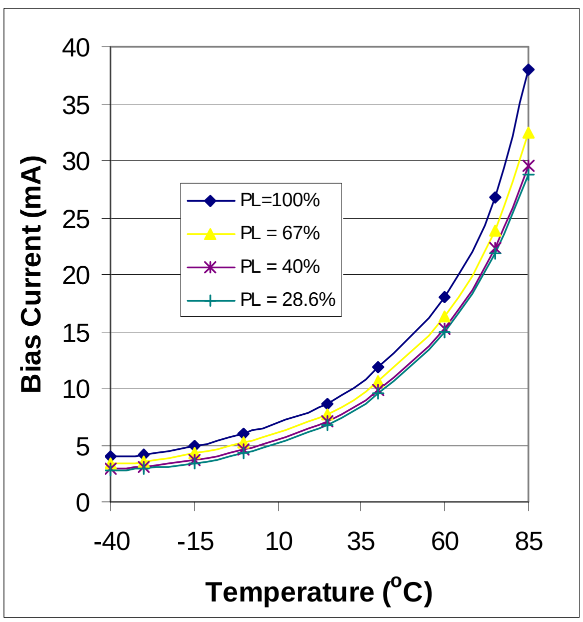
EXTINCTION RATIO vs. TEMPERATURE



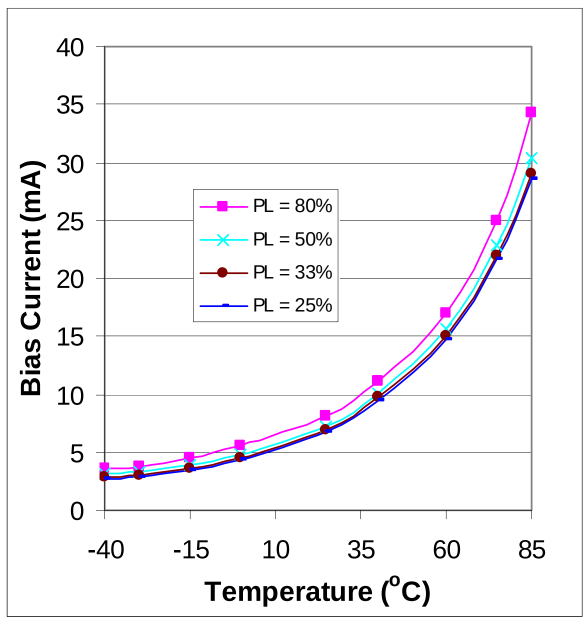
EXTINCTION RATIO vs. TEMPERATURE



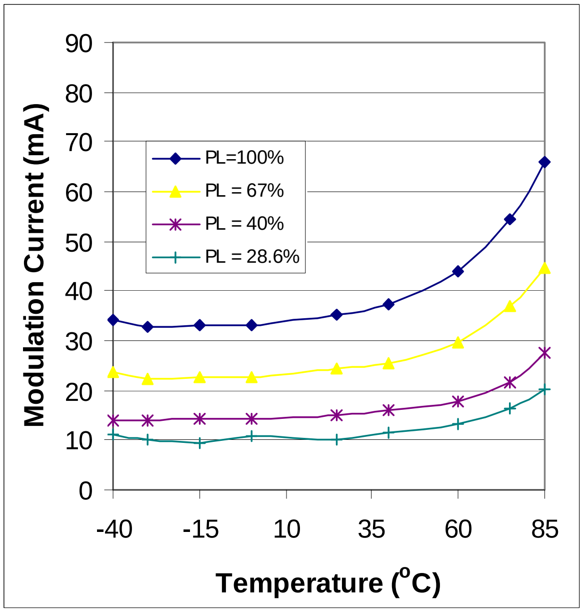
BIAS CURRENT vs. TEMPERATURE



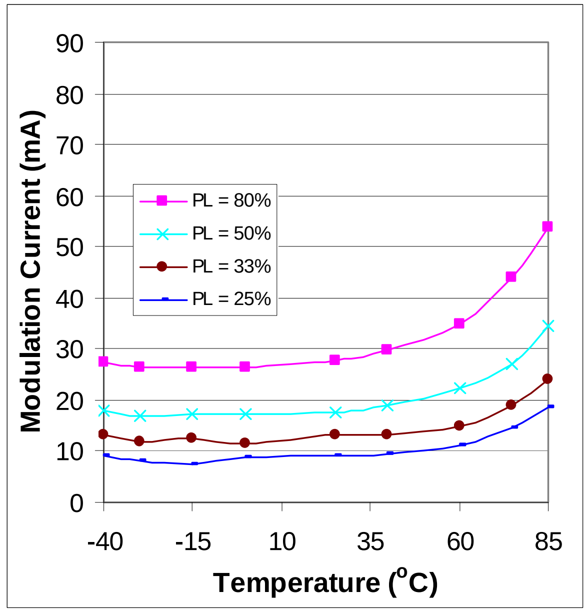
BIAS CURRENT vs. TEMPERATURE



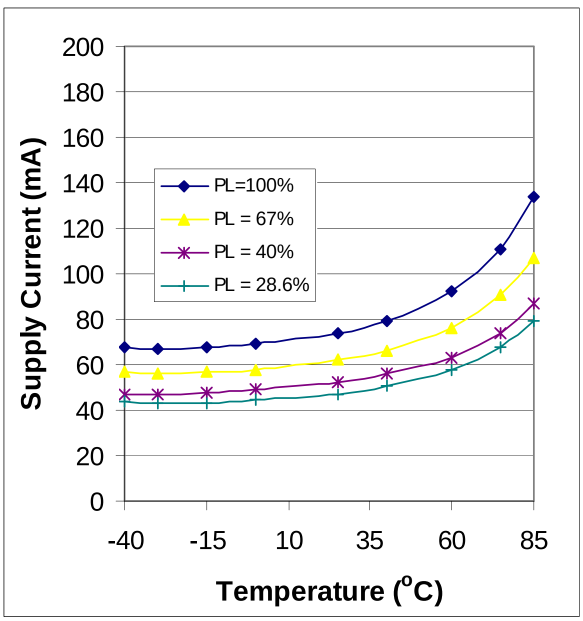
MODULATION CURRENT vs. TEMPERATURE



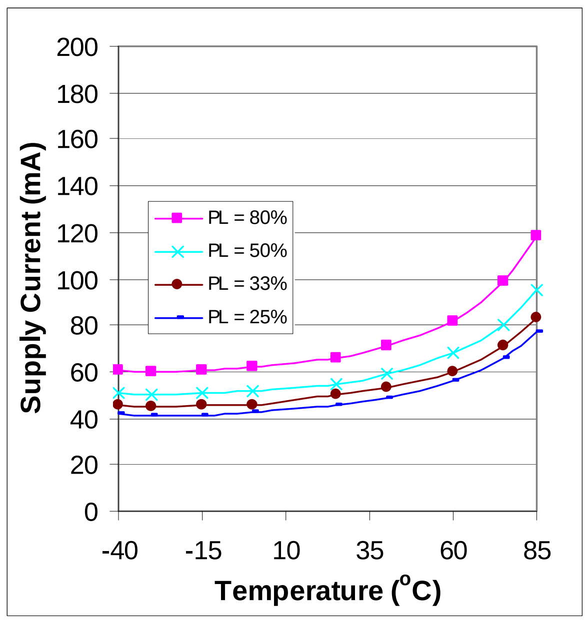
MODULATION CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE
(Includes Bias and Modulation Current)



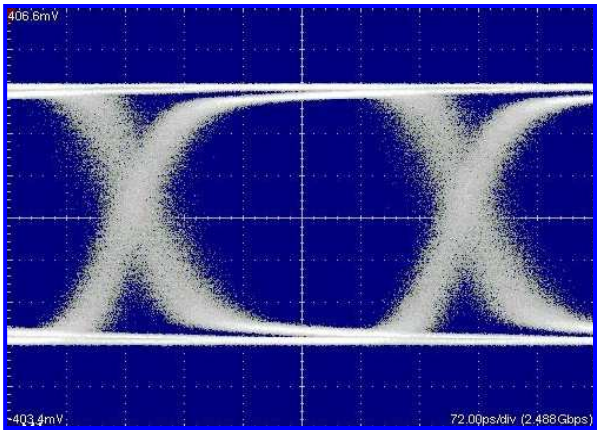
SUPPLY CURRENT vs. TEMPERATURE
(Includes Bias and Modulation Current)



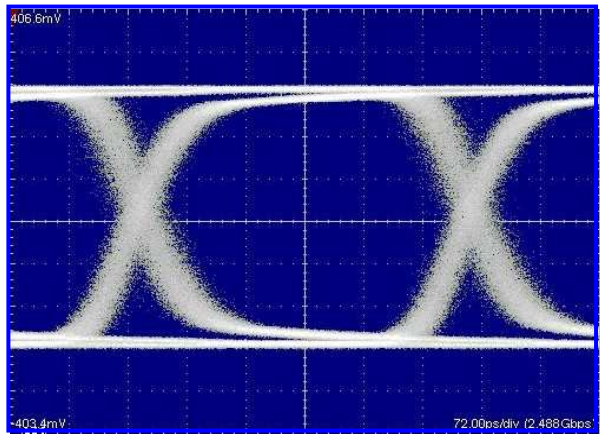
8 Digital Receiver Characteristic Graphs

(T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

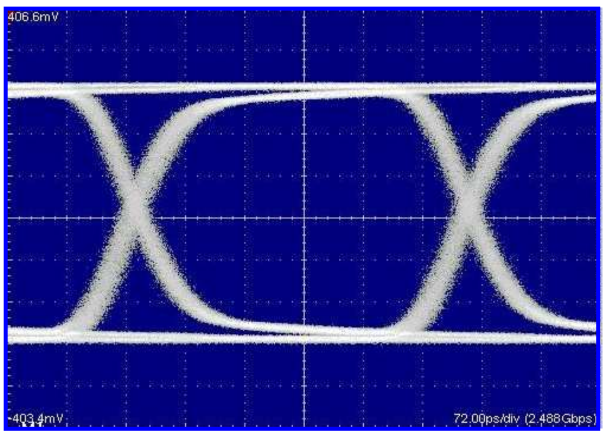
DATA OUTPUT DIAGRAM
(2488Mbps, -31dBm Input)



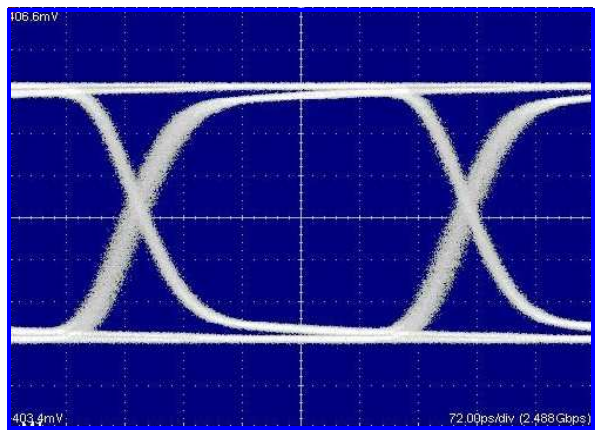
DATA OUTPUT DIAGRAM
(2488Mbps, -28dBm Input)



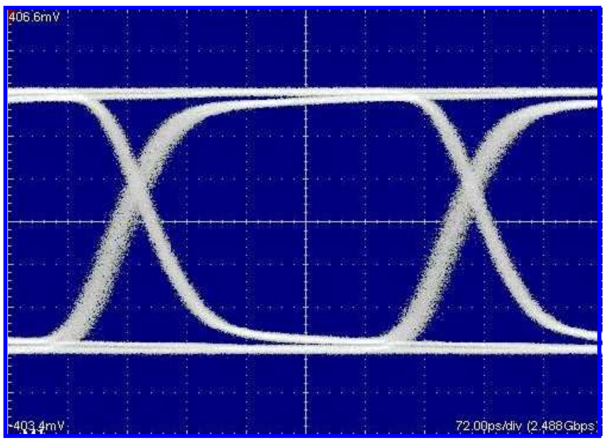
DATA OUTPUT DIAGRAM
(2488Mbps, -22dBm Input)



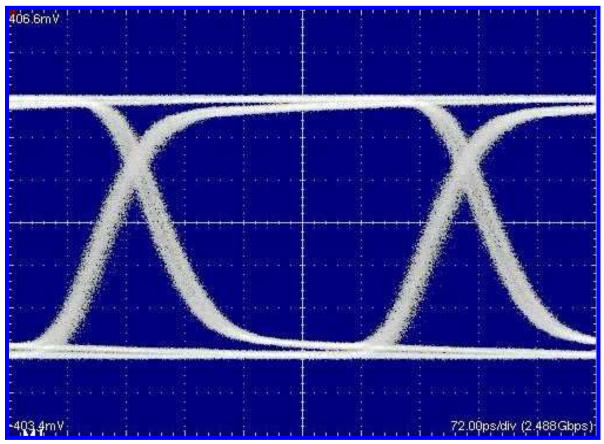
DATA OUTPUT DIAGRAM
(2488Mbps, -16dBm Input)



DATA OUTPUT DIAGRAM
(2488Mbps, -10dBm Input)



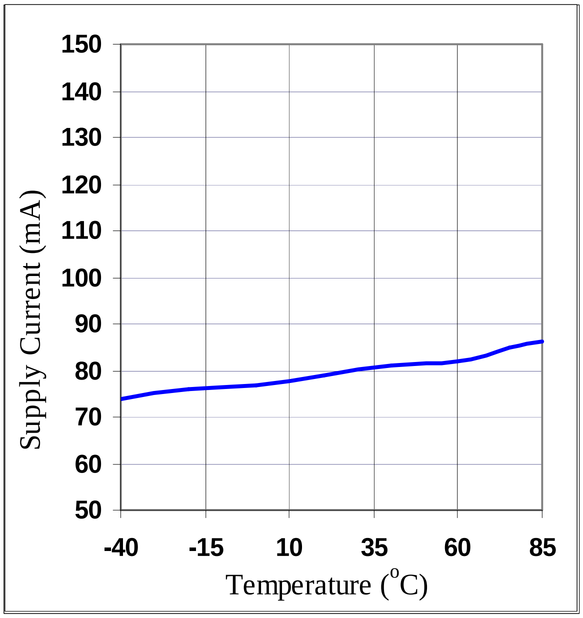
DATA OUTPUT DIAGRAM
(2488Mbps, -8dBm Input)



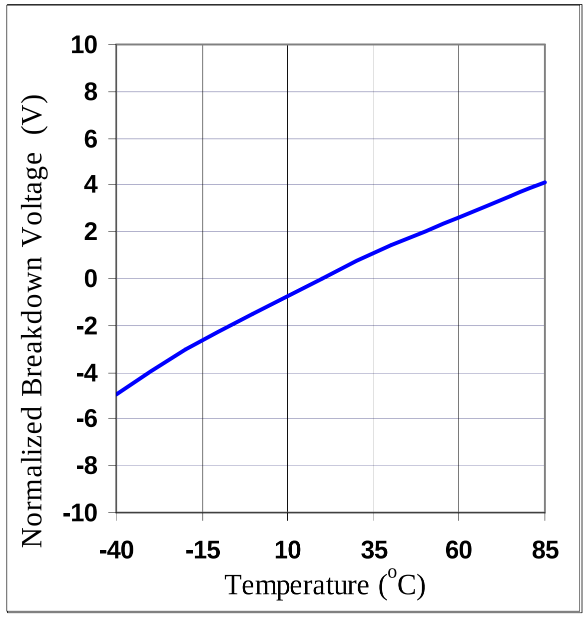
Digital Receiver Characteristic Graphs (Continued)

(T_A = +25°C, V_{CC} = +3.3V, Using Only Thermistor Controlled Compensation, unless otherwise noted.)

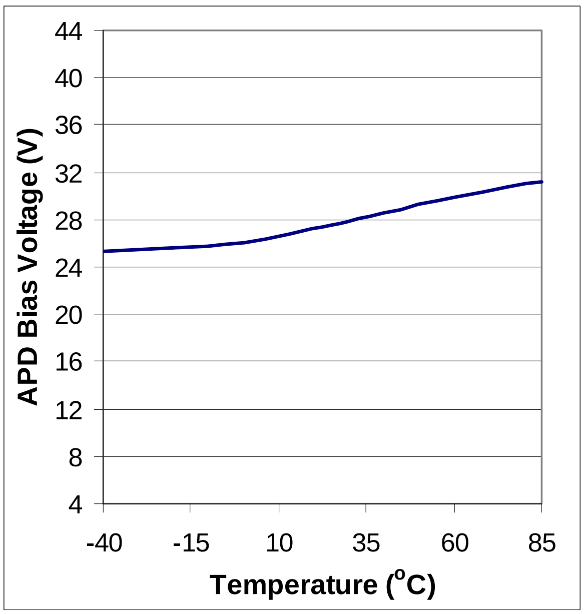
SUPPLY CURRENT vs. TEMPERATURE



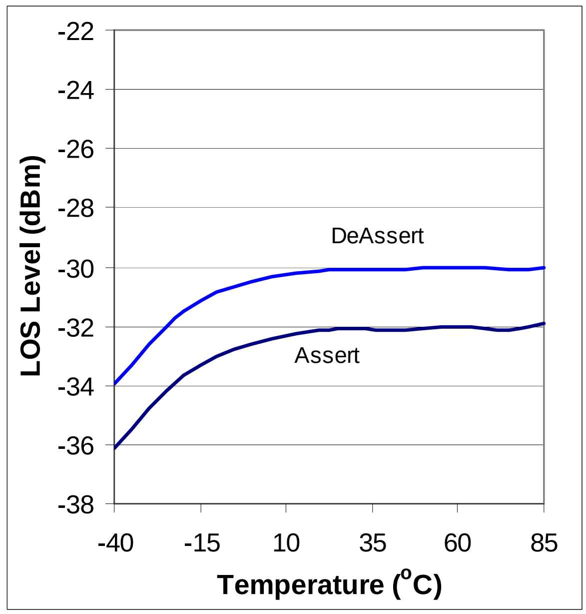
BREAKDOWN VOLTAGE vs. TEMPERATURE



APD BIAS VOLTAGE vs. TEMPERATURE



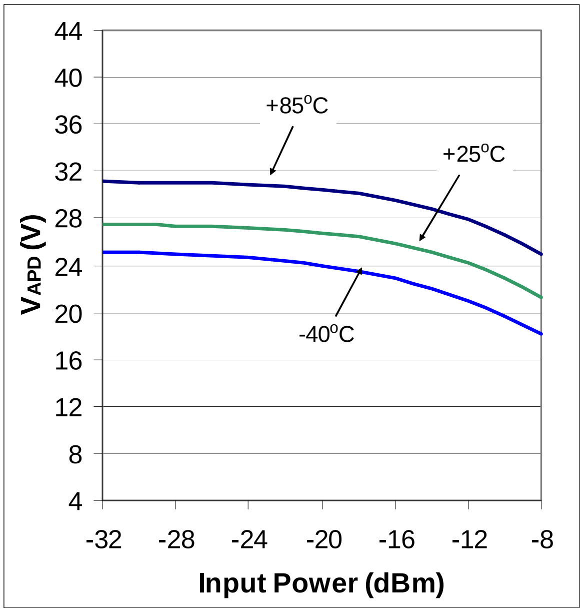
LOS LEVEL vs. TEMPERATURE



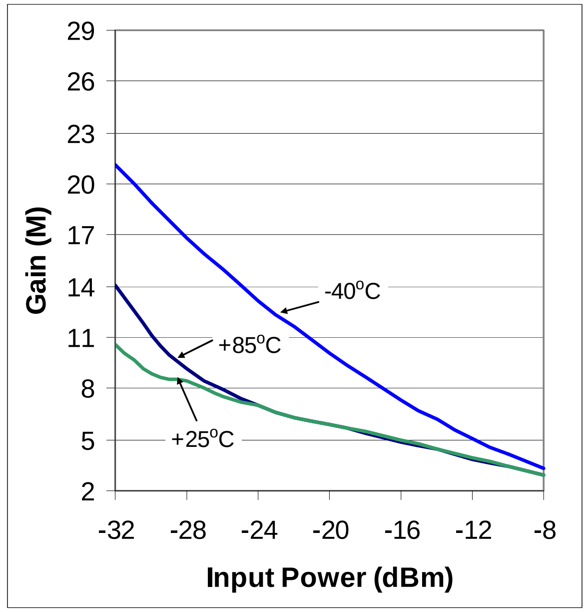
Digital Receiver Characteristic Graphs (Continued)

(T_A = +25°C, V_{CC} = +3.3V, Using Only Thermistor Controlled Compensation, unless otherwise noted.)

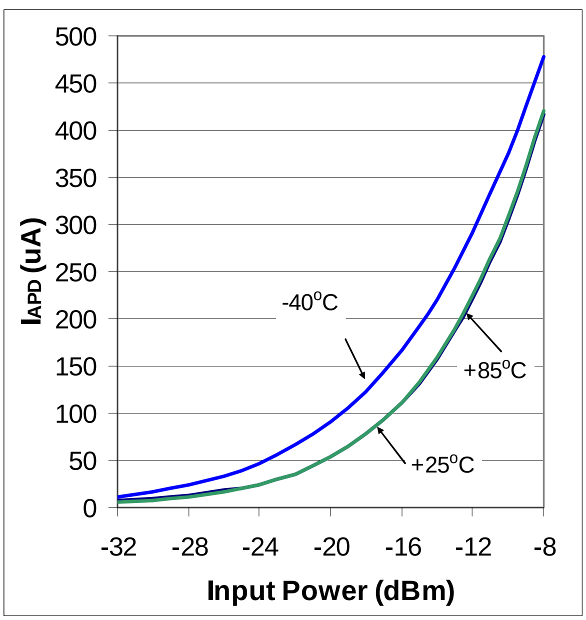
APD VOLTAGE vs. INPUT POWER



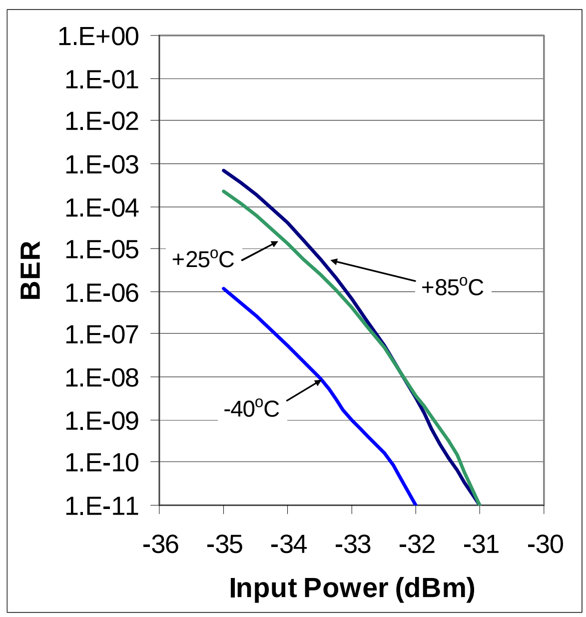
GAIN vs. INPUT POWER



APD CURRENT vs. INPUT POWER



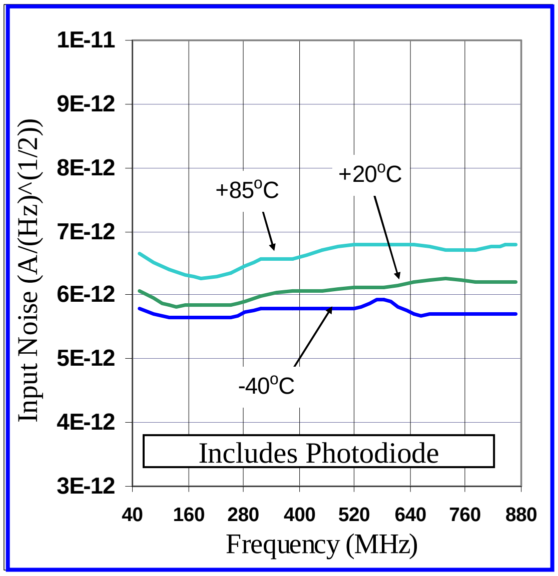
BIT ERROR RATIO vs. INPUT POWER



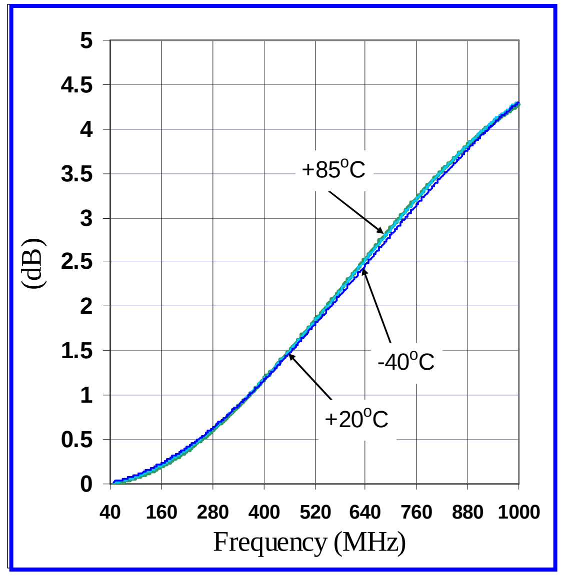
9 Analog Receiver Characteristic Graphs

(T_A = +25°C, V_{CC} = +5V, unless otherwise noted.)

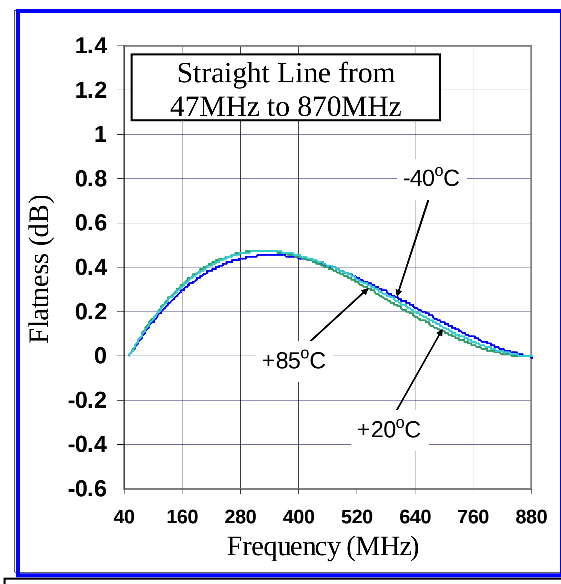
INPUT REFERRED NOISE vs. FREQUENCY



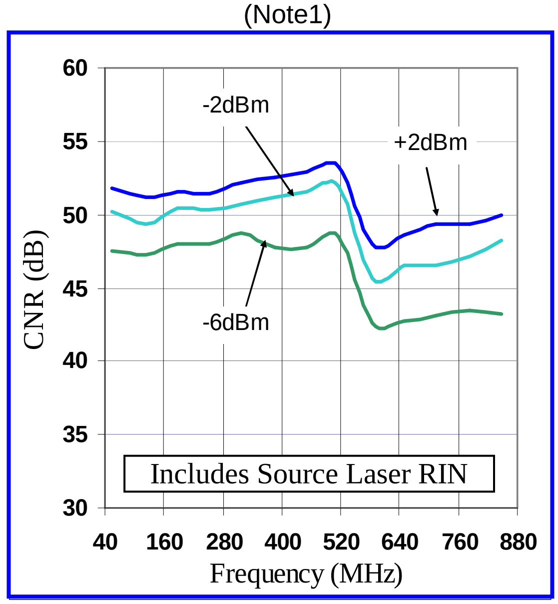
BANDWIDTH / TILT



GAIN FLATNESS vs. FREQUENCY



CARRIER to NOISE RATIO
(Note1)

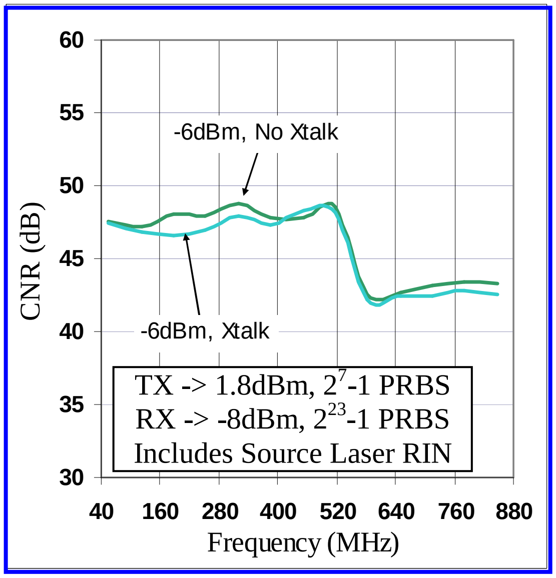


Note 1: Measured using 132 Channels, 3.4%OMI for channels < 517MHz (77 Channels), 1.7% OMI for channels > 517MHz (65 Channels)

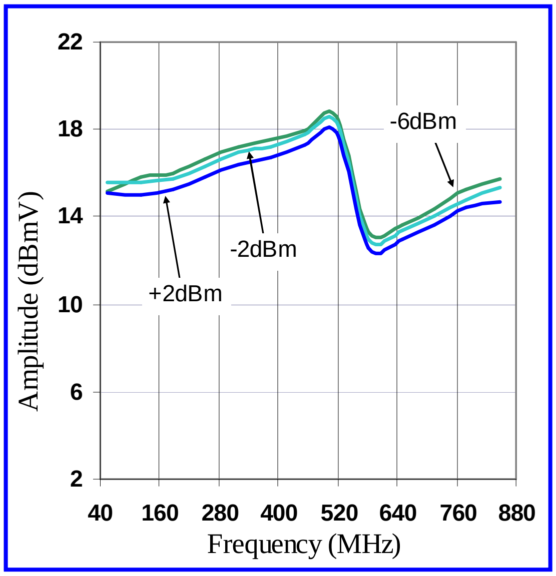
Analog Receiver Characteristic Graphs (Continued)

(T_A = +25°C, V_{CC} = +5V, unless otherwise noted.)

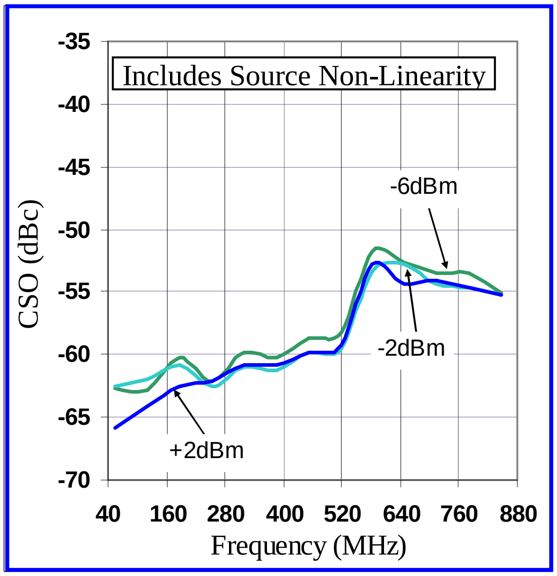
CARRIER to NOISE RATIO
(With Digital TX, RX Operating, Note 1)



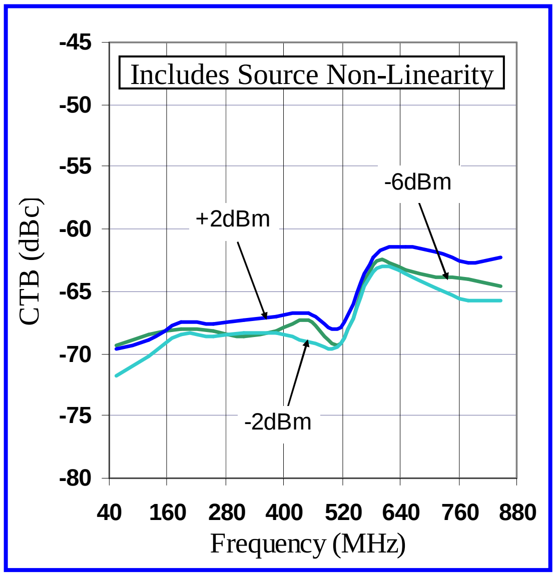
OUTPUT AMPLITUDE
(Note 1)



COMPOSITE SECOND ORDER
(Note 1)



COMPOSITE TRIPLE BEAT
(Note 1)

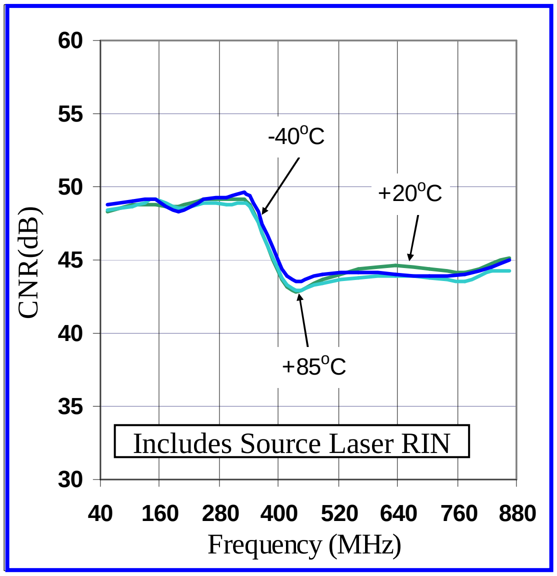


Note 1: Measured using 132 Channels, 3.4%OMI for channels < 517MHz (77 Channels), 1.7% OMI for channels > 517MHz (65 Channels)

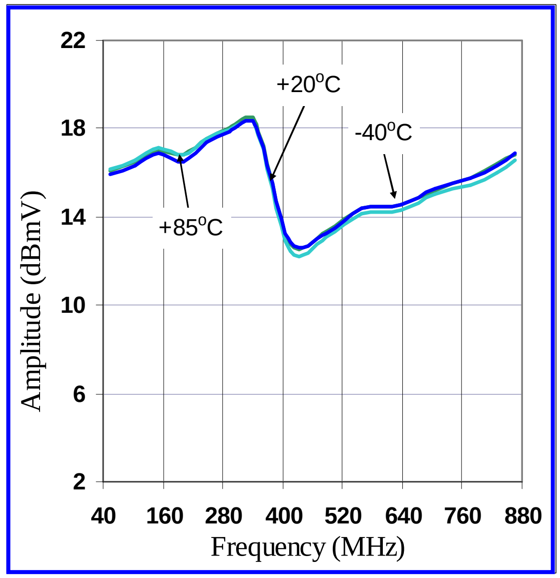
Analog Receiver Characteristic Graphs (Continued)

(T_A = +25°C, V_{CC} = +5V, unless otherwise noted.)

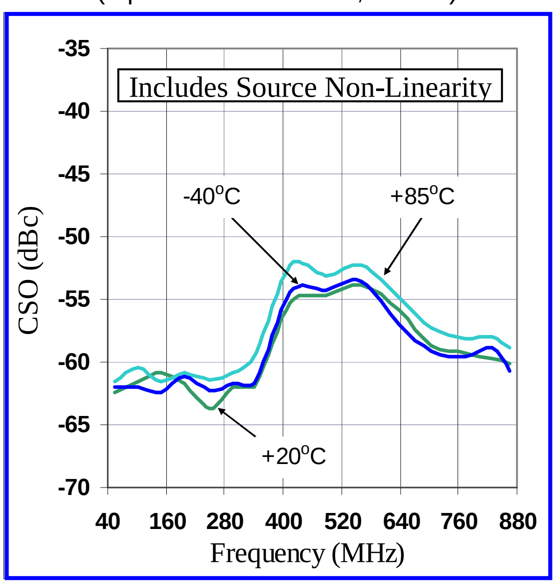
CARRIER to NOISE RATIO
(Input Power = -6dBm, Note 2)



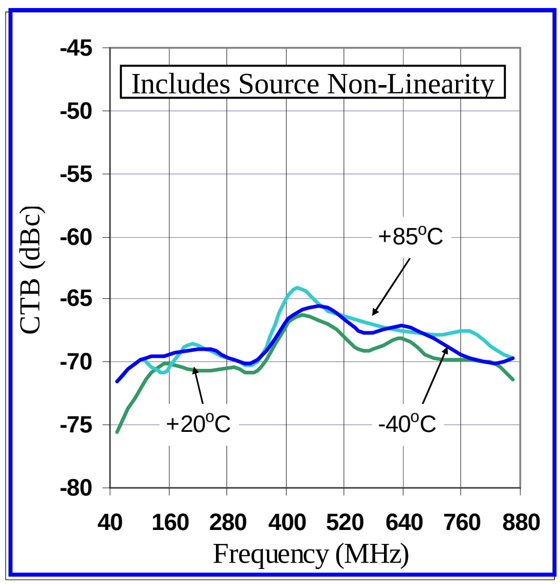
OUTPUT AMPLITUDE
(Input Power = -6dBm, Note 2)



COMPOSITE SECOND ORDER
(Input Power = -6dBm, Note 2)



COMPOSITE TRIPLE BEAT
(Input Power = -6dBm, Note 2)

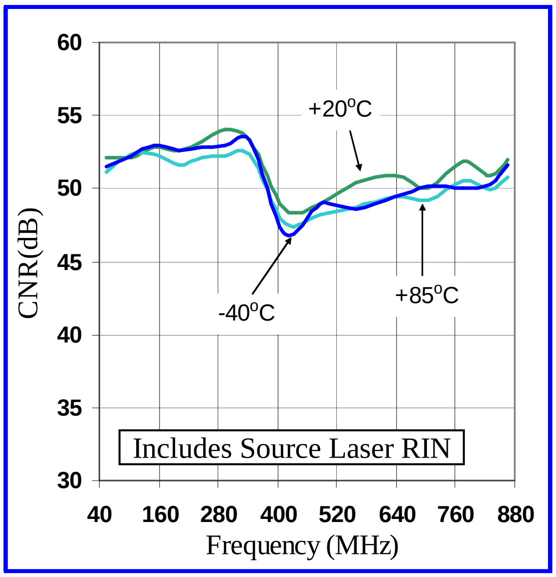


Note 2: Measured using 115 Channels, 4.0%OMI for channels < 344MHz (48Channels), 2.0% OMI for channels > 344MHz (67 Channels)

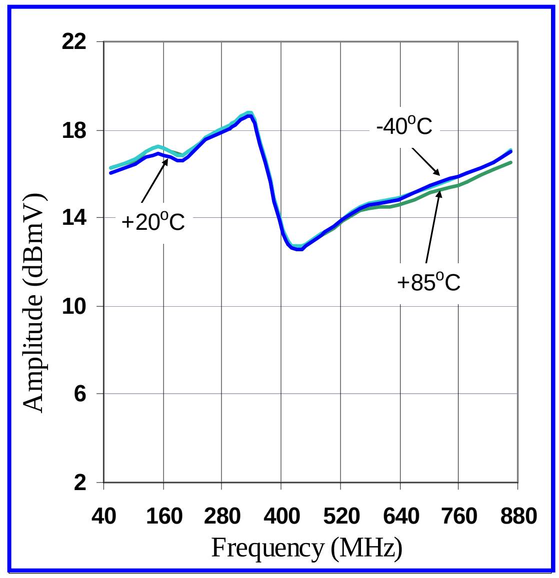
Analog Receiver Characteristic Graphs (Continued)

(T_A = +25°C, V_{CC} = +5V, unless otherwise noted.)

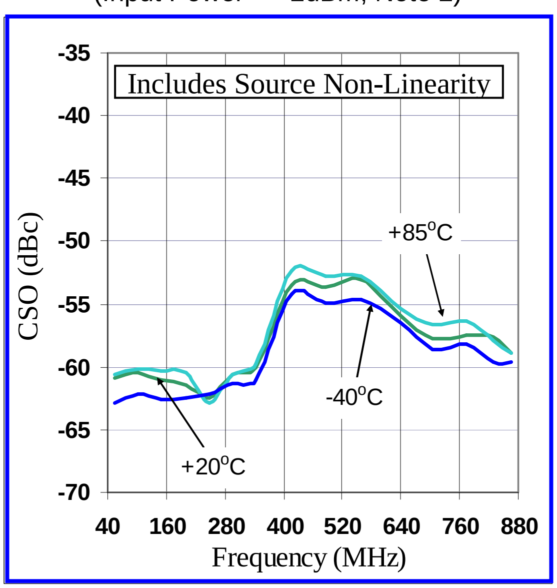
CARRIER to NOISE RATIO
(Input Power = +2dBm, Note 2)



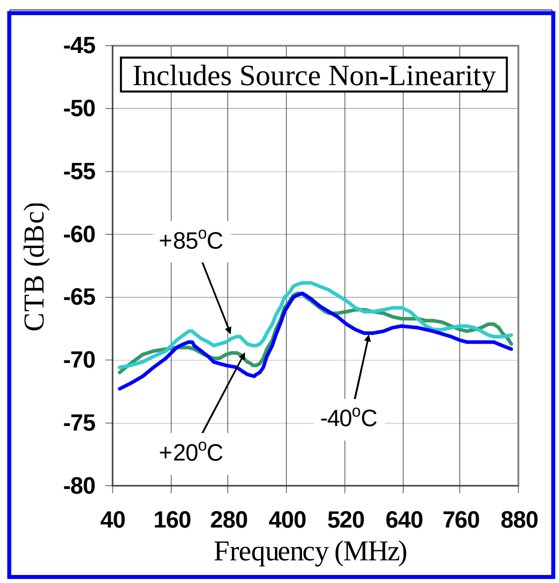
OUTPUT AMPLITUDE
(Input Power = +2dBm, Note 2)



COMPOSITE SECOND ORDER
(Input Power = +2dBm, Note 2)



COMPOSITE TRIPLE BEAT
(Input Power = -6dBm, Note 2)



Note 2: Measured using 115 Channels, 4.0%OMI for channels < 344MHz (48Channels), 2.0% OMI for channels > 344MHz (67 Channels)

10 Application Information

10.1 PON Compliance

This reference design is intended to aid PON ONT / ONU module designers and is not intended to take the place of the entire design process. The ONT / ONU designer should evaluate the reference design and modify it as necessary to meet the specification for each particular project. The designer should also carefully consider safety and EMI issues related to the specific application.

10.2 APD BIAS VOLTAGE

The APD bias voltage must be changed as temperature changes to obtain acceptable performance. This is accomplished on the HFRD 22.3 reference design using a thermistor and resistor divider network. The compensation is non-ideal but provides the basic compensation needed for simple evaluation of the reference design over a broad temperature range. For applications that operate from -40°C to +85°C a closed loop APD controller or look-up table driven temperature compensation is recommended to obtain optimal sensitivity and overload.

The GUI software provides an additional compensation feature by storing APD voltage settings in a look-up table located in the DS1863 (Table 3, 80 to A0). A new value is stored in the DS1863 EEPROM memory for every 4°C of t over the -40°C to 88°C temperature range. As the temperature changes the software updates the APD voltage setting by changing the DAC code value inside the MAX1932. This feature can be disabled by un-checking a box in the GUI software (Figure 3).

10.3 Gerber Files

The Gerber files for this reference design are available by emailing: https://support.maxim-ic.com/.

10.4 Layout Considerations

Single-ended and differential transmission lines are used on the HFRD 22.3 PCB board. Changing the PCB layer profile (see Section 16) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

11 Evaluation Quick Start

11.1 Evaluation Notice

The HFRD 22.3 reference design has DC-coupled I/O (See Sections 12 and 14) and a large optical output signal (approximately +1.0 to +2.0dBm). When evaluating the HFRD 22.3 reference design board, ensure that proper connections are made to the test equipment. Also check that all signal levels are within the proper range (common-mode, differential swing, optical Input / output power, etc.) so as to not damage the test equipment or reference design.

Precautions must also be taken in order to insure safe operation when using a device with a laser diode. Laser light emissions can be harmful and may cause eye damage. Maxim assumes no responsibility for harm, injury or test equipment damage as a result of the use of this reference design.

11.2 Evaluation Software

HFRD 22.3 comes complete with a windows based graphical user interface (GUI). The GUI communicates to the board through an easy to use USB connection. Through the software the user can monitor and change all of the critical parameters of the evaluation board. The software is available at: http://www.maxim-ic.com/tools/other/. Please check the website regularly for updates and revision history.

11.2.1 Software Requirements

The evaluation software is designed to operate on Windows 2000 or XP platforms. The software can also be used on Windows 98; however in that case unstable software operation may occur if the USB cable is unplugged without first stopping the device from windows.

11.2.2 Software Installation

To install the software, simply download the file from (http://www.maxim-ic.com/tools/other/) and run it on your computer or run the Setup.exe file from the provided CD ROM. The evaluation software runs on the Windows .NET platform. If this platform is not already installed on your computer the evaluation software will need an internet connection to complete the installation.

11.3 Evaluation Setup

After the software has been installed make the following connections to the HFRD 22 board:

1. Clean and inspect the fiber pigtail connector and then re-cap the fiber connector. In all of the proceeding steps, handle the fiber with care assuming that laser light could be emitted from the laser diode so as to not cause eye or equipment damage. Note that the output of the laser pigtail can be in excess of 2dBm. Use safe handling procedures and use an optical attenuator if needed to ensure that the power level is within the safe operating limits of the test equipment.
2. Connect a +5.0V supply to J14 (+5V) and J16 (GND). Set the current limit to 500mA. All other supply voltages are generated on the evaluation board from the +5V supply input.
3. Connect the USB cable from the computer to the HFRD 22 board. A green LED (D6, USB_OK) should be illuminated indicating that the USB controller has power.
4. Run the MOGPON program from the Windows start menu and press the "Initialize / Test Communications" button (Figure 2).
5. Pressing the *Initialize / Test Communications* button switches power on to the evaluation board. The software then examines the board and determines which board, of the HFRD 22 series, is connected on the bus. The software will then bring up a configuration menu for that evaluation board (Figure 3).
6. Adjust the external power supply voltage to ensure that the reported analog video supply voltage is between 4.9V and 5.1V.
7. Insure that the Digital Burst TX and Digital RX supplies are approximately +3.3V and that the Video Pin Bias voltage is between +12V and +15V. These voltages can be adjusted using the up and down control boxes below the reported voltages and currents.
8. The APD bias voltage, Modulation Current, and the APC Set current will also be calibrated before shipment. These values can be adjusted; however for the initial evaluation, it is recommended that you use the calibrated values.
9. The MAX1932 uses volatile memory to set the APD bias voltage on each power up the MAX1932 defaults to the FF (lowest voltage in the set range). The GUI software reads a calibration value out of the DS1863 EEPROM (Table 3, Address 80h) and loads it into the MAX1932. Each time the board is re-initialized or powered-up the calibration value will be loaded. After initialization the values can be adjusted using the Controls provided in the GUI.
10. The remaining setup steps will depend greatly on which section of the reference design will be evaluated and what test equipment is available. To complete the setup, review the schematic carefully, noting the DC-coupled connections of IN and BEN, and make the appropriate optical and electrical connections. If assistance is required, please email questions to https://support.maxim-ic.com/.

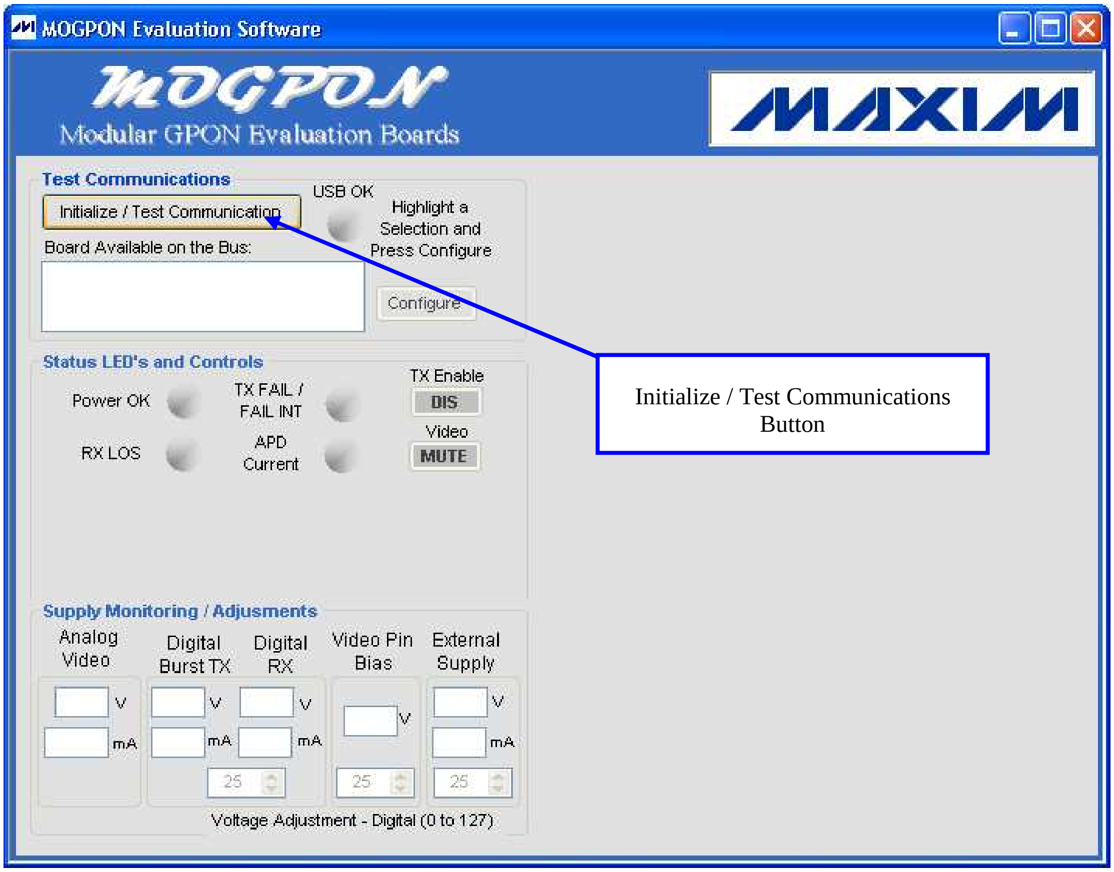


Figure 2: MOGPON Evaluation Software (Initialize)

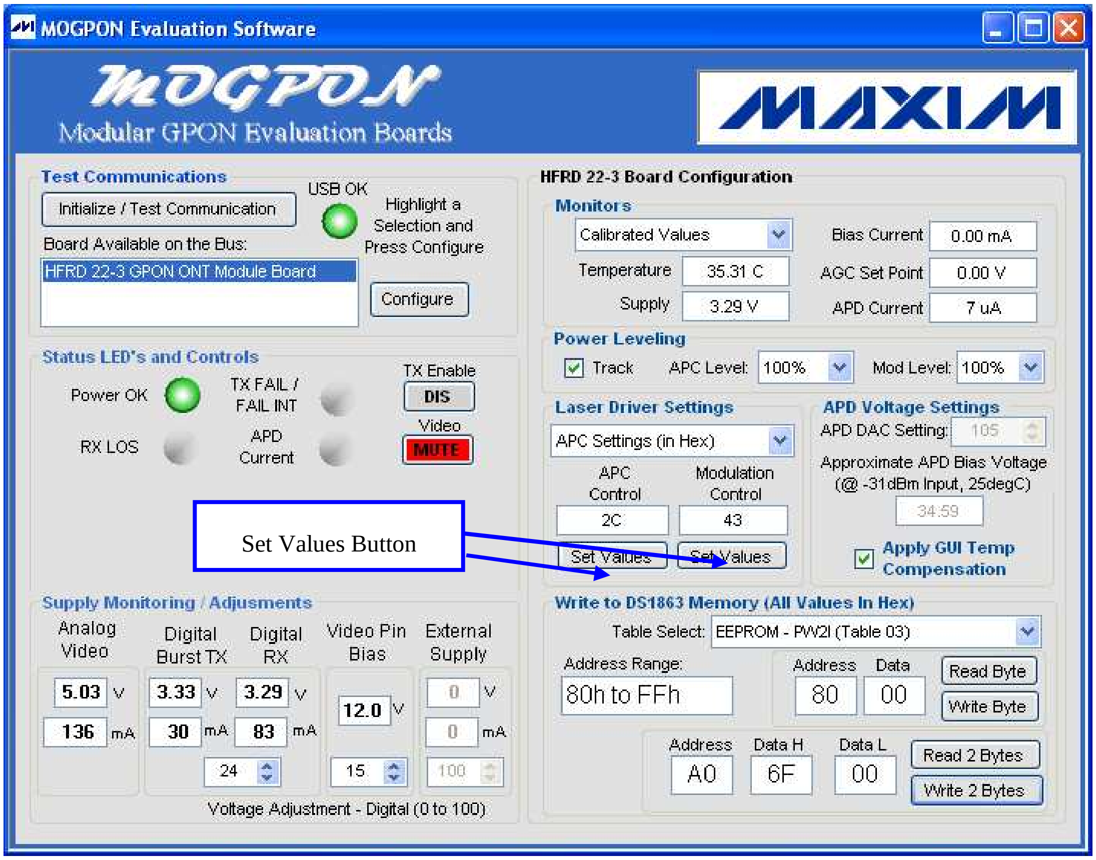


Figure 3: MOGPON Evaluation Software, HFRD 22.3 Configuration Screen

11.4 Software Usage / Options

11.4.1 Monitors

The HFRD 22 MOGPON evaluation software provides monitors for various key operating parameters of the reference design board. These values should be used as approximations and should be verified with high-quality DMM tools if a high-accuracy value is required.

11.4.2 Temperature Compensation

The HFRD 22.3 reference design uses a temperature controlled lookup table inside the DS1863 to provide automatic control of the transmitter modulation current as temperature changes. If desired, a second look-up table can be used to provide temperature compensation of the monitor diode tracking error.

The MOGPON evaluation software provides simple tools to load and read the temperature compensated values. By clicking the set values button (Figure 3) for the Modulation Current or APD Control, a temperature compensation window (Figures 4, 5) will be shown.

The software allows the user to fill a selection (Figure 4) or the entire table (Figure 5) with a specific fixed value or have the software calculate the value based on an equation. To best fit the desired curve the software offers options to fill the table with a linear, power or polynomial function. When using the equation input, always use decimal values. By pressing CAL the new values will be calculated for the selected temperatures. If the values match the desired and expected values, press FILL to write the values into the table.

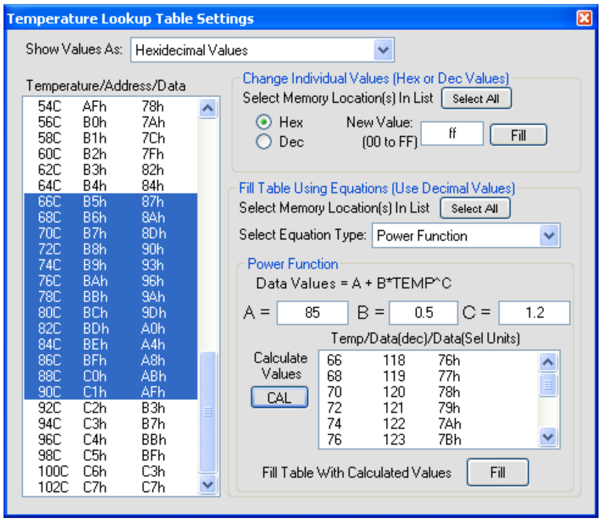


Figure 4: MOGPON Evaluation Software, Temperature Lookup Table, selection 1

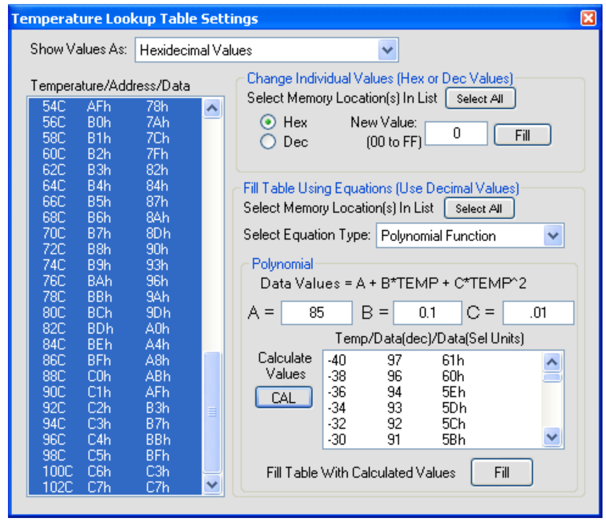


Figure 5: MOGPON Evaluation Software, Temperature Lookup Table, selection 2

12 I/O and Control Description

Component	NAME	FUNCTION
J1	OUT	Receiver (MAX3747) Non-Inverted Data Output, AC-Coupled
J2	OUTo	Receiver (MAX3747) Inverted Data Output, AC-Coupled
J3	USB	USB Mini Type B connector, connect to a computer through the provided cable.
J4	EXT	ZIF connector for external board power and communication
J5	INo	Transmitter (MAX3643) Non-Inverted Data Input, DC-Coupled*
J6	IN	Transmitter (MAX3643) Inverted Data Input, DC-Coupled*
J7	BENo	Transmitter (MAX3643) Non-Inverted Burst Enable Input, DC-Coupled*
J8	BEN	Transmitter (MAX3643) Inverted Burst Enable Input, DC-Coupled*
J14	VCC	+5V Power Supply Connection
J16	GND	Ground Power Supply Connection
J12	VID_OUT	Analog Video Output, 75Ω BNC
D4	V_RANGE	Supply voltage out of range failure. Feature not implemented on current board version.
D9	E_POK	External Supply Source Power OK. LED illuminates when the DC-DC converter (U24) is operating correctly providing a +3.3V supply to an external board through the J4 connection. If no board is connected the supply is shutdown and the LED will not be illuminated.
D10	M_POK	Power OK. LED illuminates when the low drop out regulator (U15) is operating correctly providing a +3.3V supply to the digital transmitter and receiver circuits.
D13	CL	APD Current Limit. LED illuminates when the APD current limit threshold (set by R34) has been reached.
D14	MUTE	Video MUTE. LED illuminates when the video output signal is muted.
D15	TX_FAIL	Digital Burst Transmitter APC loop Fail indicator. LED illuminates if the APC loop is unable to maintain the monitor diode set current. Additional fault conditions (if enabled in the DS1863) can also trigger the TX_FAIL signal. See the DS1863 data sheet for additional information.
D16	TX_EN	Digital Burst Transmitter Enable. LED illuminates when the MAX3643 has been enabled.
D19	LOS	Loss-of-Signal. LED illuminates when the input signal to the MAX3747 decreases below the preset threshold set by the TH pin. See MAX3747 data sheet for additional information).
TP17, TP23	GND	Monitoring Test Point for ground (GND).

*DC-Coupled I/O. Insure that the DC voltage on these pins is compatible with the test equipment before making any connections.

13 Component List

DESIGNATION	QTY	DESCRIPTION
C1, C21, C54	3	Open (0402)
C2	1	1µF ± 10%, 25V Ceramic Capacitor (0805)
C3	1	0.22µF ± 10%, 10V Ceramic Capacitor (0402)
C4, C80	2	1000pF ± 10% 25V Ceramic Capacitor (0402)
C5, C86	2	0.47µF ± 20%, 10V Ceramic Capacitor (0402)
C6	1	680pF ± 10% 10V Ceramic Capacitor (0402)
C7, C46 – C48, C87, C88	6	1µF ± 20%, 10V Ceramic Capacitor (0402)
C8	1	22pF ± 10% 10V Ceramic Capacitor (0402)
C9	1	10pF ± 10%, 10V Ceramic Capacitor (0402)
C10	1	100pF ± 10%, 10V Ceramic Capacitor (0402)
C11 - C15, C19, C25 - C32, C35, C38 - C40, C42 -C45, C49, C50, C52, C56, C59, C63-C65, C67, C69, C90 - C92, C94	36	0.1µF ± 10%, 10V Ceramic Capacitor (0402)
C16, C23	2	0.1µF ± 10% 100V Ceramic Capacitor (0805)
C17, C72	2	2.2µF ± 10% 10V Ceramic Capacitor (0603)
C18, C22	2	33pF ± 10% 10V Ceramic Capacitor (0402)
C20, C41	2	3300pF ± 10% 10V Ceramic Capacitor (0402)
C24, C75-C78	5	0.01µF ± 10%, 10V Ceramic Capacitor (0402)
C33, C71, C85	3	0.1µF ± 10%, 100V Ceramic Capacitor (0603)
C34, C51, C55, C57, C62, C66, C93	7	1µF ± 10%, 10V Ceramic Capacitor (0603)
C36	1	0.001µF ± 10%, 100V Ceramic Capacitor (0603)
C37, C73	2	4.7µF ± 10%, 25V Ceramic Capacitor (0805)
C53	1	Open (0603)
C58, C82, C83	3	0.01µF ± 10% Ceramic Capacitor (0603)
C60, C61	2	4700pF ± 10% Ceramic Capacitor (0402)
C68, C79, C89	3	10µF ± 20%, 6.3V Ceramic Capacitor (0603)
C70	1	22µF ± 20%, 10V Ceramic Capacitor (1206)
C74	1	2.2µF ± 10%, 25V Ceramic Capacitor (0805)
C81	1	4.7µF ± 10%, 10V Ceramic Capacitor (0603)
C84	1	10µF ± 10%, 10V Ceramic Capacitor (0805)
D1, D2	2	Diode Panasonic MA27P0100LCT
D3	1	Diode Diodes Inc, BAT46W
D4, D6, D9, D10, D16	5	Green LED
D13 - D15, D19	4	Red LED
D5	1	Optical Triplexer ExceLight SXT5241-Q/GP1
D8	1	Schotkey Diode Panasonic MA2Z785-00LCT
J1, J2, J5 - J8	6	Side Mount SMA Connector, Tab Contact
J3	1	USB (B Mini) Connector Tyco 440247-1
J4	1	ZIF Connector Molex 52207-1085
J12	1	Side Mount 75Ω BNC Connector, Trompeter UCBJE20-1
J14, J16	2	Test Points
L1	1	Short
L3	1	47µH ±20% Inductor (1210) Taiyo-Yuden CBC3225T470M
L4 – L6, L8, L9, L15	6	1500Ω Ferrite Bead (0402) TDK MMZ1005A152ET
L7, L11	2	2.2nH ±10% Multilayer Inductor (0402)
L10	1	22µH ±20% Inductor (1210) Taiyo-Yuden CBC3225T220M
L12	1	3.5µH ±10% Inductor (1210) Toko D52LC
L14	1	8.2nH ±10% Multilayer Inductor (0402)
L18	1	4.7µH ±20% Inductor (1210) Taiyo-Yuden CBC3225T4R7M
L22, L25, L26	3	1500Ω Ferrite Bead (0603) TDK MMZ1608A152ET
Q1, Q3	2	MOSFET Fairchild FDN302P
Q2	1	Transistor Fairchild BSS123
R1, R2, R17, R29, R40, R56, R78, R80, R90, R93, R101	11	0Ω ±5% Resistor (0402)

Component List (Continued)

R3, R58, R75, R76, R106	5	100Ω ±1% Resistor (0402)
R4, R6, R11, R12, R32, R34, R54	7	1kΩ ±1% Resistor (0402)
R5	1	20.0Ω ±5% Resistor (0402)
R7	1	82.5Ω ±1% Resistor (0402)
R8, R9	2	2.67Ω ±1% Resistor (0402)
R10	1	22kΩ ±1% Thermistor (0402) Panasonic ERT-J0ER223J
R13 - R16, R19, R25, R44, R74, R77, R89, R94, R97 – R99, R102, R104, R109, R111, R112	19	Open (0402)
R18, R61, R67 - R72	8	470Ω ±5% Resistor (0402)
R20, R21	2	130Ω ±5% Resistor (0402)
R22, R23	2	82Ω ±5% Resistor (0402)
R24	1	1.5kΩ ±1% Resistor (0402)
R26, R103	2	20kΩ ±1% Resistor (0402)
R27, R64, R87, R88	4	24.9kΩ ±1% Resistor (0402)
R28, R33, R49 – R51, R83, R85, R92, R107, R108	10	10kΩ ±1% Resistor (0402)
R30, R31, R52, R55, R62, R66, R73, R86	8	49.9Ω ±1% Resistor (0402)
R35	1	499kΩ ±1% Resistor (0402)
R36	1	11kΩ ±1% Resistor (0402)
R37, R41, R48, R60	4	4.7kΩ ±5% Resistor (0402)
R42, R43	2	1.62kΩ ±1% Resistor (0402)
R45	1	82.5kΩ ±1% Resistor (0402)
R46, R47	2	110kΩ ±1% Resistor (0402)
R53	1	33.2kΩ ±1% Resistor (0402)
R57	1	7.5kΩ ±1% Resistor (0402)
R59	1	86.6kΩ ±1% Resistor (0402)
R63, R82	2	49.9kΩ ±1% Resistor (0402)
R65	1	100kΩ ±1% Resistor (0402)
R79	1	39.2kΩ ±1% Resistor (0402)
R81	1	27kΩ ±5% Resistor (0402)

R84	1	15.0Ω ±1% Resistor (0402)
R91	1	681Ω ±1% Resistor (0402)
R95, R96, R100	3	0.1Ω ±1% Resistor (0402)
R105	1	80.6kΩ ±1% Resistor (0402)
R110	1	15kΩ ±1% Resistor (0402)
TP17, TP23	2	Test Points
U1	1	Burst Laser Driver Maxim MAX3643ETG
U2	1	Balun Transformer Pulse Engineering CX2038L
U3	1	PON Laser Controller Maxim DS1863E+
U4	1	Limiting Amplifier Maxim MAX3747EUB
U5	1	Video Amplifier Maxim MAX3654ETE+
U6	1	DC-DC Converter Maxim MAX5025EUT-T
U7	1	Operational Amplifier Maxim MAX4240EUK-T
U8	1	Digital Resistor Maxim DS3902U-530
U9	1	APD Bias Supply Maxim MAX1932ETC
U10	1	USB Microcontroller Microchip PIC16C745-I/SO
U11	1	Low Drop-Out Regulator Maxim MAX1793EUE-33
U12, U13, U16, U17	4	Inverter Fairchild NC7WZ04P6X
U14, U19	2	Quad ADC Maxim MAX1362EUB
U18	1	High Voltage Current Monitor Maxim MAX4007EUT-T
U20, U22, U23	3	High-Side Current Sense Maxim MAX4070AUA
U21	1	Bi-Directional Level Translator Maxim MAX3373EEKA-T
U24	1	DC-DC Converter Maxim MAX1556ETB
Y1	1	Crystal ECS INC. XC679CT
	1	HFRD 22.3 PCB
	1	MOGPON Evaluation Software Version 1.0
	1	USB A to USB B mini Cable

14 Schematic

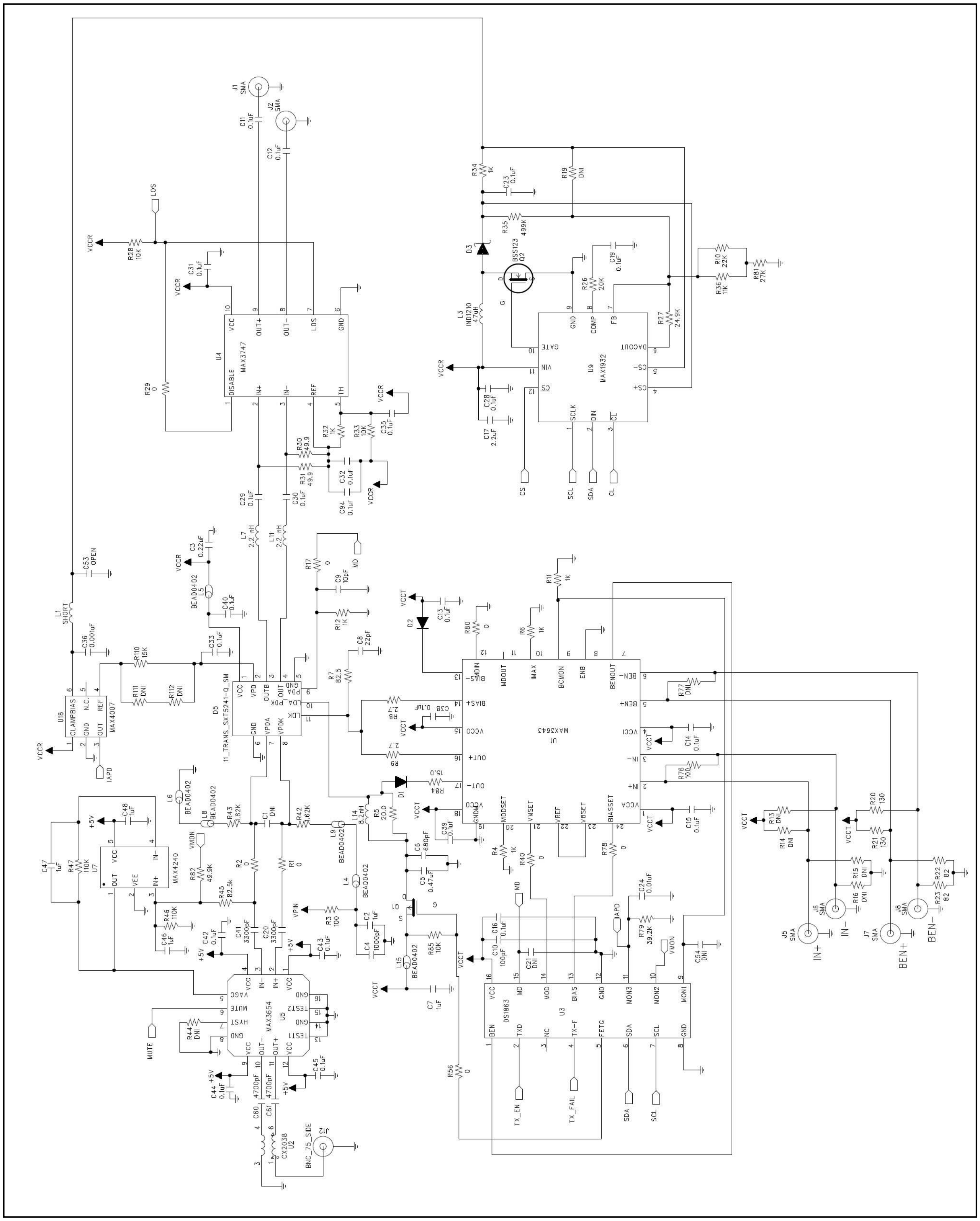


Figure 6: HFRD 22.3 Schematic, Part 1 - PMD Devices

Schematic (Continued)

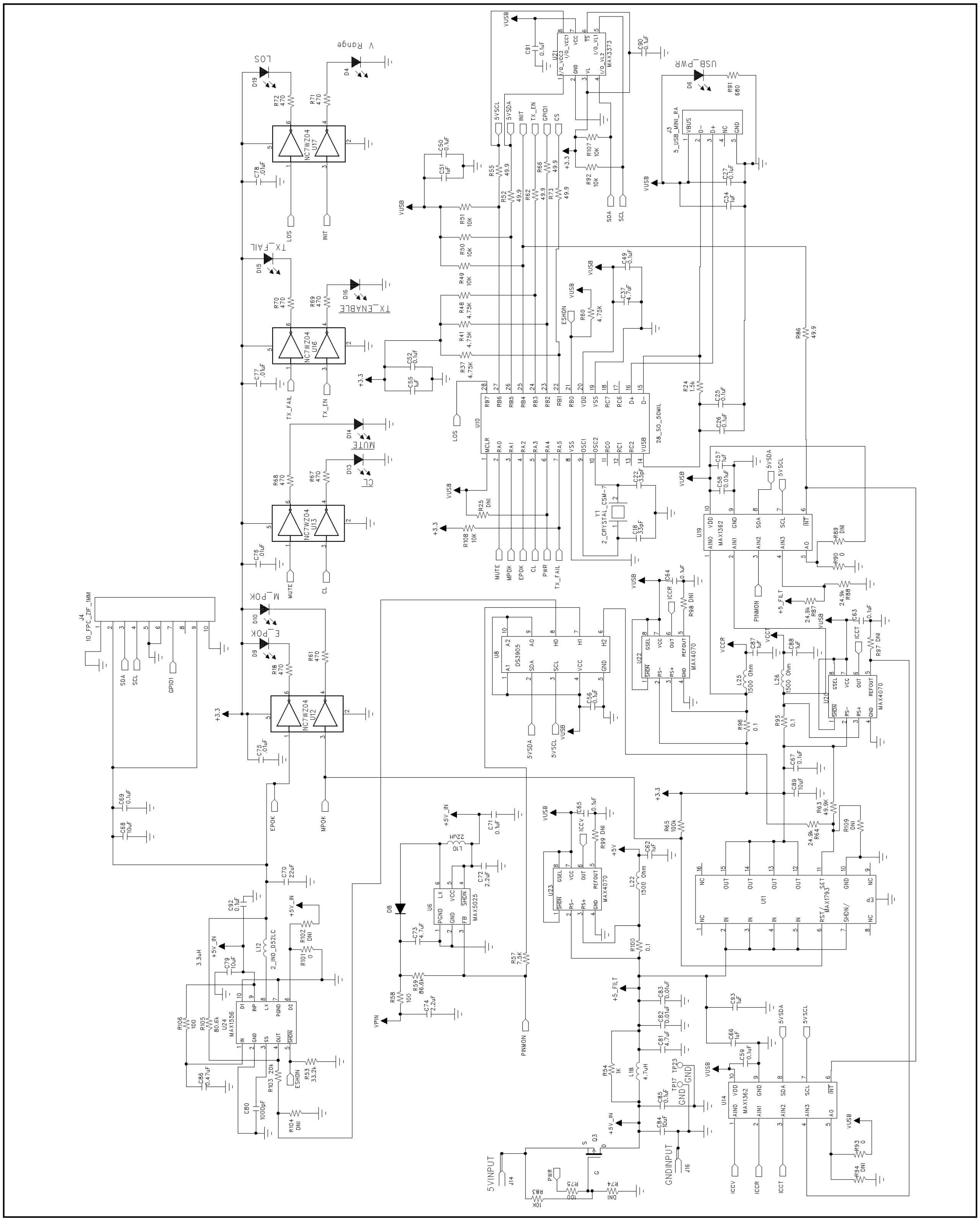


Figure 7: HFRD 22.3 Schematic, Part 2 - USB Control / Monitoring / Supply Management

15 Board Layout

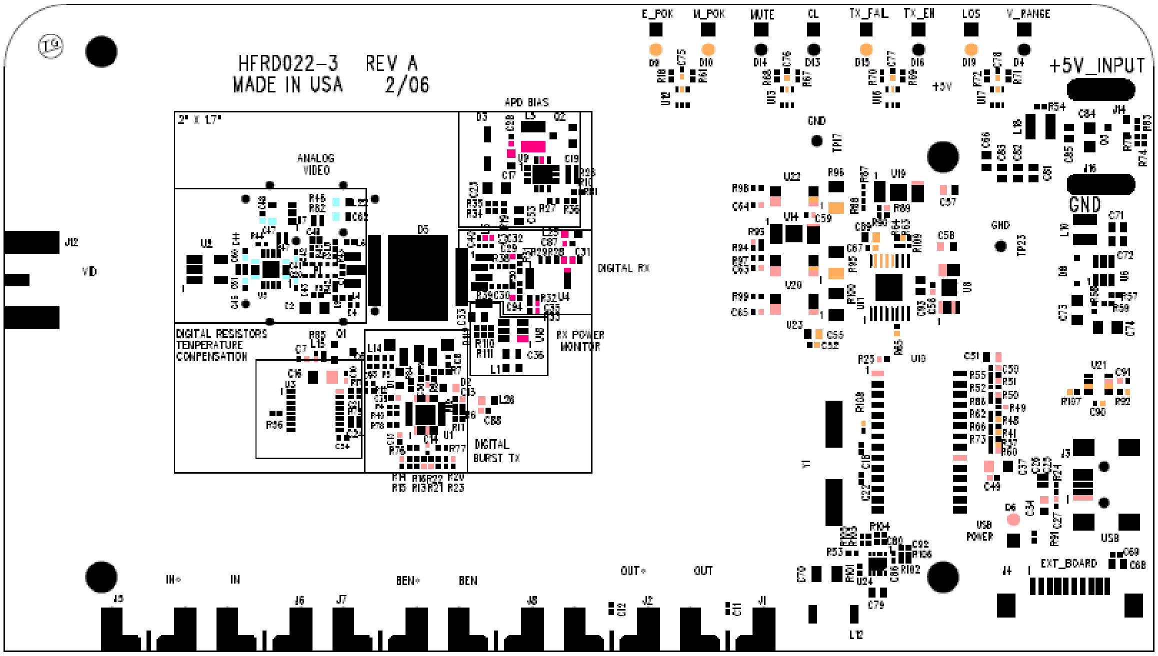


Figure 8: Component Placement Guide

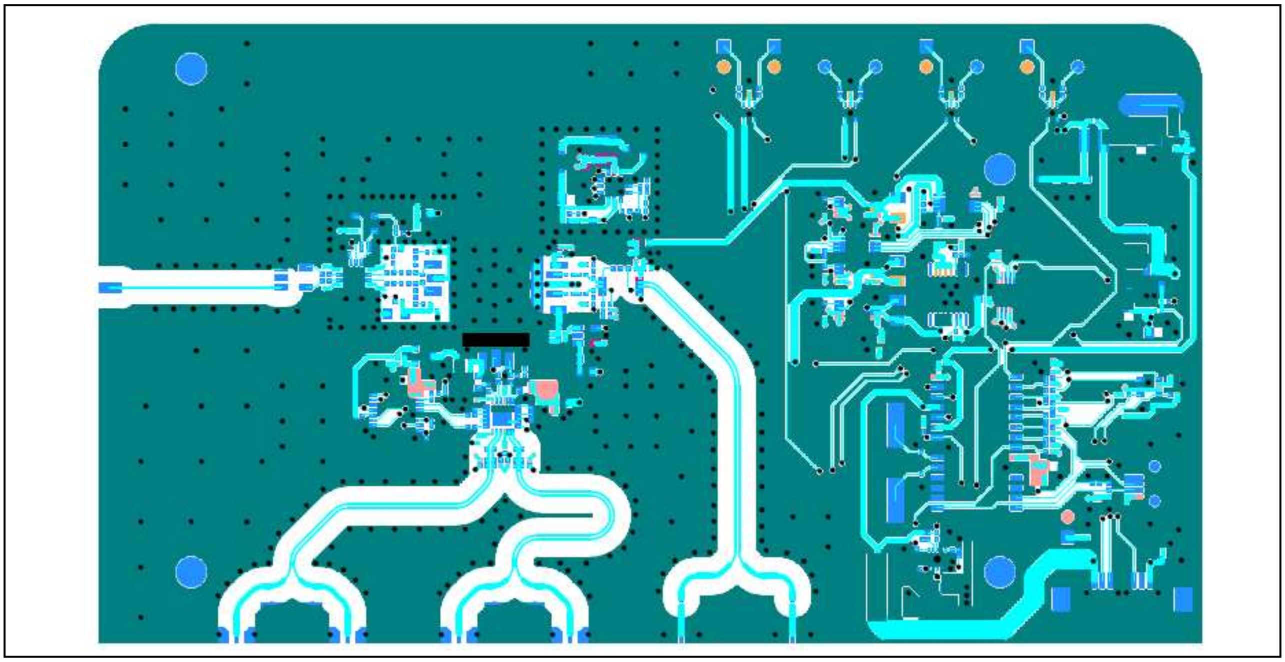


Figure 9: Board Layout, Layer 1

Board Layout (Continued)

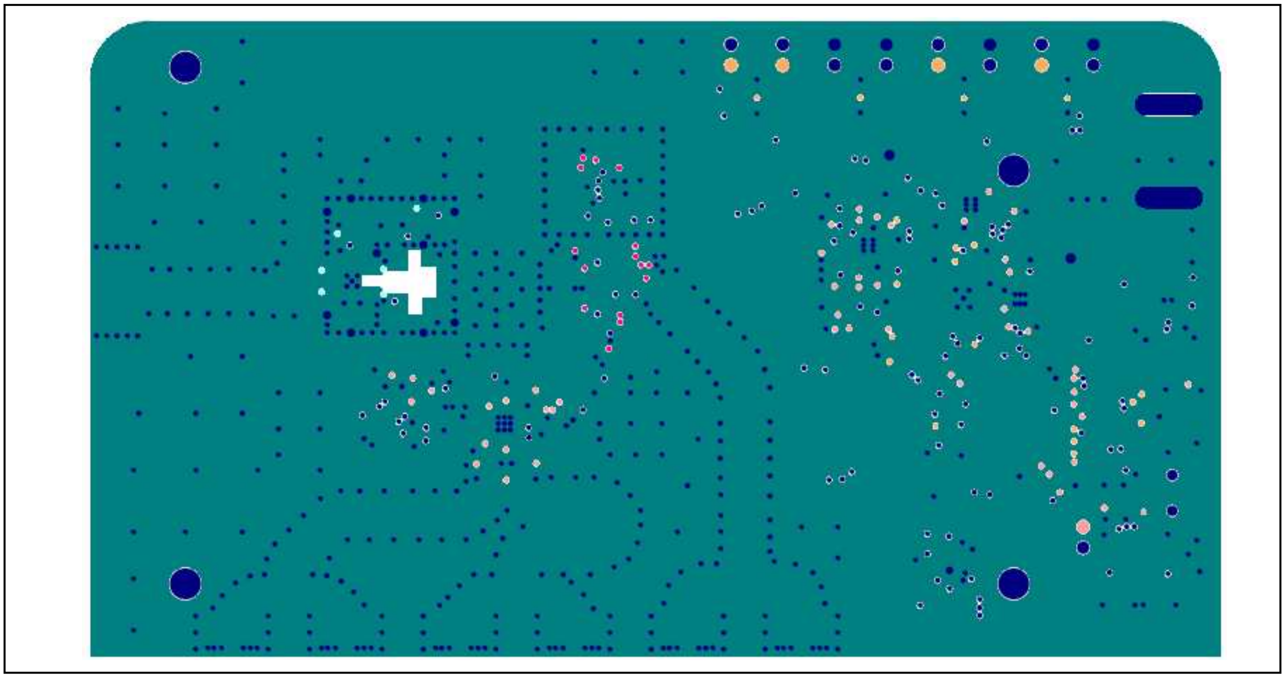


Figure 10: Board Layout, Layer 2

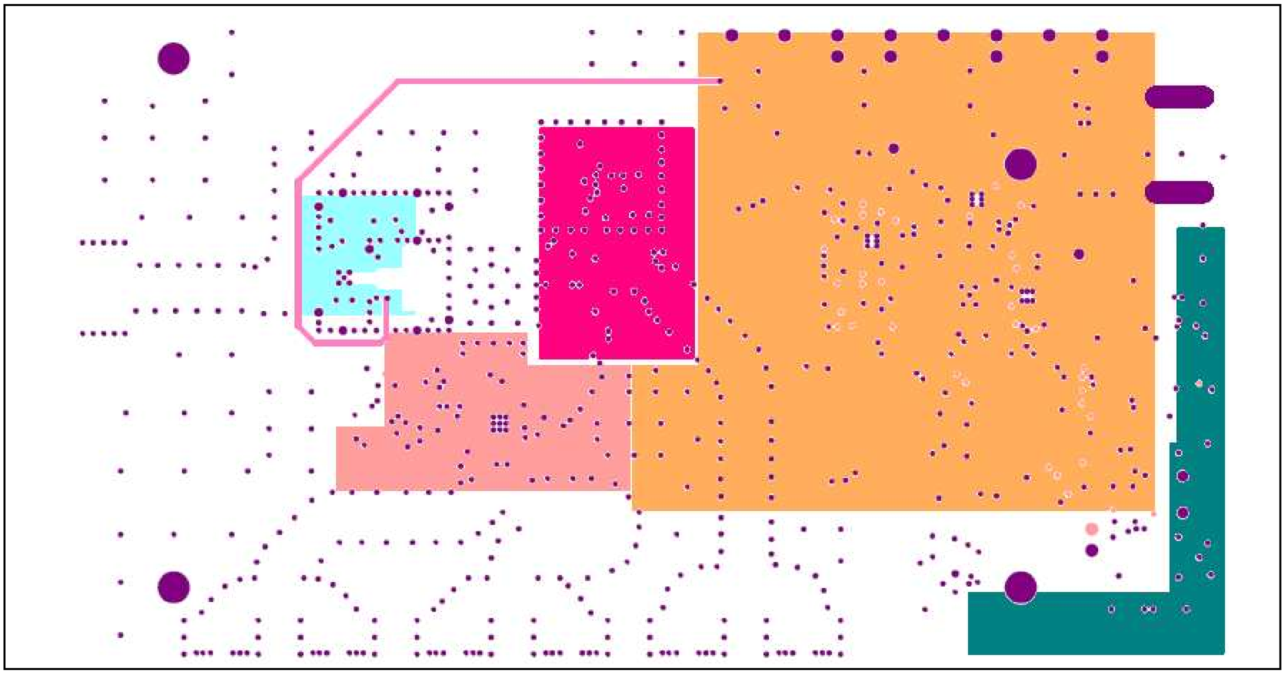


Figure 11: Board Layout, Layer 3

Board Layout (Continued)

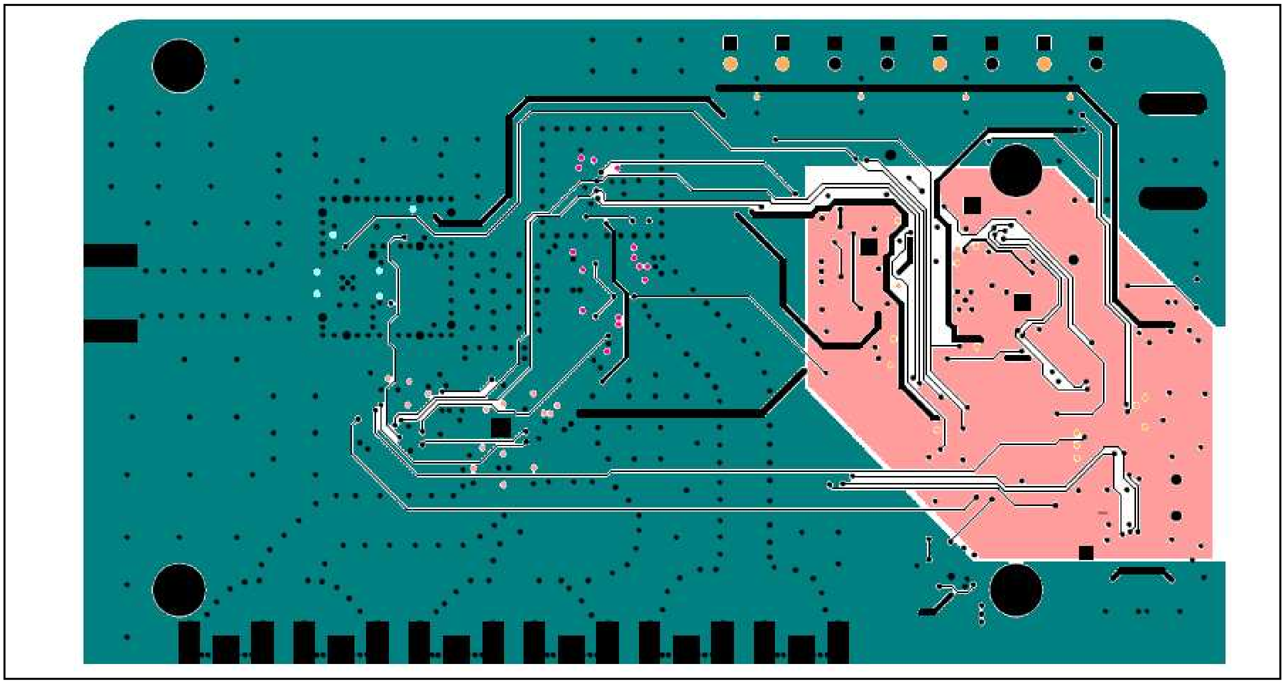


Figure 12: Board Layout, Layer 4

16 Layer Profile

The HFRD 22.3 reference design board includes controlled-impedance transmission lines. The layer profile is based on the following assumptions:

1. Dielectric material is FR4 with a dielectric constant of ~ 4.5
2. 1oz copper foil

	SINGLE ENDED	COUPLED
A	27mil	12mil
B	>50mil	7mil
C	15mil	15mil
D	As Needed	As Needed

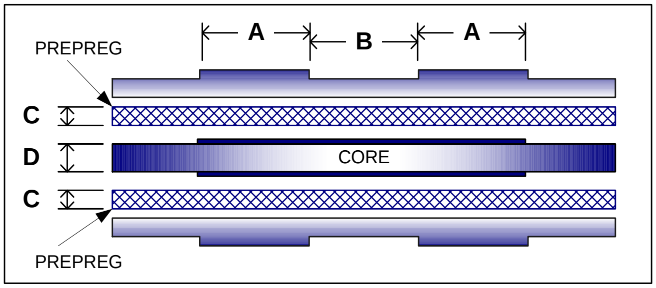


Figure 13: Layer Profile