

IRF7862PbF

HEXFET® Power MOSFET

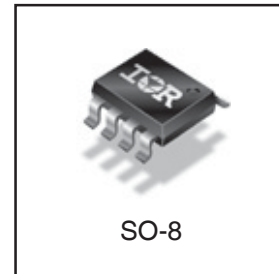
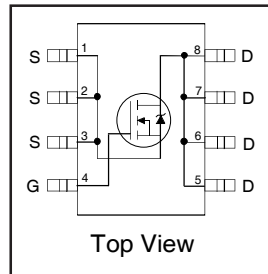
Applications

- Synchronous MOSFET for Notebook Processor Power
- Synchronous Rectifier MOSFET for Isolated DC-DC Converters

V_{DSS}	$R_{DS(on)}$ max	Qg
30V	3.3mΩ @ $V_{GS} = 10V$	30nC

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- 20V V_{GS} Max. Gate Rating
- 100% tested for Rg
- Lead-Free



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	21	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	17	
I_{DM}	Pulsed Drain Current ①	170	
P_D @ $T_A = 25^\circ C$	Power Dissipation	2.5	W
P_D @ $T_A = 70^\circ C$	Power Dissipation	1.6	
	Linear Derating Factor	0.02	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	—	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④	—	50	

Notes ① through ⑤ are on page 9

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.023	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	3.0	3.3	mΩ	V _{GS} = 10V, I _D = 20A ③
		—	3.7	4.5		V _{GS} = 4.5V, I _D = 16A ③
V _{GS(th)}	Gate Threshold Voltage	1.35	—	2.35	V	V _{DS} = V _{GS} , I _D = 100μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-5.4	—	mV/°C	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
gfs	Forward Transconductance	87	—	—	S	V _{DS} = 15V, I _D = 16A
Q _g	Total Gate Charge	—	30	45	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 16A See Figs. 15 & 16
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	7.5	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	3.1	—		
Q _{gd}	Gate-to-Drain Charge	—	9.8	—		
Q _{godr}	Gate Charge Overdrive	—	9.6	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	12.9	—		
Q _{oss}	Output Charge	—	18	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _g	Gate Resistance	—	1.0	1.6	Ω	
t _{d(on)}	Turn-On Delay Time	—	16	—	ns	V _{DD} = 15V, V _{GS} = 4.5V I _D = 16A R _G = 1.8Ω See Fig. 18
t _r	Rise Time	—	19	—		
t _{d(off)}	Turn-Off Delay Time	—	18	—		
t _f	Fall Time	—	11	—		
C _{iss}	Input Capacitance	—	4090	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	810	—		
C _{riss}	Reverse Transfer Capacitance	—	390	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	350	mJ
I _{AR}	Avalanche Current ①	—	16	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	170		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 16A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	17	26	ns	T _J = 25°C, I _F = 16A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	33	50	nC	di/dt = 430A/μs ③
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

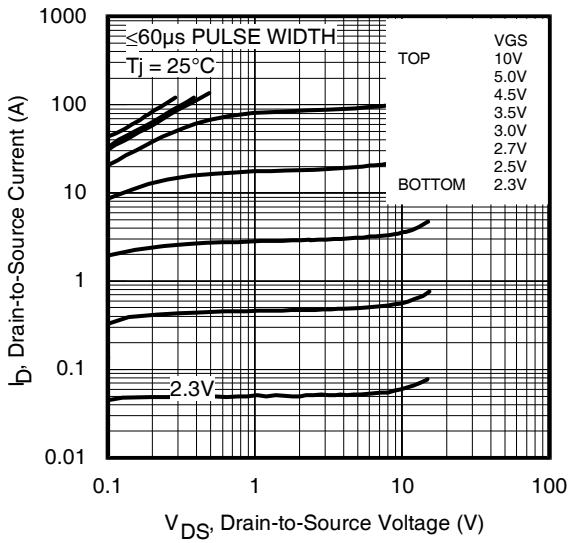


Fig 1. Typical Output Characteristics

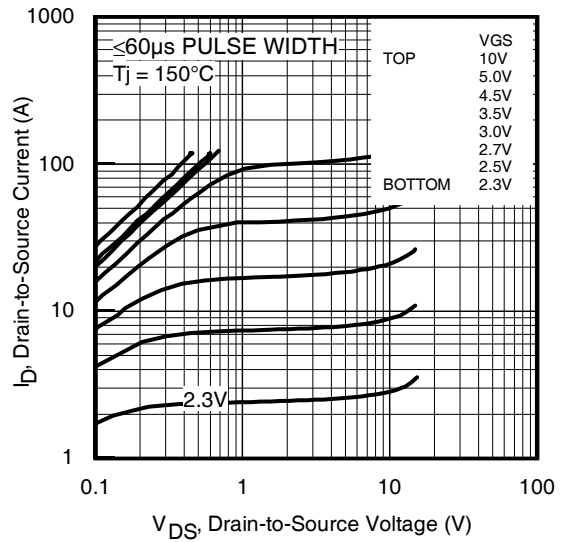


Fig 2. Typical Output Characteristics

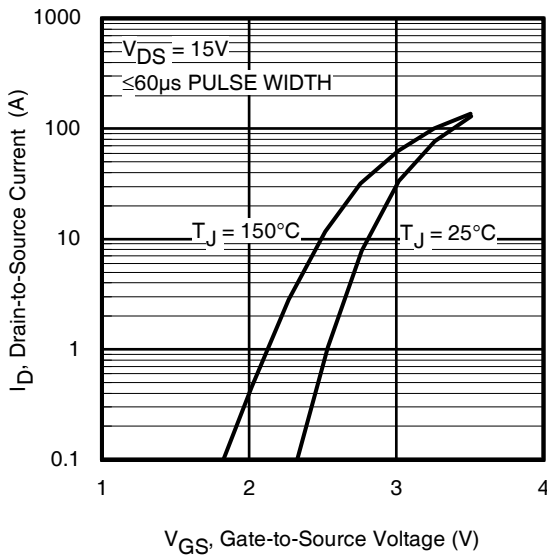


Fig 3. Typical Transfer Characteristics

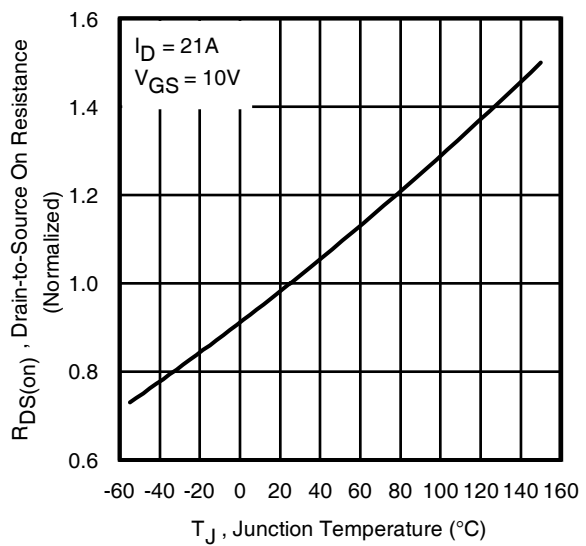


Fig 4. Normalized On-Resistance vs. Temperature

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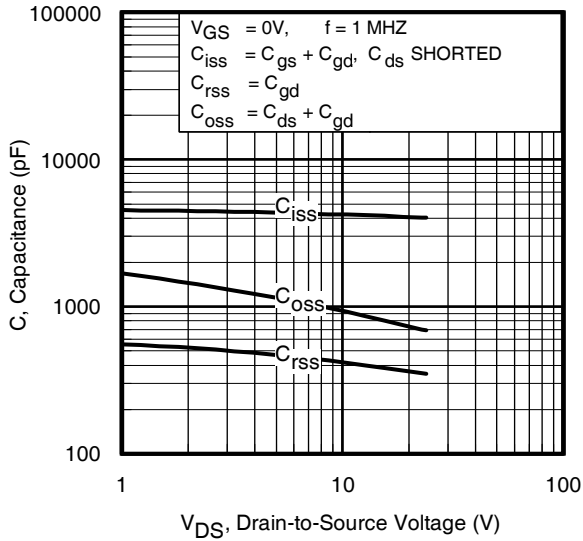


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

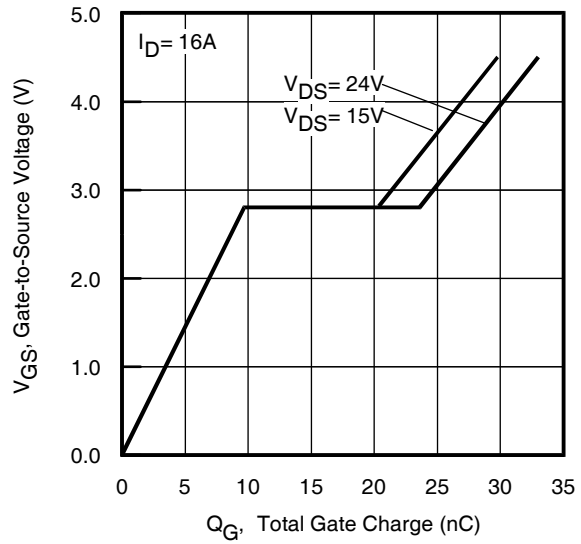


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

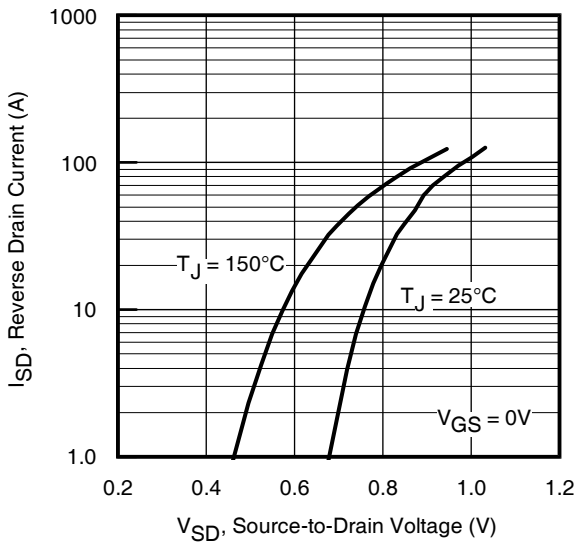


Fig 7. Typical Source-Drain Diode Forward Voltage

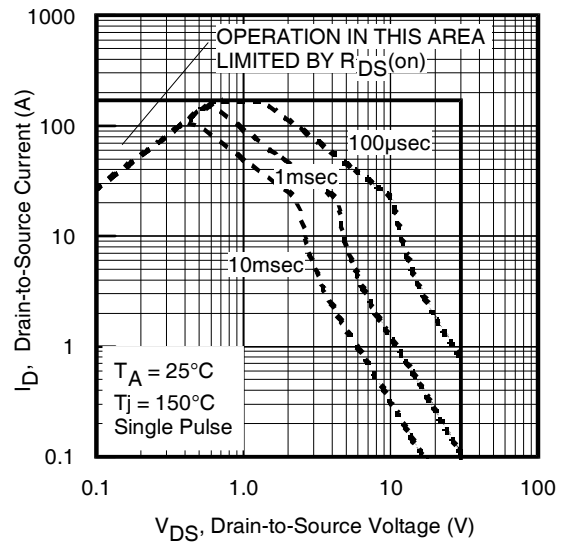


Fig 8. Maximum Safe Operating Area

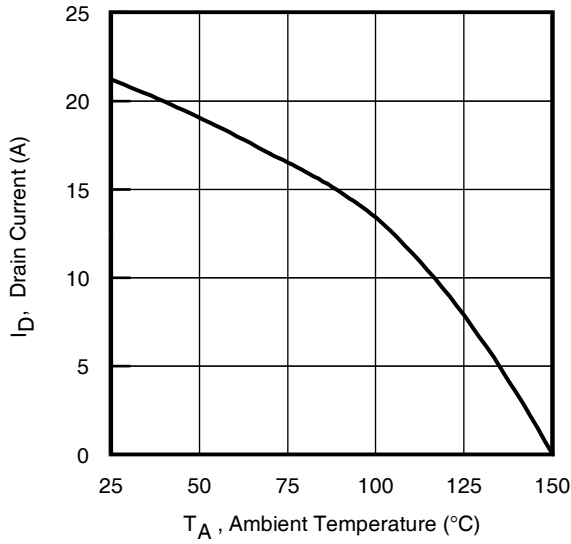


Fig 9. Maximum Drain Current vs. Ambient Temperature

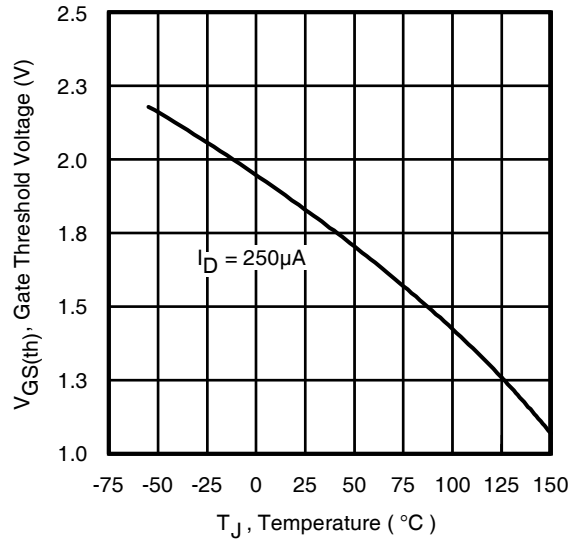


Fig 10. Threshold Voltage vs. Temperature

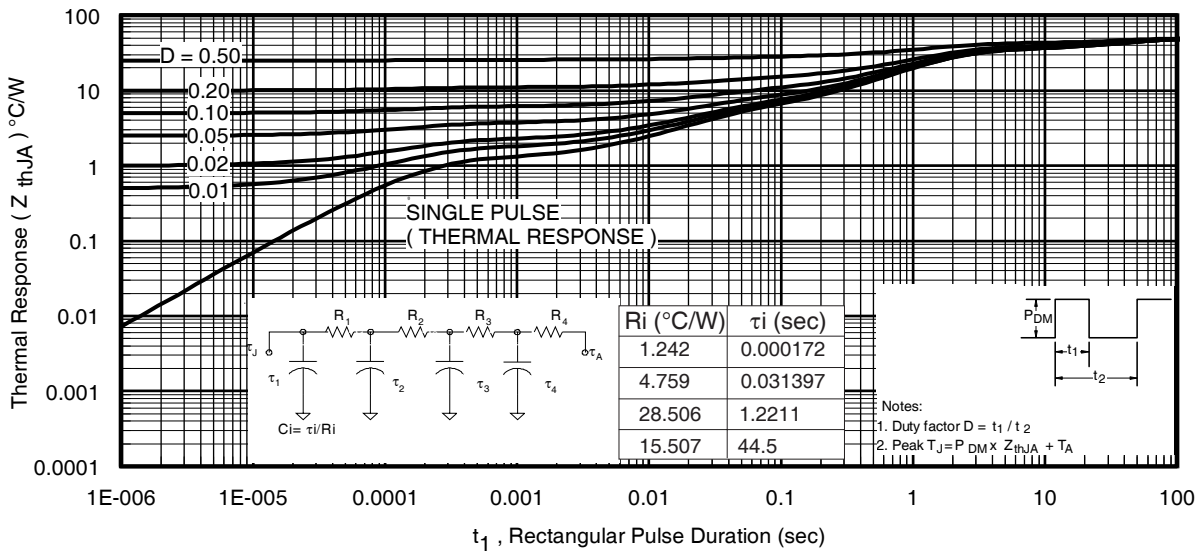


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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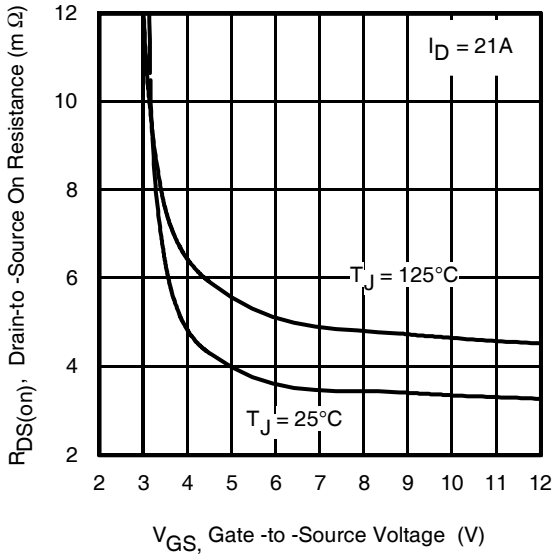


Fig 12. On-Resistance vs. Gate Voltage

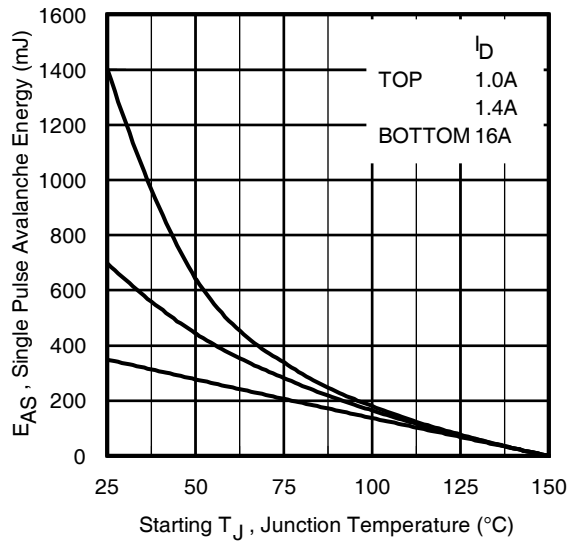


Fig 13. Maximum Avalanche Energy vs. Drain Current



Fig 14. Unclamped Inductive Test Circuit and Waveform



Fig 15. Gate Charge Test Circuit



Fig 16. Gate Charge Waveform

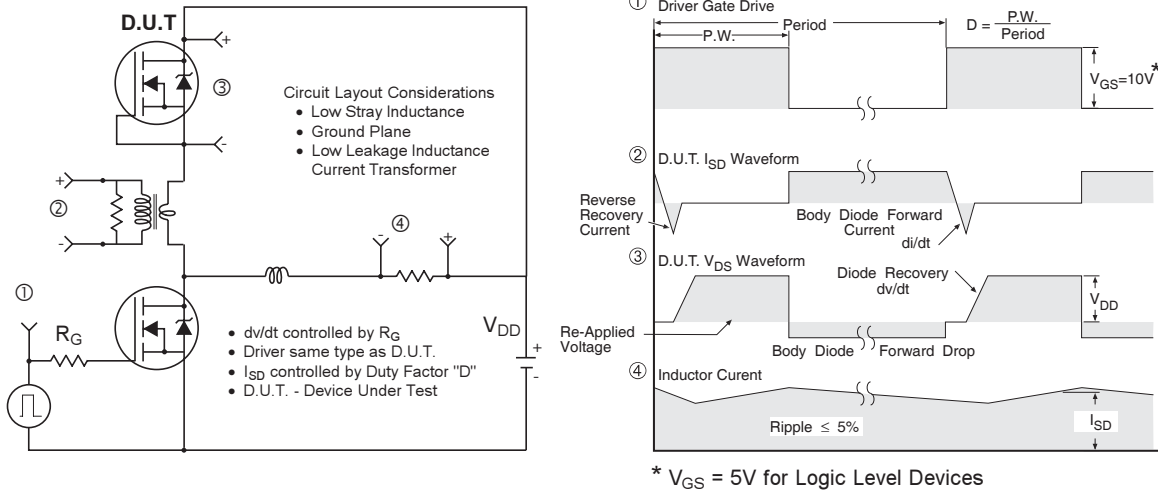


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

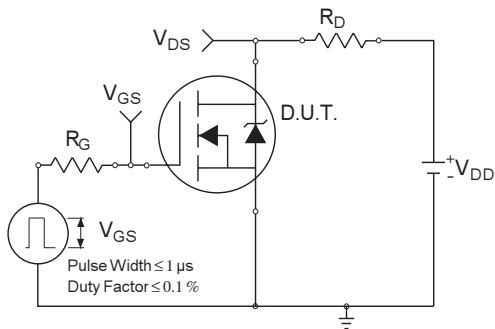


Fig 18a. Switching Time Test Circuit

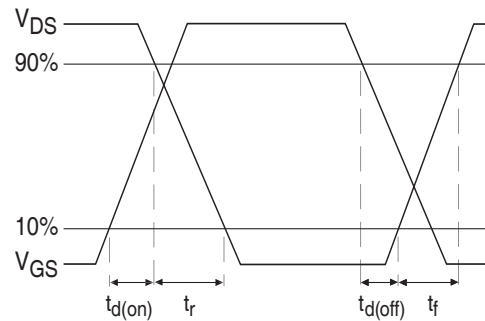


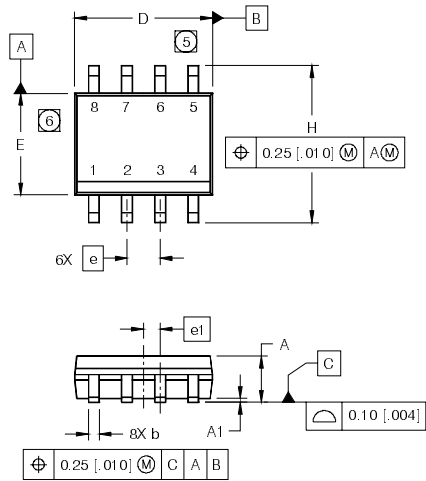
Fig 18b. Switching Time Waveforms

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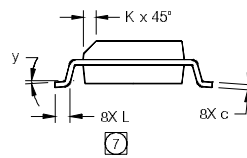
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SO-8 Package Outline (MOSFET & Fetky)

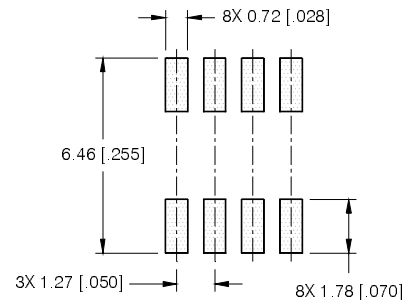
Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



FOOTPRINT

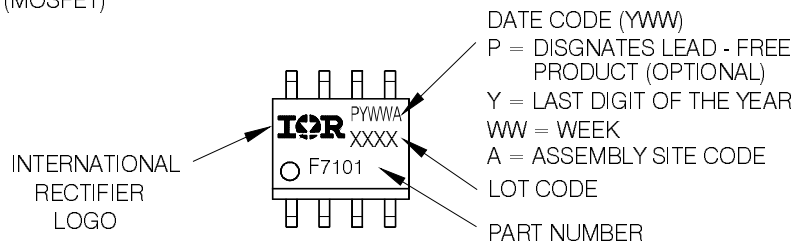


NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

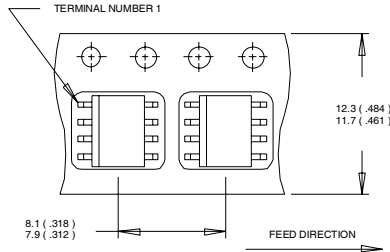
SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

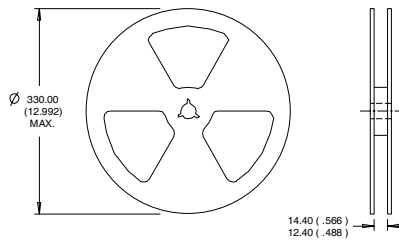


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

SO-8 Tape and Reel Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 2.7\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 16\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.
- ⑤ R_{θ} is measured at T_J of approximately 90°C .

Revision History

Date	Comment
6/4/2009	Maximum $R_{ds(on)}$ at $V_{gs} = 10\text{V}$ changed from $3.7\text{m}\Omega$ to $3.3\text{m}\Omega$. All other parameters are unchanged.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

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 Qualification Standards can be found on IR's Web site.

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