ALPHA & OMEGA SEMICONDUCTOR

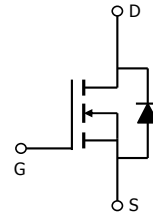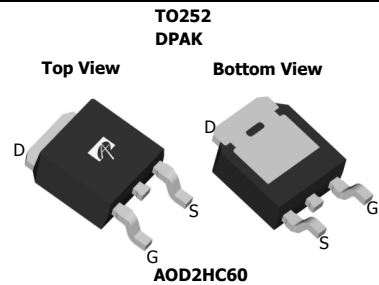# AOD2HC60
600V,2.5A N-Channel MOSFET

General Description

The AOD2HC60 is fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability this part can be adopted quickly into new and existing offline power supply designs.

Product Summary

V_{DS} @ $T_{j,max}$	700
I_{DM}	14A
$R_{DS(ON),max}$	< 2Ω
$Q_{g,typ}$	7.6nC
E_{oss} @ 400V	1.6µC

100% UIS Tested!
100% R_g Tested!

Green Product

TO252 DPAK

Top View

Bottom View

AOD2HC60

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current[B]	T_C=25℃	I_D	2.5	A
	T_C=100℃		2	
Pulsed Drain Current [C]		I_{DM}	14	
Avalanche Current [C]		I_{AR}	7.5	A
Repetitive avalanche energy [C]		E_{AR}	28	mJ
Single pulsed avalanche energy [H]		E_{AS}	132	mJ
MOSFET dv/dt ruggedness		dv/dt	100	V/ns
Peak diode recovery dv/dt			20	
Power Dissipation [B]	T_C=25℃	P_D	74	W
	Derate above 25°C		0.6	W/ °C
Junction and Storage Temperature Range		T_J, T_{STG}	-50 to 150	℃
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		T_L	300	℃

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient [A,G]	$R_{\theta JA}$	45	55	℃/W
Maximum Case-to-sink [A]	$R_{\theta CS}$	-	0.5	℃/W
Maximum Junction-to-Case[D,F]	$R_{\theta JC}$	1.3	1.7	℃/W

Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V, T$_J$=25°C	600			V
		I$_D$=250µA, V$_{GS}$=0V, T$_J$=150°C		700		
BV$_{DSS}$ /ΔTJ	Zero Gate Voltage Drain Current	ID=250µA, VGS=0V		0.59		V/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=600V, V$_{GS}$=0V			1	µA
		V$_{DS}$=480V, T$_J$=125°C			10	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±30V			±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=5V, I$_D$=250µA	3	4	5	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=0.8A		1.65	2	Ω
g$_{FS}$	Forward Transconductance	V$_{DS}$=40V, I$_D$=1.25A		2.3		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V		0.78	1	V
I$_S$	Maximum Body-Diode Continuous Current				2.5	A
I$_{SM}$	Maximum Body-Diode Pulsed Current				14	A
DYNAMIC PARAMETERS						
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz		466		pF
C$_{oss}$	Output Capacitance			23		pF
C$_{o(er)}$	Effective output capacitance, energy related [I]	V$_{GS}$=0V, V$_{DS}$=0 to 480V, f=1MHz		19		pF
C$_{o(tr)}$	Effective output capacitance, time related [J]			31		pF
C$_{rss}$	Reverse Transfer Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz		1.3		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz		6.3		Ω
SWITCHING PARAMETERS						
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=480V, I$_D$=2.5A		7.6	10	nC
Q$_{gs}$	Gate Source Charge			3.1		nC
Q$_{gd}$	Gate Drain Charge			1.4		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=300V, I$_D$=2.5A, R$_G$=25Ω		18		ns
t$_r$	Turn-On Rise Time			14		ns
t$_{D(off)}$	Turn-Off DelayTime			27		ns
t$_f$	Turn-Off Fall Time			17		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=2.5A,dI/dt=100A/µs,V$_{DS}$=100V		183		ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=2.5A,dI/dt=100A/µs,V$_{DS}$=100V		2.1		µC

A. The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25°C.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150°C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150°C.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150°C.

G.These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25°C.

H. L=60mH, I$_{AS}$=2.1A, V$_{DD}$=150V, R$_G$=10Ω, Starting T$_J$=25°C

I. C$_{o(er)}$ is a fixed capacitance that gives the same stored energy as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

J. C$_{o(tr)}$ is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

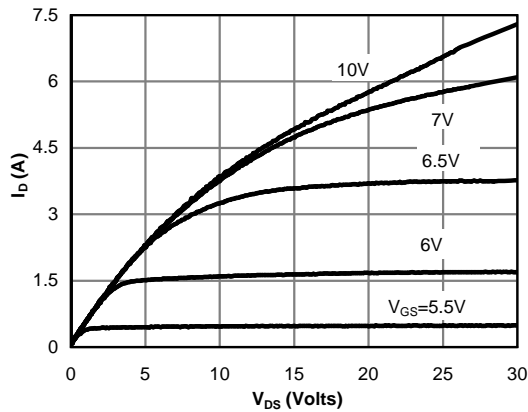## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

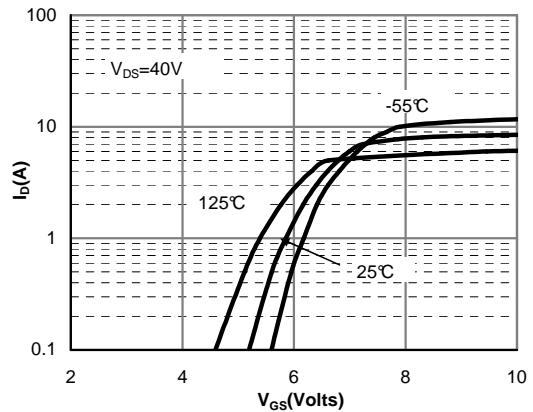Fig 1: On-Region Characteristics

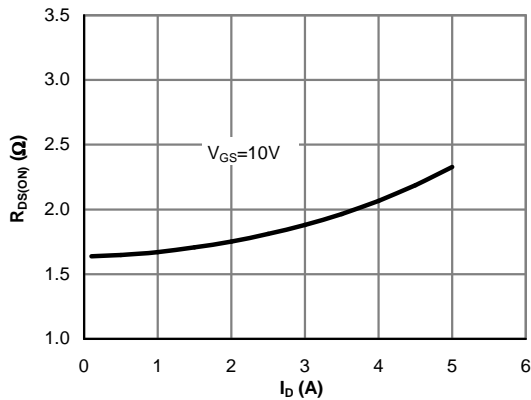Figure 2: Transfer Characteristics

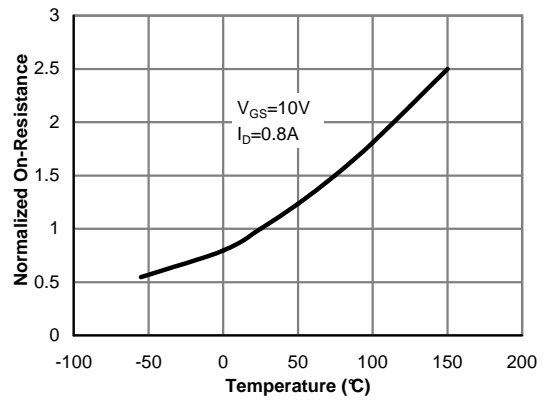Figure 3: On-Resistance vs. Drain Current and Gate Voltage
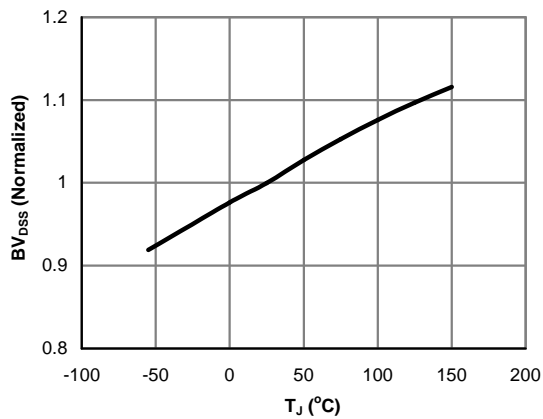

Figure 4: On-Resistance vs. Junction Temperature

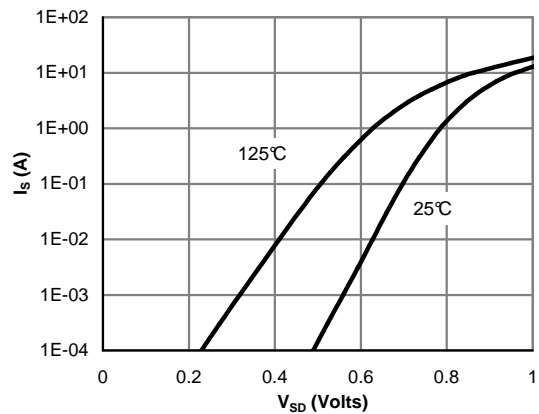Figure 5: Break Down vs. Junction Temperature

Figure 6: Body-Diode Characteristics

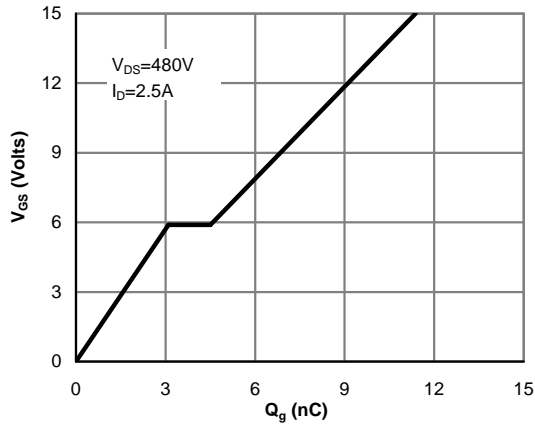**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

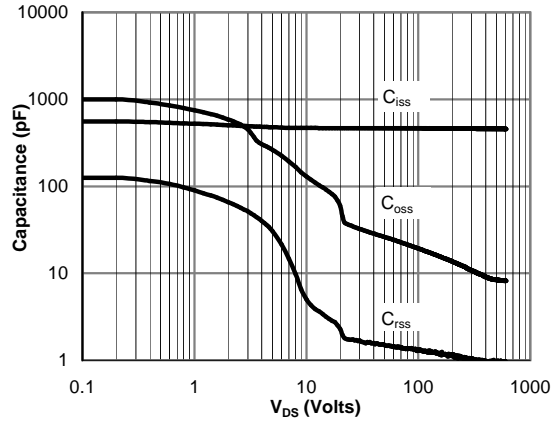
Figure 7: Gate-Charge Characteristics
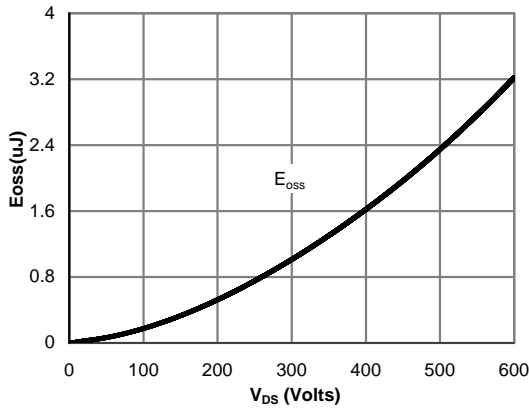

Figure 8: Capacitance Characteristics

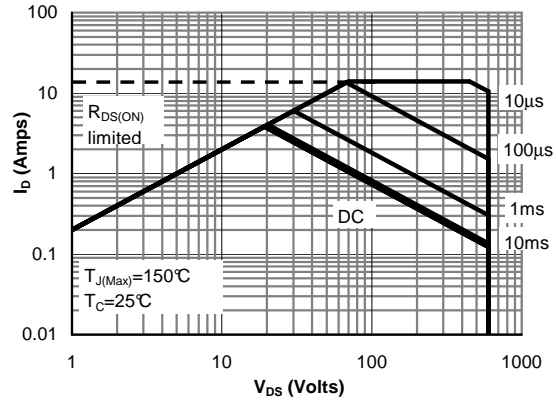Figure 9: Coss stored Energy

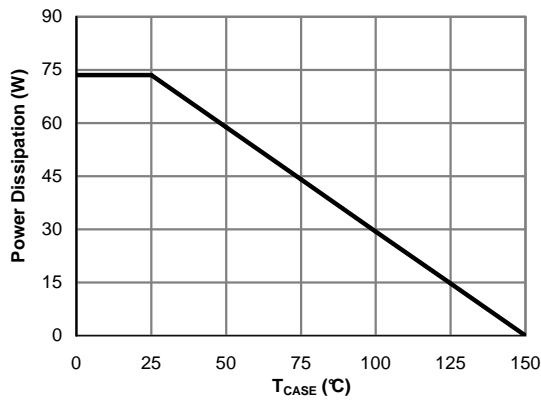Figure 10: Maximum Forward Biased Safe Operating Area (Note F)
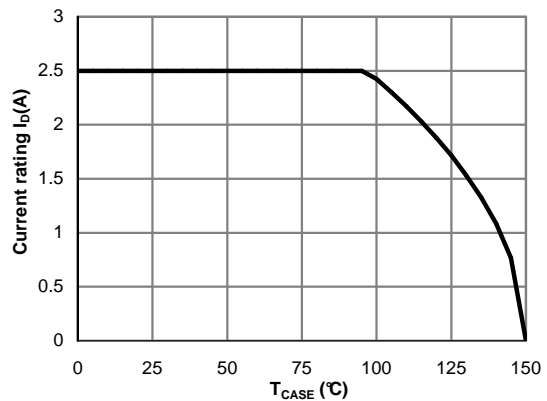

Figure 11: Power De-rating (Note B)

Figure 12: Current De-rating (Note B)
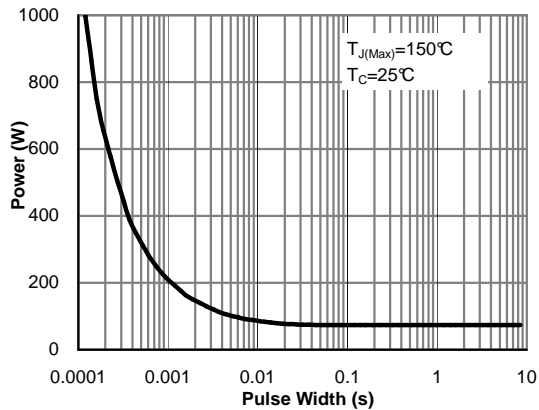
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

$T_{J(Max)}=150°C$
$T_C=25°C$

Figure 13: Single Pulse Power Rating Junction-to-Case (Note F)

$T_{J(Max)}=150°C$
$T_A=25°C$
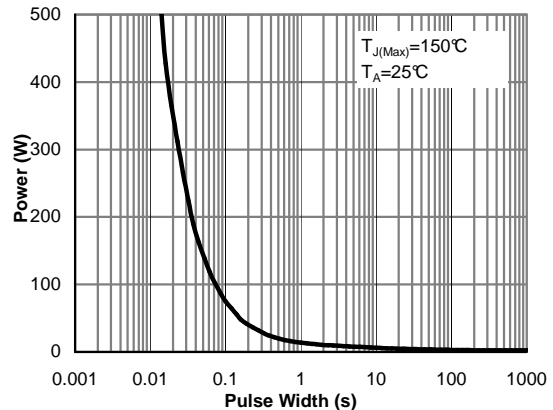
Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

$D=T_{on}/T$
$T_{J,PK}=T_C+P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$
$R_{\theta JC}=1.7°C/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse
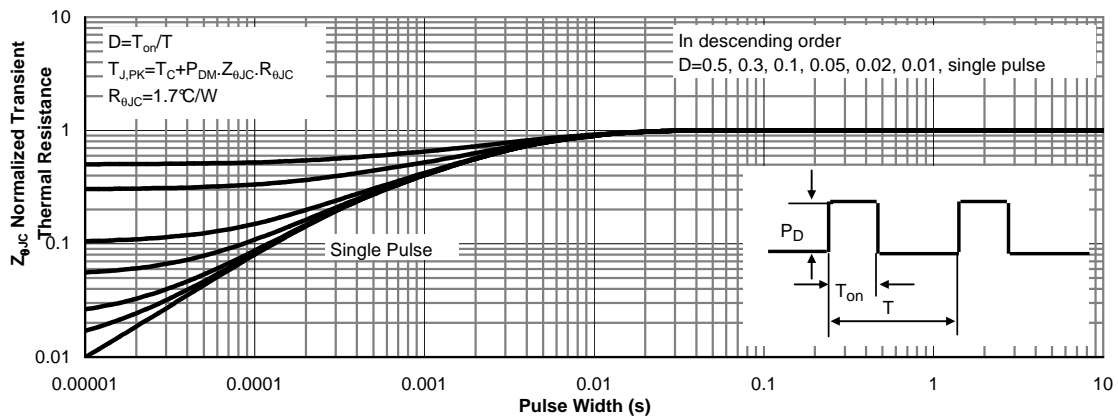
Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

$D=T_{on}/T$
$T_{J,PK}=T_A+P_{DM} \cdot Z_{\theta JA} \cdot R_{\theta JA}$
$R_{\theta JA}=55°C/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse
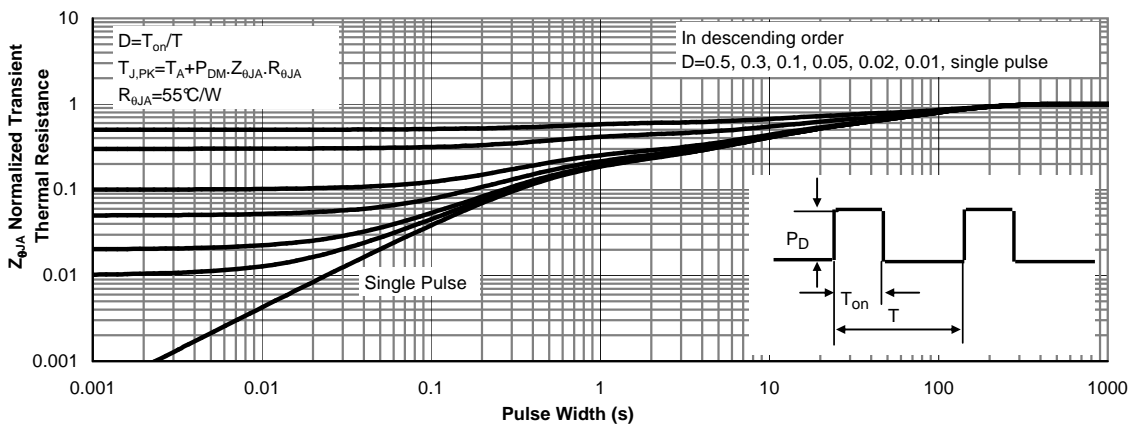
Single Pulse
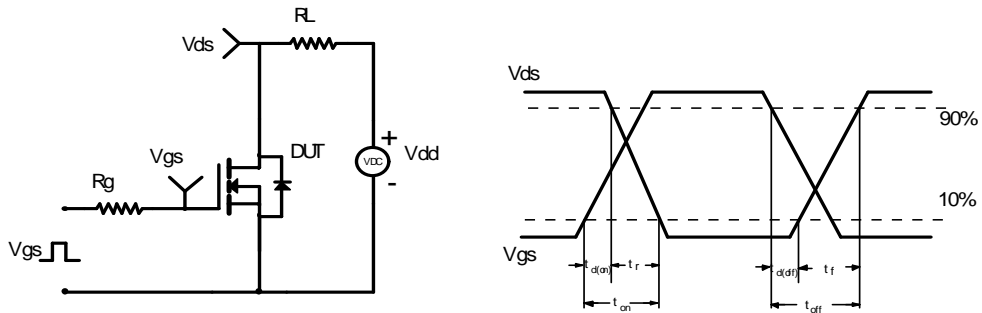
Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

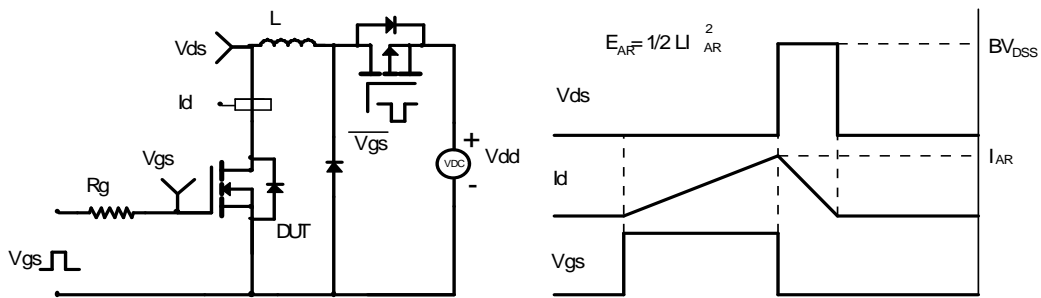## Gate Charge Test Circuit & Waveform

$$E_{AR} = 1/2 \, LI^2_{AR}$$

Vgs

10V

Qg

Qgs

Qgd

Charge
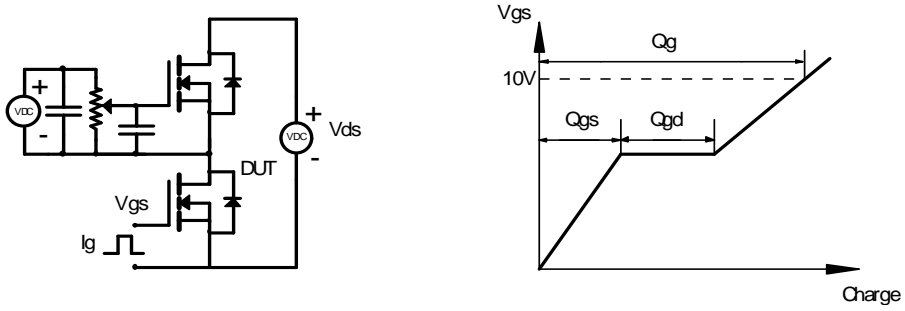
Resistive Switching Test Circuit & Waveforms

Vds

RL

Vgs

Rg

DUT

Vdd

Vds

Vgs

90%

10%

$t_{d(on)}$ t_r

t_{on}

$t_{d(off)}$ t_f

t_{off}

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Vds

L

Id

Vgs

Rg

$\overline{Vgs}$

DUT

Vdd

$E_{AR} = 1/2 \, LI^2_{AR}$

Vds

Id

Vgs

BV_{DSS}

I_{AR}

Diode Recovery Test Circuit & Waveforms

Vds +

Vds -

DUT

Isd

L

Vgs

Ig

Vdd

$Q_{rr} = - \int I \, dt$

Vgs

Isd

I_F

dI/dt

t_{rr}

I_{RM}

Vds

Vdd