SLA7050M/7051M/7052M

October 2005

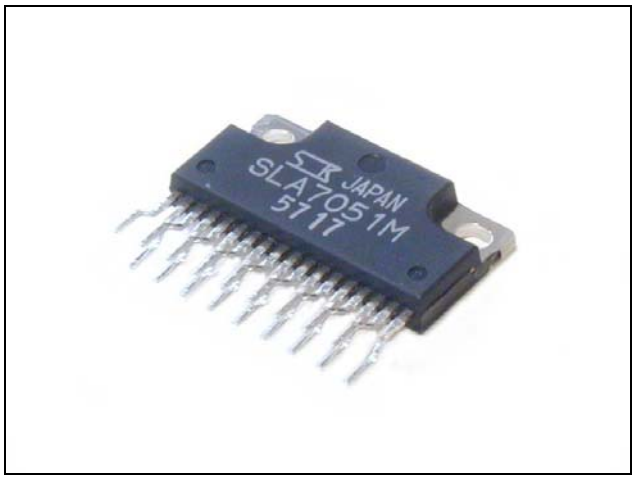
■General Description

Combining low-power CMOS logic with high-current, high-voltage power FET outputs, the Series SLA705xM translator/driver provides complete control and drive for a two-phase unipolar stepper motor with internal fixed off time, pulse-width modulation (PWM) control of the output current in a power multi-chip module (PMCM™).

The CMOS logic section provides the sequencing logic, direction, full/half-step control, synchronous/asynchronous PWM operation, and a "sleep" function. The minimum CLOCK input is an ideal fit for applications where a complex µP is unavailable or overburdened. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure a proper input-logic high. For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. The NMOS outputs are capable of sinking up to 1,2 or 3 A and withstanding 46 V in the off state. Ground-clamp and flyback diodes provide protection against inductive transients. Special power-up sequencing is not required.

Full-step (2 phase) and half-step operation are externally selectable. Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This sequence mode offers an improved torquespeed product, greater detent torque, and is less susceptable to motor resonance. Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD D-DA), providing an eight-step sequence.

■Package----SLA18Pin



■Applications

- ●PPC
- ●Printer
- ●OA Equipment

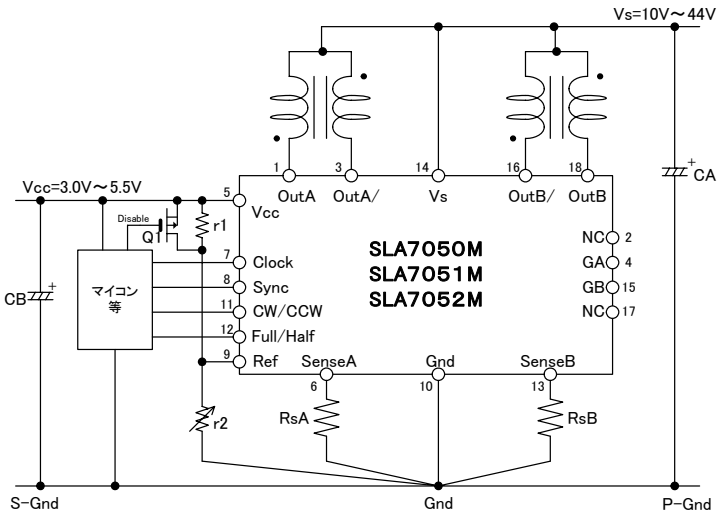
■Features

- ●To 3A Output Rating
- ●Internal Sequencer for Full or Half-Step Operation
- ●PWM Constant-Current Motor Drive
- ●Cost-Effective, Multi-Chip Solution
- ●100 V, Avalanche-Rated NMOS
- ●Low rDS(on) NMOS Outputs (300 milli-ohms typical)
- ●Advanced, Improved Body Diodes
- ●Half-Step and Full-Step Unipolar Drive
- ●Inputs Compatible with 3.3 V or 5 V Control Signals
- ●Sleep Mode
- ●Internal Clamp Diodes

■Key Specifications

- ●Motor Supply Voltage (VM)：44V max
- ●Load Supply Voltage (Vs)：10V～44V
- ●Logic Supply Voltage (Vcc)：3V～5.5V
- ●Output Current (Io)：1A(SLA7050M)
  2A(SLA7051M)
  3A(SLA7052M)
- ●Output Maximum Voltage (V_{DSS})：100V min

Typical Connection



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Scope

The present specifications shall apply to Sanken 2 Phase Stepper Motor Driver IC,SLA705xM Series.
The present specifications shall apply to SLA 705xM Series which is performed RoHS instructions.
Lead part solder：Pb free　Inner solder：Lead content ＞85%

Outline

Type	Hybrid integrated circuit
Structure	Plastic molded (transfer mold)
Applications	To drive a 2 phase stepper motor. (Full or Half Step. PWM Current Control.)

Absolute maximum ratings

Characteristic	Symbol	Ratings	Unit	Remarks
Motor Supply Voltage	V_M	46	V	
Load Supply Voltage	V_S	46	V	
Logic Supply Voltage	Vcc	7	V	
Output Current	Io	1.0	A	SLA7050M
		2.0		SLA7051M
		3.0		SLA7052M
Logic Input Voltage	V_{IN}	−0.3～Vcc+0.3	V	
REF Input Voltage	V_{REF}	−0.3～Vcc+0.3	V	
Sense Voltage	V_{Rs}	−2～2	V	Tw<1μS doesn't contain it.
Total Device Dissipation	P_D	4	W	at Ta=25℃
		20	W	at Tc=25℃
Junction Temperature	Tj	150	℃	
Operating Temperature Range	Ta	−20～85	℃	
Storage Temperature Range	Tstg	−30～150	℃	

Electrical characteristics

Recommendable Operating Range

Characteristic	Symbol	Ratings		Unit	Remarks
		MIN	MAX		
Motor Supply Voltage	V_M		44	V	
Load Supply Voltage	V_S	10	44	V	
Logic Supply Voltage	Vcc	3.0	5.5	V	Please adjust the Vcc surge voltage to 0.5V or less.
REF Input Voltage	V_{REF}	0.1	1.0	V	The control current accuracy decreases in 0.1V or less.
Package Temperature	Tc		100	℃	10Pin temperature (at No Fin)

Electrical Characteristic (Ta=25℃,Vs=24V,Vcc=5V Unless Otherwise Noted)

Characteristic	Symbol	Limits			Unit	Test Condition
		MIN	TYP	MAX		
Load Supply Current	I_S			15	mA	Regularity
	I_{SS}			100	μA	at SLEEP operates
Logic Supply Current	Icc			3	mA	
Output Maximum Voltage	V_{DSS}	100			V	V_S=44V I_{DSS}=1mA
FET On-State Resistance	$R_{DS(on)}$		0.3	0.5	Ω	I_D=1A
FET Diode Forward Voltage	V_{SD}		0.8	1.1	V	I_{SD}=1A
Maximum Clock Frequency	Fclock			100	kHz	
Logic Input Voltage	V_{IL}			Vcc×0.25	V	
	V_{IH}	Vcc×0.75			V	
Logic Input Current	I_{IL}		±1		μA	
	I_{IH}		±1		μA	
REF Input Voltage	V_{REF}	0		1.5	V	Stationary current control
	V_{REFS}	2.0		Vcc	V	Output OFF(Sleep)
REF Input Current	I_{REF}		±10		μA	
Sense Voltage	VRs		V_{REF}		V	

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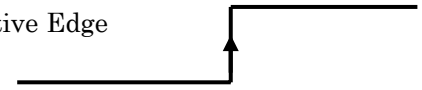
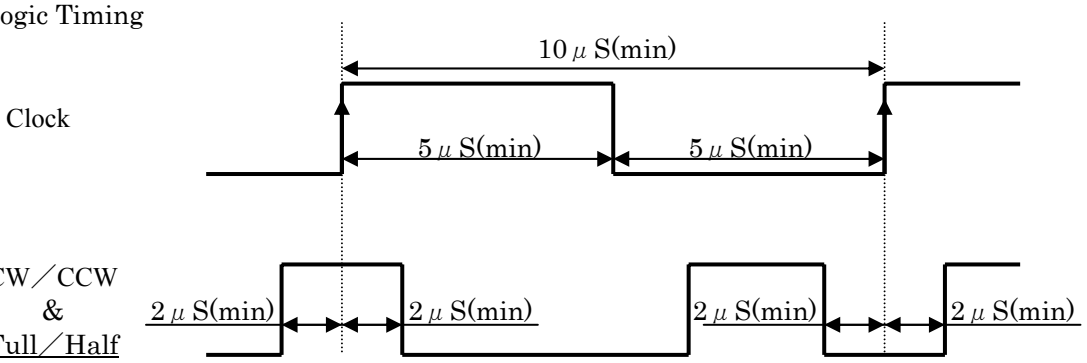
Electrical Characteristic (Ta=25℃,Vs=24V,Vcc=5V Unless Otherwise Noted)

Characteristic	Symbol	Limits			Unit	Test Condition
		MIN	TYP	MAX		
PWM OFF Time	T_{OFF}		12		μS	
PWM Minimum ON Time	$T_{ON(min)}$		5		μS	
Sleep-Enable return time	T_{SE}	100			μS	V_{REF} : 2.0→1.5V Io : 1.5A
Switching Time	T_{ONC}		2.5		μS	Clock→Out
	T_{OFFC}		2.0		μS	Clock→Out

Truth table

Pin Function	Low level	High level
CW／CCW	Forward(CW)	Reverse(CCW)
Full／Half	Full Step	Half Step
REF	Enable	Output disable(Sleep)
Sync	Non synchronous PWM	Synchronous PWM
Clock	Positive Edge 	

Input Logic Timing



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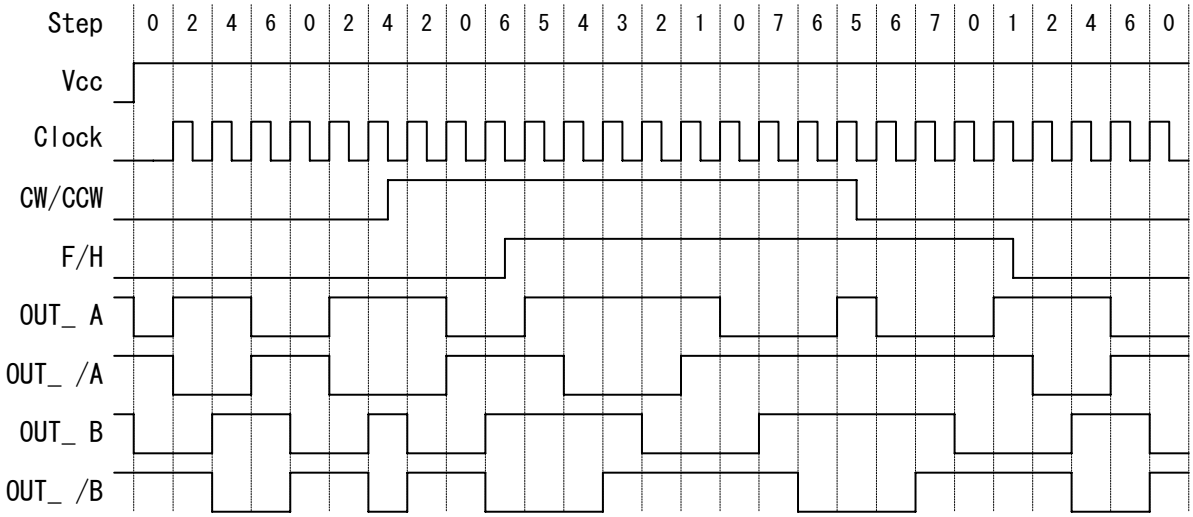
Timing chart



・This timing chart is a voltage mark.
・PWM signal for current control is not superimposed on this timing chart.

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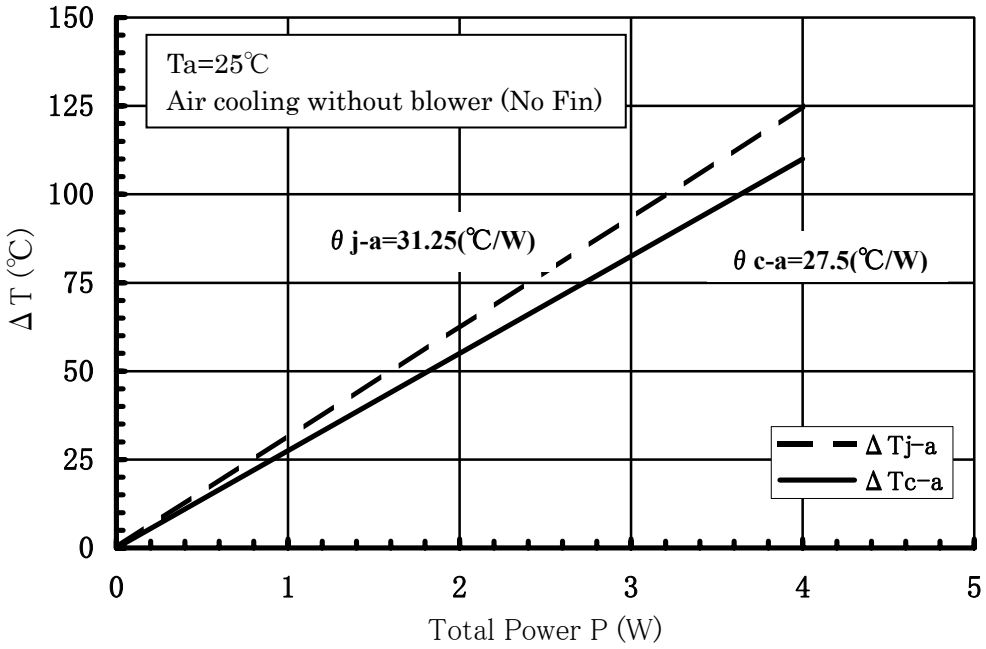
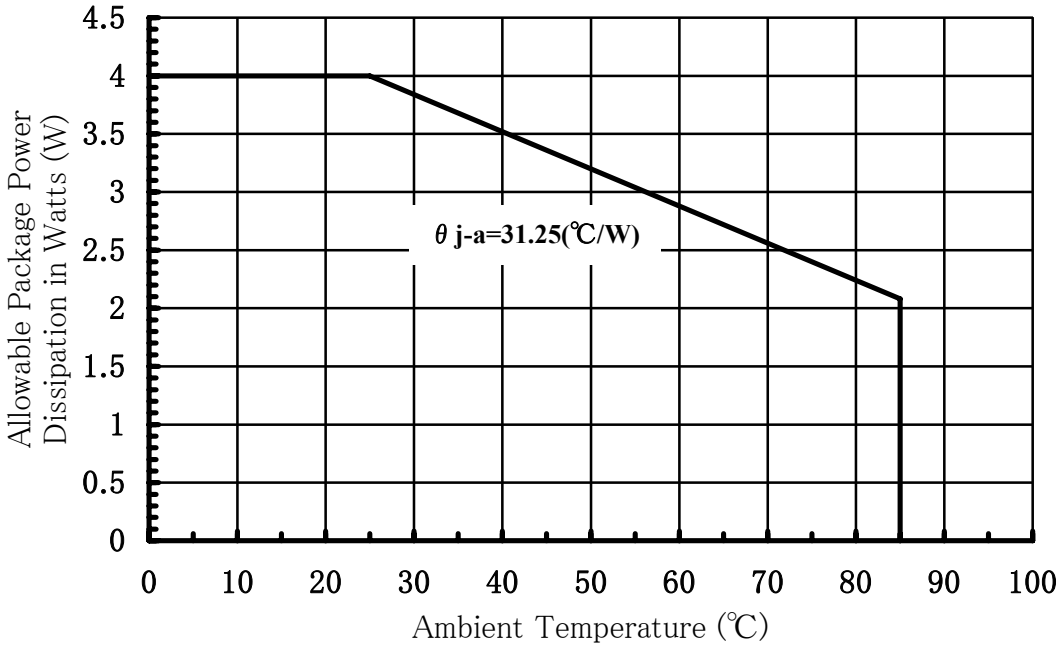
Heat design data

Total Power－ΔT indegc



※The temperature of the case is 10pin.

Ta - P



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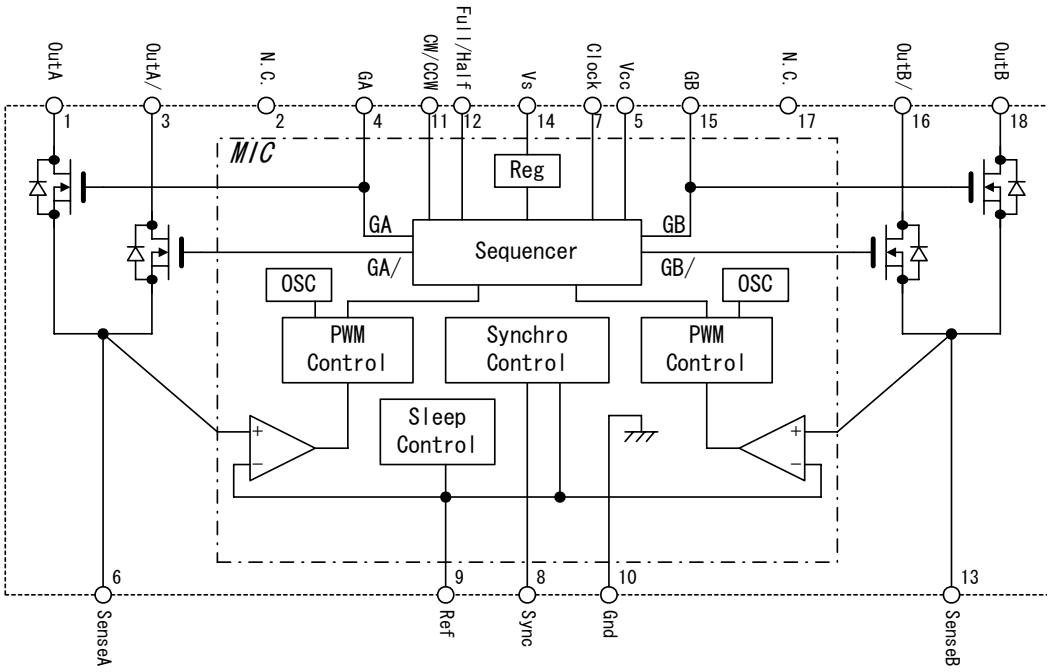
Block diagram (Connection diagram)



Pin arrangement ,Functional table

Pin Number	Symbol	Function
1	OutA	Phase A Output
2	N.C.	No Contact
3	OutA/	Phase A/ Output
4	GA※	Phase A Gate
5	Vcc	Logic supply
6	SenseA	Phase A current sense
7	Clock	Step clock
8	Sync	Synchronous PWM control
9	Ref	Current reference & Output disable
10	GND	GND
11	CW/CCW	Forward reverse control
12	Full/Half	Full step half step control
13	SenseB	Phase B current sense
14	Vs	Load supply
15	GB※	Phase B Gate
16	OutB/	Phase B/ Output
17	N.C.	No Contact
18	OutB	Phase B Output

※The gating signal of MOS FET outputs, and use 4pin and 15pin by the unwiring, please.

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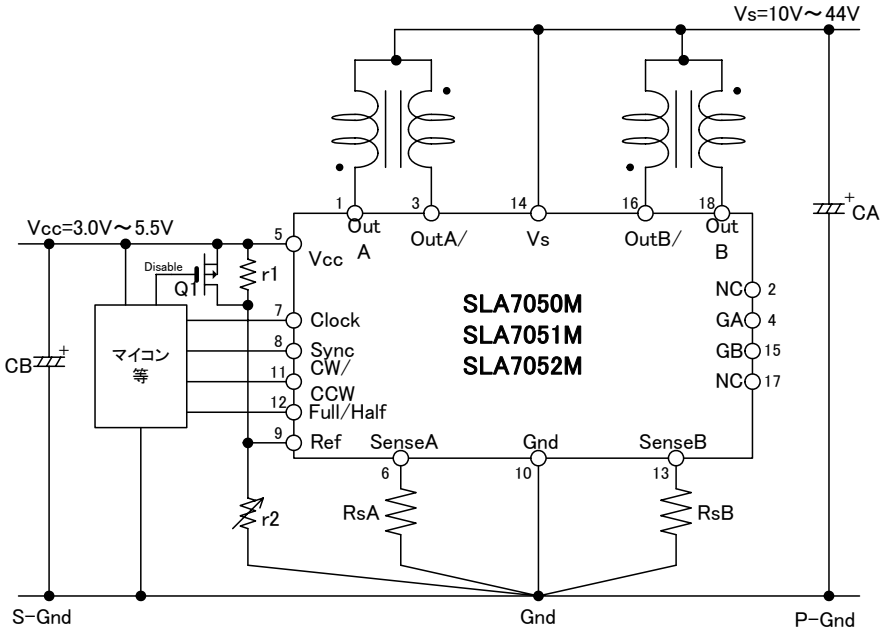
Example application circuit



Reference constant

Rs=0.1～2Ω(Loss attention　P≒Io²×Rs)	CA=100μF／50V
R1=10kΩ	CB=10μF／10V
R2=5.1kΩ(VR)	Q1：

☆Be careful of especially the noise on Vcc line.
If the noise on Vcc line exceeds 0.5V, a product may incorrect-operate.

☆When you do not use Logic inputs (CW/CCW and F/H, Sync), please be sure to connect with Vcc or GND.

☆To minimize the effect of system ground I･R drops on the logic and reference input signals, Ground pin should have a low-impedance return to system groud.

☆2pin,4pin,15pin and 17pin are No Contact.

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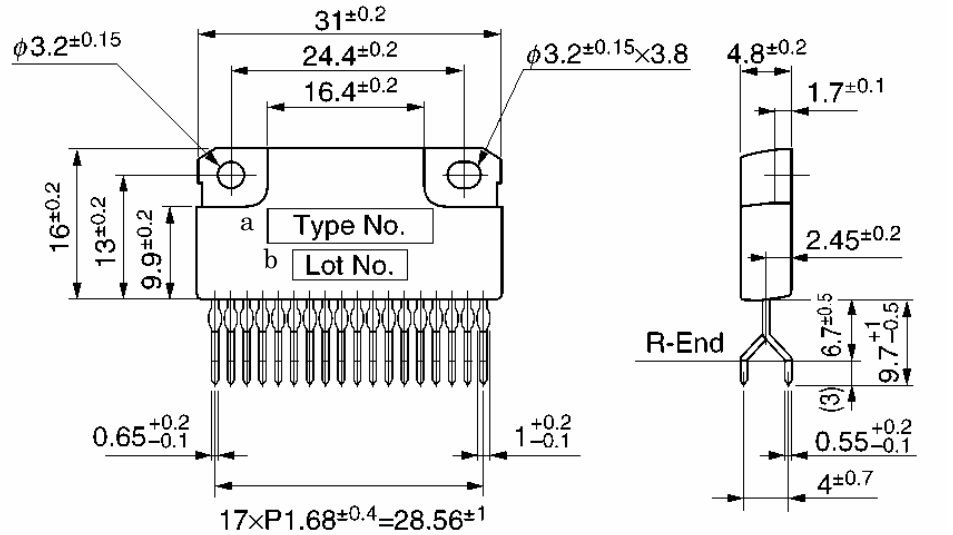
Package information s

Package type and physical dimensions



Dimensions in mm

a. Type Number SLA705xM

b. Lot Number

1st letter The last digit of year

2nd letter Month

1～9 月 : Arabic Numerals

10 月 : O

11 月 : N

12 月 : D

(1 to 9 for Jan. to Sept. O for Oct. N for Nov. D for Dec.)

3rd &4th letter day

01～31 : Arabic Numerals

Appearance

The body shall be clean and shall not bear any stain, rust or flaw.

Marking

The type number and lot number shall be clearly marked in white.

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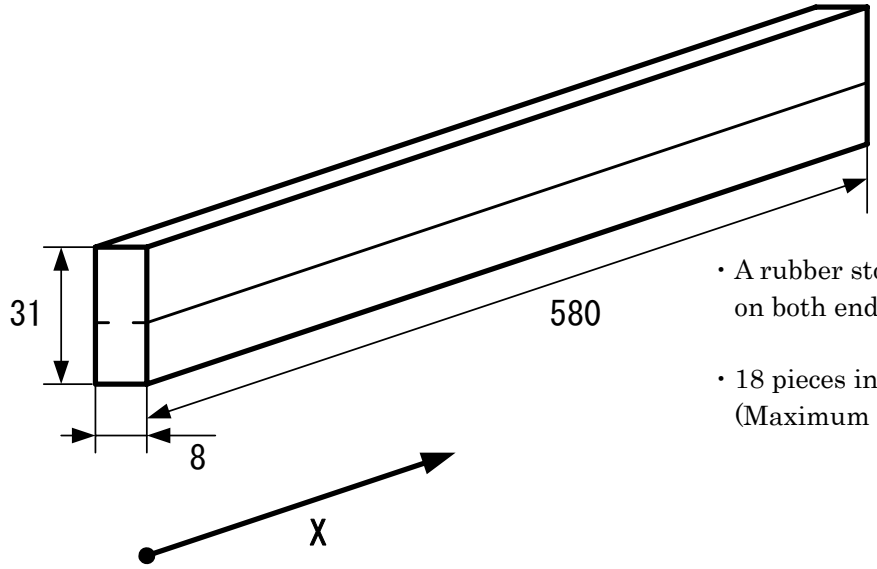
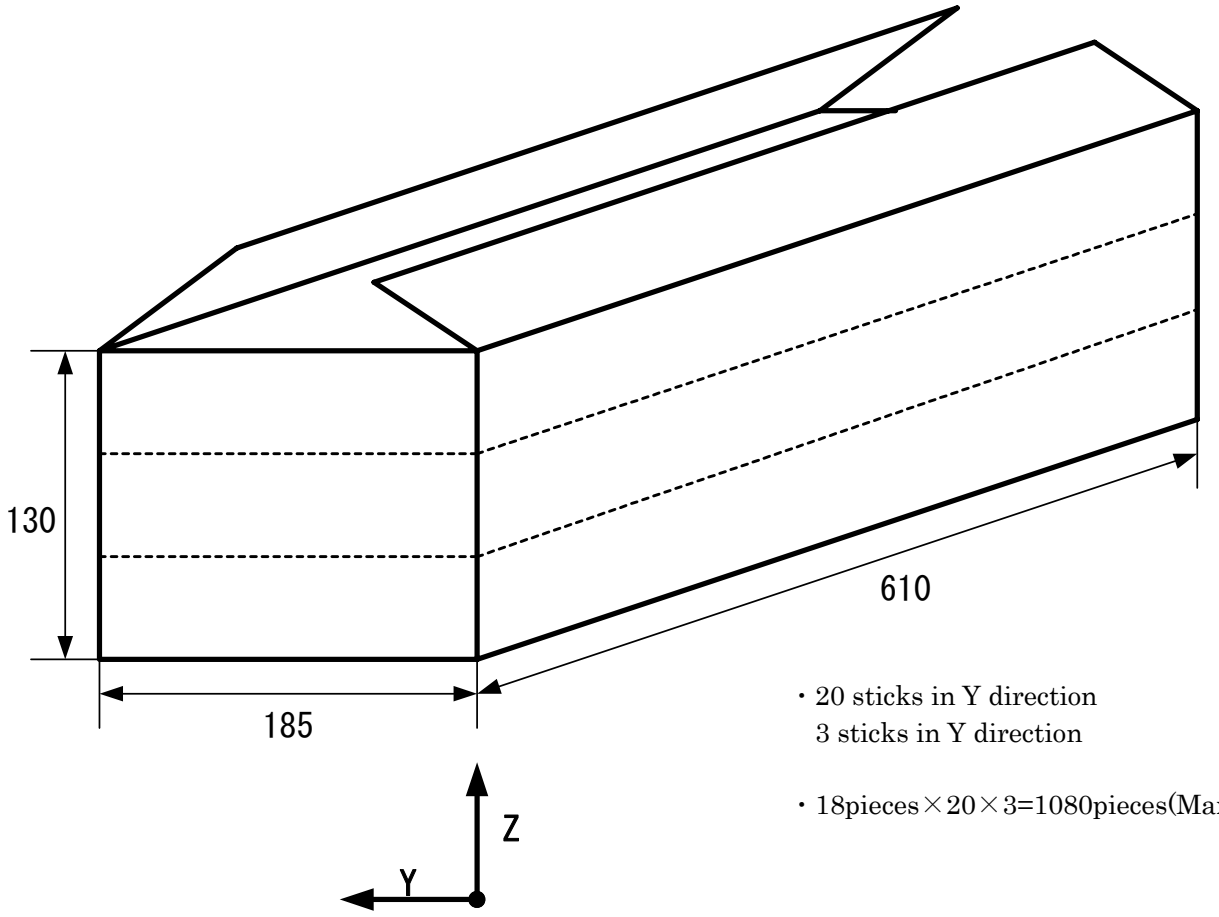
Packing specifications



・A rubber stopper is provided on both ends of the stick.

・18 pieces in X direction
(Maximum 18 pieces in one stick)



・20 sticks in Y direction
3 sticks in Y direction

・18pieces×20×3=1080pieces(Max.)

Dimensions in mm

Cautions and warnings

The calculation of control current

SLA705xM Series control current Io is calculated as follow.

Io＝VREF／Rs

REF Voltage range is 0.1V～1.0V

※When the REF<0.1V, the accuracy of control current is reduce.

Moreover, if REF voltage is set up more than 2.0V, all outputs will be in OFF state.

Installation to a heat sink

1)Recommended Clamping Torque (to External Heat sink)　0.490～0.822N・m

2)Recommended Silicone

G746	{SHIN-ETSU CHEMICAL}
YG6260	{GE TOSHIBA SILICONES}
SC102	{DOW CORNING TORAY SILICONE}

Notice

This driver has C-MOS inputs. Please notice as following contents.

・When static electricity is a problem, care should be taken to properly control the room humidity. This is particularly true in the winter when static electricity is most troublesome.

・Care should be taken with device leads and with assembly sequencing to avoid applying static charges to IC leads. PC board pins should be shorted together to keep them at the same potential to avoid this kind of trouble.

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