LAN7500/LAN7500i

Hi-Speed USB 2.0 to 10/100/1000 Ethernet Controller

PRODUCT FEATURES

Data Brief

Highlights

- Single Chip Hi-Speed USB 2.0 to 10/100/1000 Ethernet Controller
- 10/100/1000 Ethernet MAC with Full-Duplex Support
- 10/100/1000 Ethernet PHY with HP Auto-MDIX
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated USB 2.0 Hi-Speed PHY
- Implements Reduced Power Operating Modes
- Supports EEPROM-less Operation for Reduced BOM
- NetDetach provides automatic USB attach/detach when Ethernet cable is connected/removed

Target Applications

- Embedded Systems / CE Devices
- Set-Top Boxes / PVR's
- Networked Printers
- USB Port Replicators
- Standalone USB to Ethernet Dongles
- Test Instrumentation / Industrial

Key Benefits

- USB Device Controller
  - Fully compliant with USB Specification Revision 2.0
  - Supports HS (480 Mbps) and FS (12 Mbps) modes
  - Four endpoints supported
  - Supports vendor specific commands
  - Integrated USB 2.0 PHY
  - Remote wakeup supported
- High-Performance 10/100/1000 Ethernet Controller
  - Fully compliant with IEEE802.3/802.3u/802.3ab
  - Integrated Ethernet MAC and PHY
  - 10BASE-T, 100BASE-TX, and 1000BASE-T support
  - Full- and half-duplex capability (only full-duplex operation at 1000Mbps)
  - Full-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - 9 KB jumbo frame support
  - Automatic payload padding and pad removal
  - Loop-back modes
  - Supports checksum offloads (IPv4, IPv6, TCP, UDP)
  - Supports Microsoft NDIS 6.2 large send offload
  - Supports IEEE 802.1q VLAN tagging
    - Ability to add and strip IEEE 802.1q VLAN tags
    - VLAN tag based packet filtering (all 4096 VIDs)
  - Flexible address filtering modes
    - 33 exact matches (unicast or multicast)
    - 512-bit hash filter for multicast frames
    - Pass all multicast
    - Promiscuous unicast/multicast modes
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
    - Perfect DA frame, wakeup frame, magic packet, broadcast frame, IPv6 & IPv4 TCP SYN
    - 8 programmable 128-bit wakeup frame filters
  - ARP and NS offload
  - PME pin support
  - Integrated Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - HP Auto-MDIX support
    - Link status change wake-up detection
  - Support for 5 status LEDs
  - Supports various statistical counters
- Power and I/Os
  - Various low power modes
  - 12 GPIOs
  - Supports bus-powered and self-powered operation
  - Variable voltage I/O supply (2.5V/3.3V)
- Miscellaneous Features
  - EEPROM Controller
  - IEEE 1149.1 (JTAG) Boundary Scan
  - Requires single 25 MHz crystal
- Software
  - Windows XP/ Vista / Windows 7 Driver
  - Linux Driver
  - Win CE Driver
  - MAC OS Driver
  - EEPROM/Manufacturing Utility for Windows/DOS
  - PXE Support
  - DOS ODI Driver
- Packaging
  - 56-pin QFN (8x8 mm) lead-free RoHS compliant
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)

Order Numbers:

LAN7500-ABZJ for 56 pin, QFN lead-free RoHS compliant package (0 to +70°C temp range)

LAN7500i-ABZJ for 56 pin, QFN lead-free RoHS compliant package (-40 to +85°C temp range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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General Description

The LAN7500/LAN7500i is a high performance Hi-Speed USB 2.0 to 10/100/1000 Ethernet controller. With applications ranging from embedded systems, set-top boxes, and PVR's, to USB port replicators, USB to Ethernet dongles, and test instrumentation, the device is a high performance and cost competitive USB to Ethernet connectivity solution.

The LAN7500/LAN7500i contains an integrated 10/100/1000 Ethernet MAC and PHY, Filtering Engine, USB PHY, Hi-Speed USB 2.0 device controller, TAP controller, EEPROM controller, and a FIFO controller with a total of 32 KB of internal packet buffering.

The internal USB 2.0 device controller and USB PHY are compliant with the USB 2.0 Hi-Speed standard. The device implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3, IEEE 802.3u, IEEE 802.3ab standards. ARP and NS offload is also supported.

Multiple power management features are provided, including various low power modes and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. These wake events can be programmed to initiate a USB remote wakeup.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

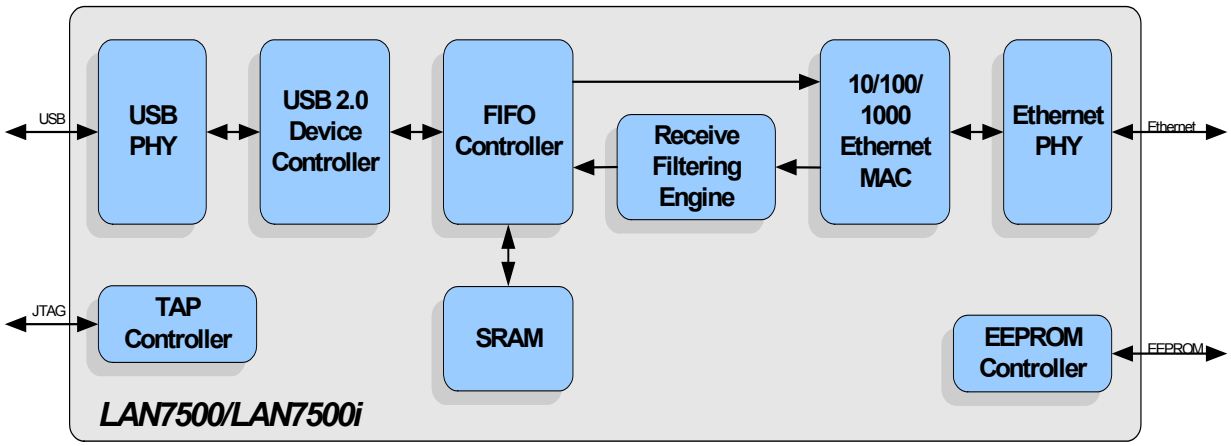


Figure 1 LAN7500/LAN7500i System Diagram

56-QFN Package Outline

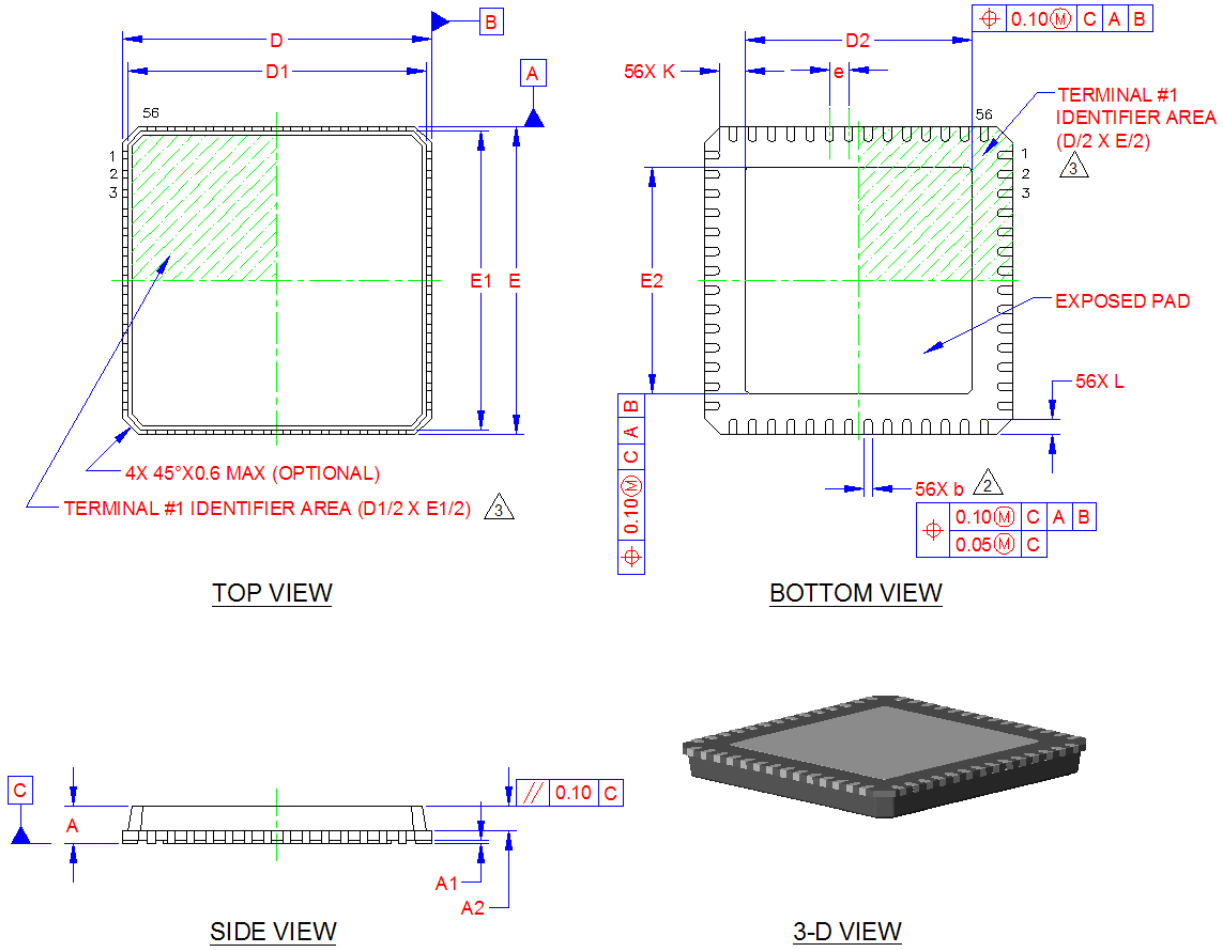


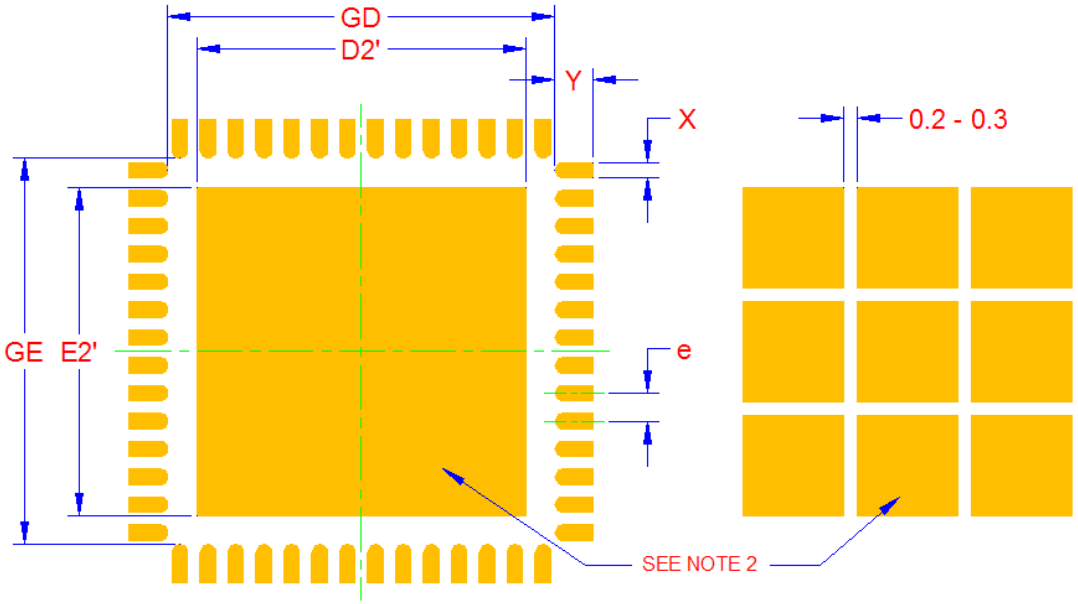
Figure 2 56-QFN Package

Table 1 56-QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.70	0.85	1.00	Overall Package Height
A1	0.00	0.02	0.05	Standoff
A2	-	-	0.90	Mold Cap Thickness
D/E	7.85	8.00	8.15	X/Y Body Size
D1/E1	7.55	7.75	7.95	X/Y Mold Cap Size
D2/E2	5.80	5.90	6.00	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
K	0.55	-	-	Center Pad to Pin Clearance
e		0.50 BSC		Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.93	-	7.05
D2'/E2'	-	5.90	5.90
X	-	0.28	0.28
Y	-	0.69	0.69
e		0.50	

NOTES:
1. THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

PCB LAND PATTERN

Figure 3 56-QFN Recommended PCB Land Pattern