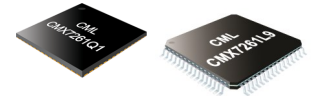


## CMX7261

### Full Duplex Multi-transcoder IC

G723.1 · G729A · G.711 · Linear PCM · CVSD



Small 64-pin VQFN/LQF Packages

#### Introduction

Digital voice coding has become an important operation in today's digital communications world.

There is a large range of digital voice based systems deployed, each using one of the available digital voice coding algorithms, which are generally interoperable. Therefore, a transcoding operation becomes a necessity where systems need to interconnect.

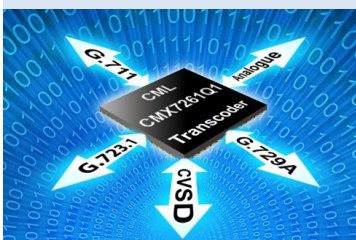
The CMX7261 Multi-transcoder IC is the solution by providing multiple digital voice coding algorithms within a single device. This provides the necessary coding and transcoding functions with the flexibility to enable further digital voice coding algorithms to be added in the future.

#### Features

- Self-contained functionality
- Embedded audio code
- No external DSP required
- Full duplex and half-duplex operation
- Coding and transcoding
- Supporting popular voice coding algorithms: Linear PCM, G.711, G.729A, G.723.1 and CVSD
- Voice activity detection
- Selectable input output source
  - Analogue
  - C-BUS to host
  - External PCM codec
- Auxiliary functions
  - GPIO
  - Analogue input/output gain adjustment
  - Analogue input/output multiplexer

#### Applications

- Digital radio systems
- Personal area network voice links
- Privacy-type digital voice links
- Wireless PABX
- VoIP systems
- Software Defined Radios (SDR)



#### Brief Description

The CMX7261 is a Multi-transcoder IC offering a range of popular voice codecs (digital voice coding algorithms) in a single chip.

Capable of both full-duplex and half-duplex operation, the CMX7261 combines a number of popular digital voice coding algorithms into a single IC. Built on *FirmASIC*® component technology opens up the potential of providing further voice coding algorithms and the possibility of customisation.

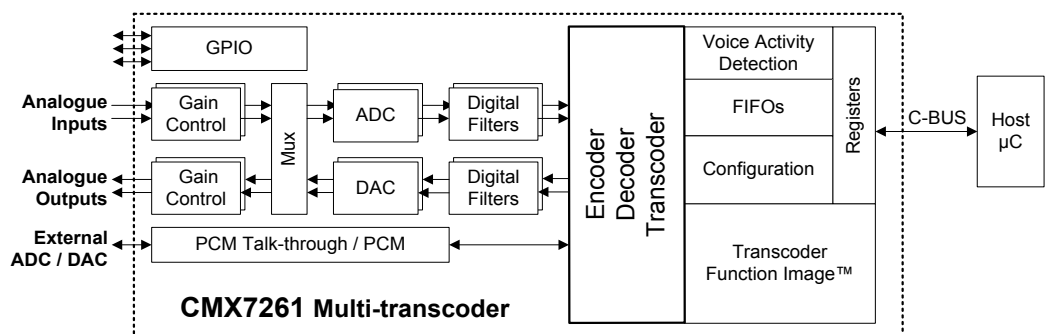
The CMX7261 is part of CML's Dura Talk™ digital voice processor range and presents a highly flexible solution to your digital voice coding and transcoding requirements.

Two Function Images™ are currently available. A Function Image™ (FI) being a data file that is uploaded during device initialisation and defines the device's function and feature set.

Function Image™	Encode, Decode and Transcode
7261FI-1.x	<p>Analogue, Linear PCM, G.711, G.729A, CVSD</p>
7261FI-2.x	<p>Analogue, Linear PCM, G.711, G.723.1</p>

In common with other *FirmASIC*® based products, the CMX7261 additionally offers a number of auxiliary features: configurable GPIO, programmable input and output digitally controlled attenuators, host C-BUS port and a separate master/slave PCM serial interface.

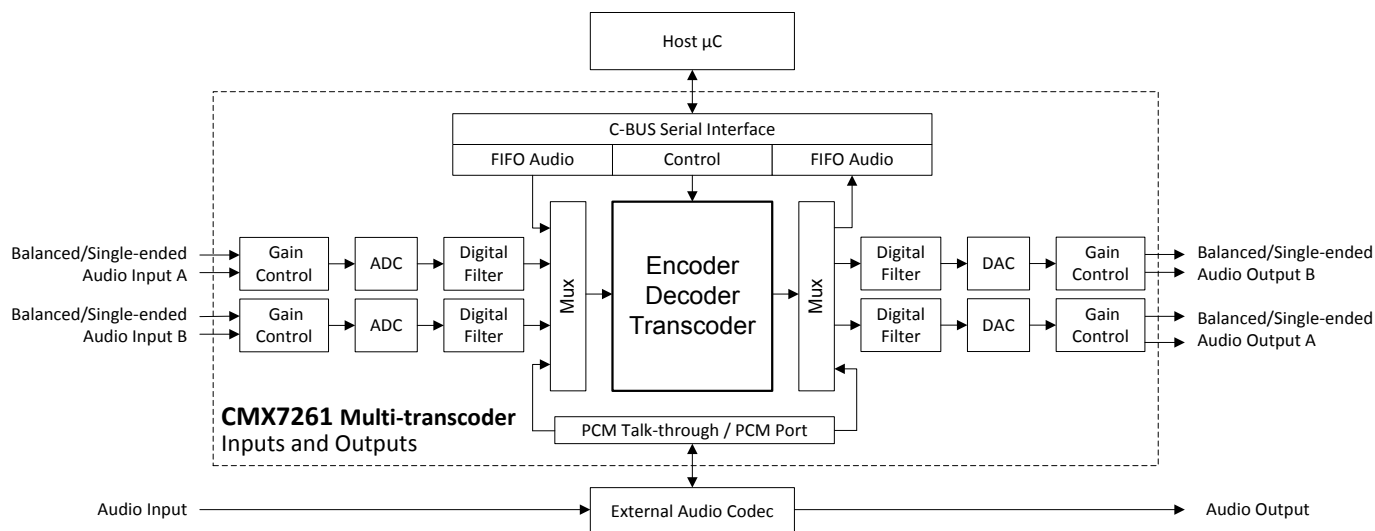
The CMX7261 operates from a 3.0 to 3.6 V supply, includes selectable powersaving modes and is available in small 64-pin VQFN/LQFP packages.



## Signal Interfacing

In half duplex mode the transcoder output can be sent to one, any two, or all of the possible output ports – C-BUS (for transfer to host controller), PCM (for transfer to external DAC) or analogue audio output.

In full duplex mode a single output must be selected. The input to the transcoder must come from one of the input ports – C-BUS (input data from the host controller), PCM (from the external ADC) or analogue audio input.



## Digital Voice Coding Algorithms

The following digital voice coding algorithms are supported via Function Image™ upload.

### Linear PCM

Speech is sampled with 16 bit words at 8ks/s providing a coded data rate of 64kbits/second.

#### G.711

The G.711 standard is an ITU recommendation for audio companding. The standard specifies coding of linear PCM speech at 8ks/s into logarithmic PCM speech at 8ks/s – a coded data rate of 64kbits/second. There are two variants:  $\mu$ -law is used primarily in North America – codes 14-bit linear PCM to 8-bit logarithmic PCM and A-law is used in the rest of the world – codes 13-bit linear PCM to 8-bit logarithmic PCM.

#### G.729A

The G.729 standard is an ITU recommendation for coding of speech signals at 8ks/s using conjugate-structure algebraic-code-excited linear prediction (CS-ACELP) into an 8kbits/s coded bitstream. G.729 annex A provides a reduced-complexity version at the basic coding rate of 8kbits/s whilst maintaining compatibility with G.729.

### CVSD

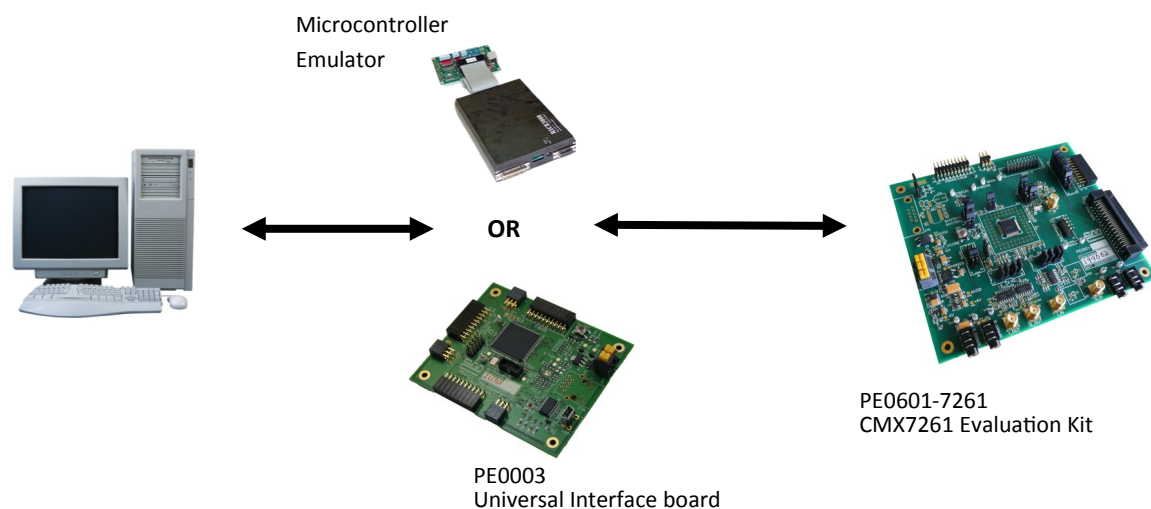
Continuously variable slope delta modulation (CVSD) is a voice coding technique using delta modulation with variable step size. CVSD encodes at 1 bit per sample, so that audio sampled at 16kHz is encoded at 16kbits/s. Similarly, audio sampled at 32kHz is encoded at 32kbits/sec.

#### G.723.1

The G.723.1 is an ITU recommendation for coding speech samples at 8ks/s with a 30ms frame size. This translates to 240 PCM samples per G.723.1 frame.

The vocoder produces a compressed bit stream at either 5.3kbits/s or 6.3kbits/s depending on the selected mode of operation. In addition, G.723.1 Annex A defines a discontinuous transmission (DTX) capability.

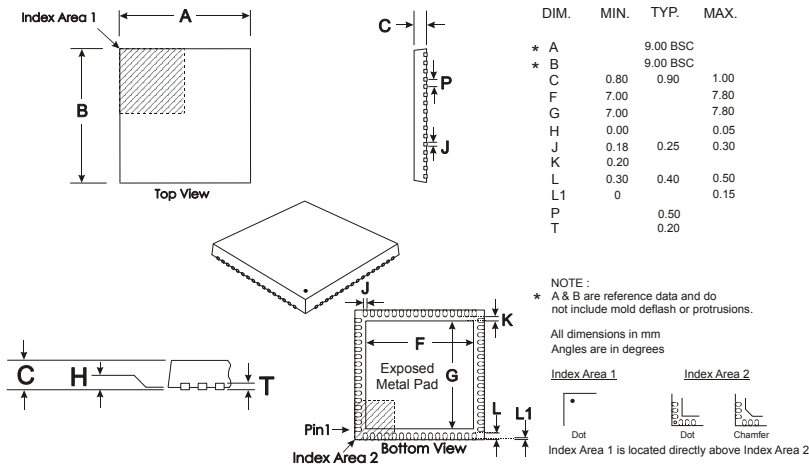
## Evaluation / Demonstration



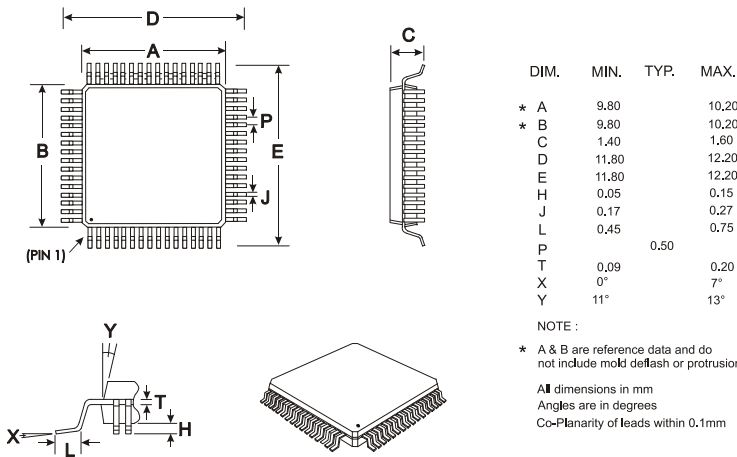
## CMX7261 Electrical Specification Summary

Operating Limits	Min	Typ	Max	Unit
Supply Voltage				
Digital Supply	3.0	3.3	3.6	V
Core Supply	1.7	1.8	1.9	V
Analogue Supply	3.0	3.3	3.6	V
Operating Temperature	-40	-	+85	°C
Xtal Frequency	4.0	-	12.288	MHz
External Clock Frequency	9.6	-	24.576	MHz
Current Consumption				
Idle Mode				
Digital Supply	-	670	-	µA
Analogue Supply	-	17	-	µA
Transcoding mode – DIDD				
G.723.1 Decoder 6.3 kbits/sec	-	10	-	mA
G.723.1 Decoder 5.3 kbits/sec	-	10	-	mA
G.723.1 Encoder 6.3 kbits/sec	-	24	-	mA
G.723.1 Encoder 5.3 kbits/sec	-	22	-	mA
G.711 A-law Encoder	-	4.7	-	mA
G.711 A-law Decoder	-	4.6	-	mA
G.729A Decoder	-	7.7	-	mA
G.729A Encoder	-	19.7	-	mA
CVSD Decoder	-	4.4	-	mA
CVSD Encoder	-	4.5	-	mA
Processing Delays				
G.723.1 6.3kbits/sec	-	75	-	ms
G.723.1 5.3kbits/sec	-	75	-	ms
G711 µ-Law	-	15	-	ms
G711 A-Law	-	15	-	ms
PCM	-	15	-	ms

## CMX7261 Package Options



64-pin VQFN Mechanical Outline (Q1)



64-pin LQFP Mechanical Outline (L9)

For detailed product information visit: [www.cmlmicro.com](http://www.cmlmicro.com) or search for: **CMX7261**



CML's proprietary FirmASIC® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. FirmASIC® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a FirmASIC® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. FirmASIC® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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