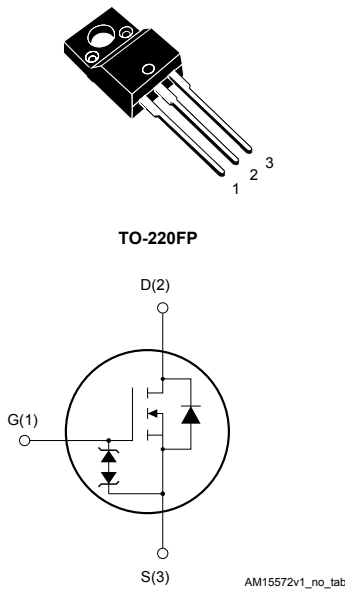


N-channel 600 V, 85 mΩ typ., 30 A MDmesh™ M6 Power MOSFET in a TO-220FP package



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STF36N60M6	600 V	99 mΩ	30 A

- Reduced switching losses
- Lower R_{DS(on)} per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R_{DS(on)} per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link

[STF36N60M6](#)

Device summary

Order code	STF36N60M6
Marking	36N60M6
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	30	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	19	A
$I_{DM}^{(2)}$	Drain current (pulsed)	102	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	40	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 30\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400$
- $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	750	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$		85	99	m Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1960	-	pF
C_{oss}	Output capacitance		-	93	-	pF
C_{riss}	Reverse transfer capacitance		-	6	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	332	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 30\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	44.3	-	nC
Q_{gs}	Gate-source charge		-	10.1	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 15\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	15.2	-	ns
t_r	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	50.2	-	ns
t_f	Fall time		-	7.3	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		30	A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		102	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 30\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	340		ns
Q_{rr}	Reverse recovery charge		-	5.3		μC
I_{RRM}	Reverse recovery current		-	31		A
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	430		ns
Q_{rr}	Reverse recovery charge		-	7.7		μC
I_{RRM}	Reverse recovery current		-	36		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

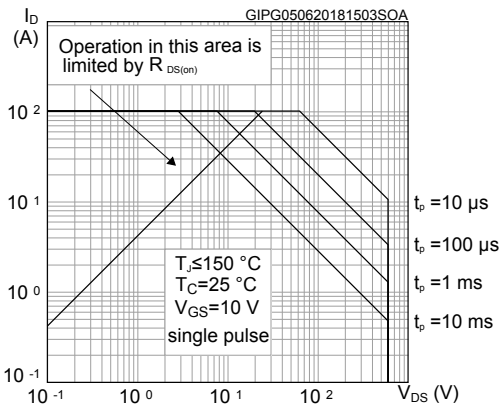


Figure 2. Thermal impedance

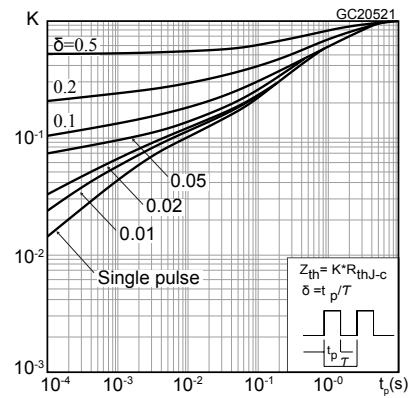


Figure 3. Output characteristics

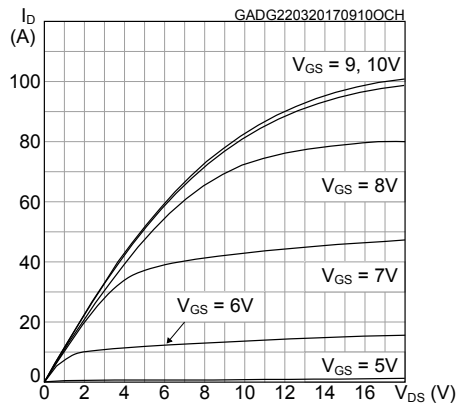


Figure 4. Transfer characteristics

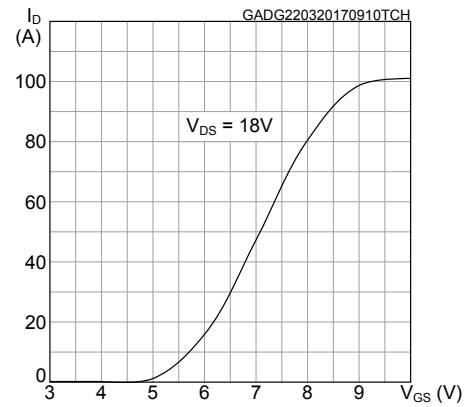


Figure 5. Gate charge vs gate-source voltage

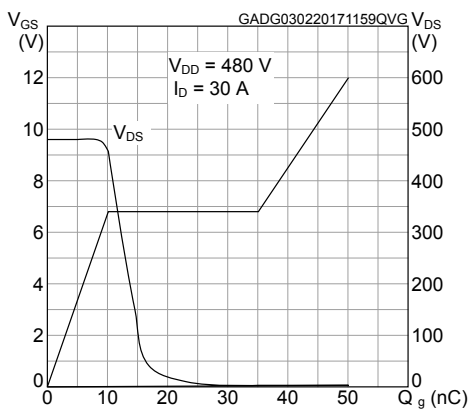


Figure 6. Static drain-source on-resistance

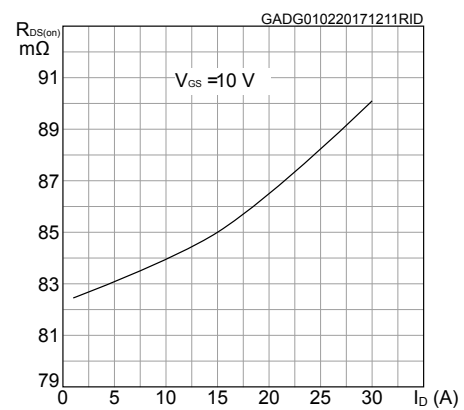


Figure 7. Capacitance variations

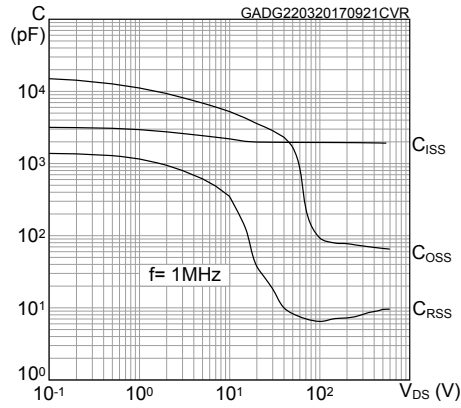


Figure 8. Normalized gate threshold voltage vs temperature

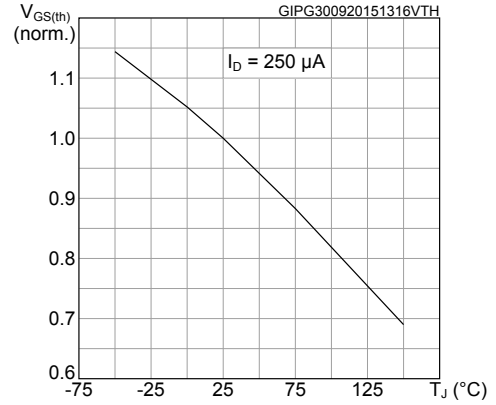


Figure 9. Normalized on-resistance vs temperature

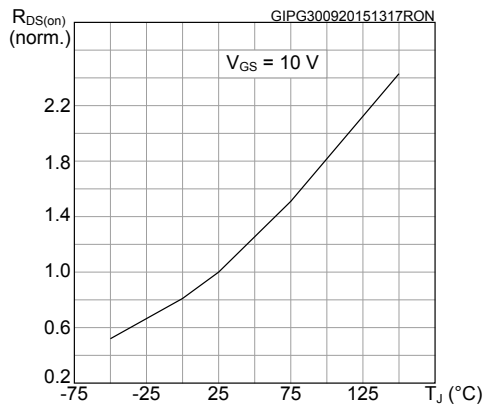


Figure 10. Normalized V_{(BR)DSS} vs temperature

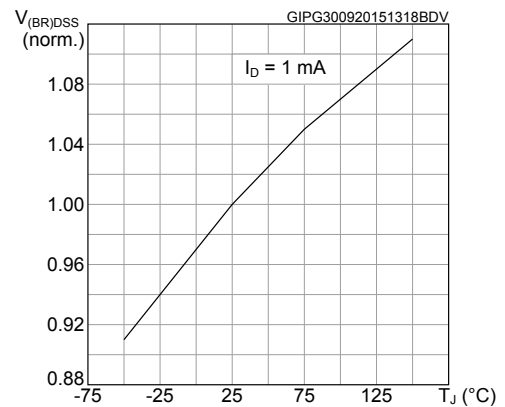


Figure 11. Output capacitance stored energy

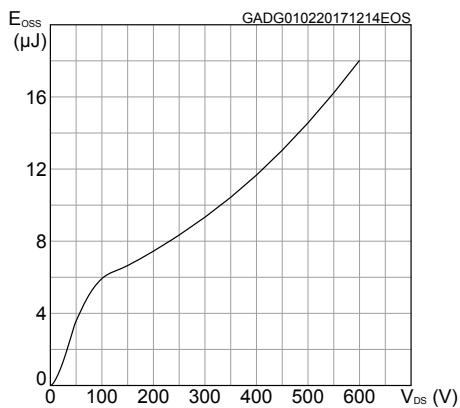
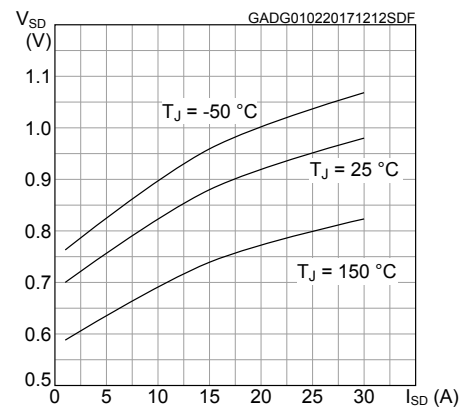


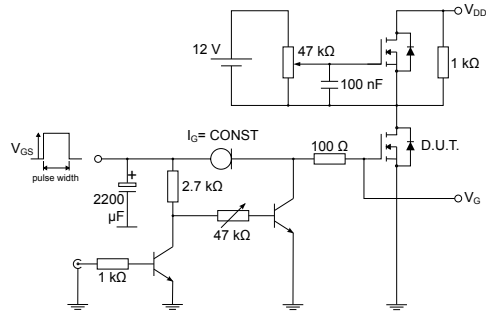
Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times


AM01468v1

Figure 14. Test circuit for gate charge behavior


AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times


AM01470v1

Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform

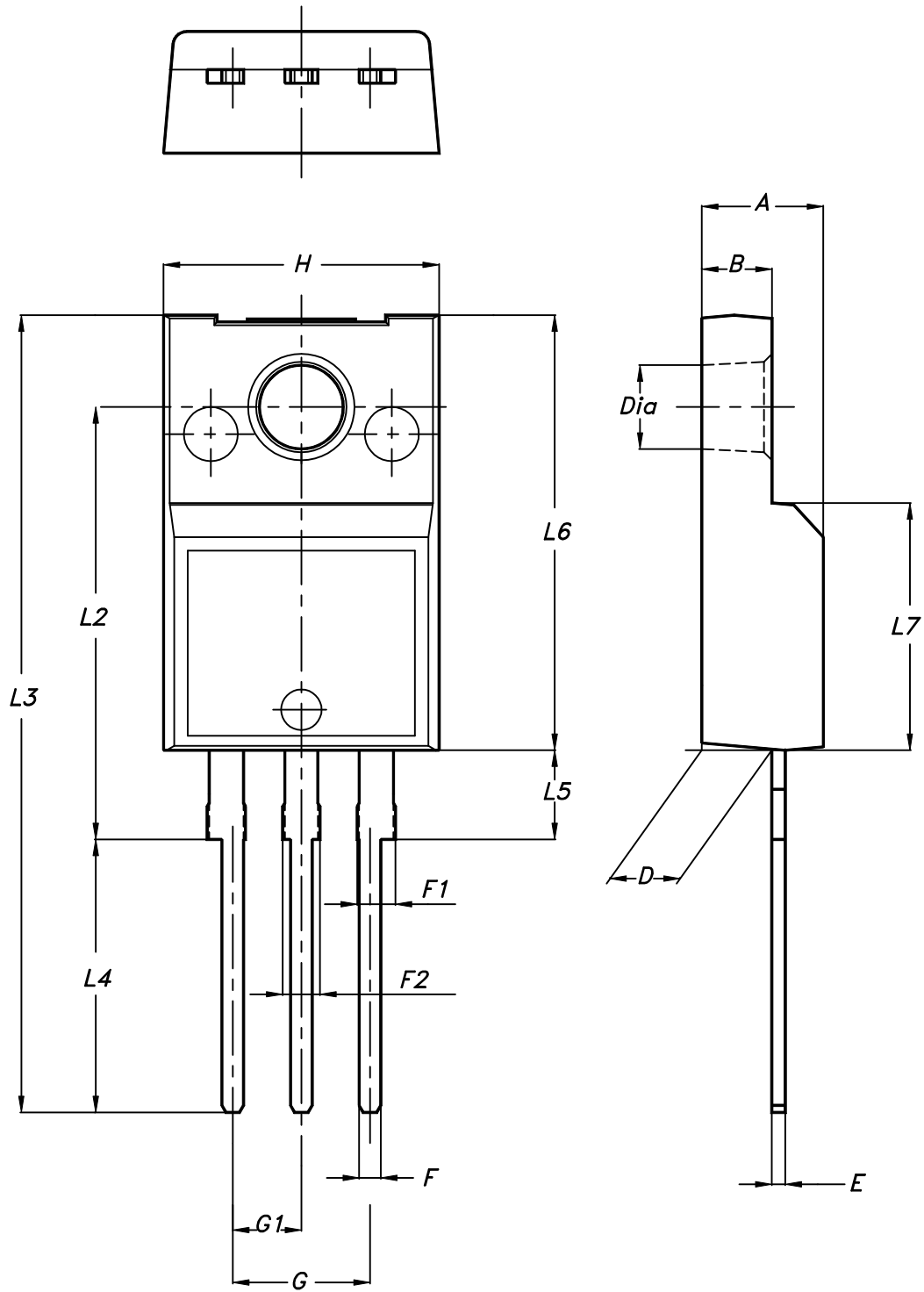

AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 19. TO-220FP package outline



7012510_Rev_12_B

Table 8. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Jul-2018	1	First release.

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