Single Chip 96-Port STS-1/STM-0 Cross-Connect

FEATURES

- Implements a 240G memory switch fabric with STS-1/AU-3 switching granularity.
- 96 ingress and 96 egress STS-48/STS-12 ports for a maximum of 4608 STS-1/AU-3 streams in a single device.
- Supports a single-stage, anycast switching capacity of 240G.

SWITCH PORT CONFIGURATION

- Each port can be individually configured for 2.488Gbit/s or 622Mbit/s operation. Ingress and egress links of a port can be individually configured.
- Optionally inserts AIS on ingress links that are out-of-frame.
- Supports unequipped overwrite, and path AIS overwrite on a per egress port and per egress grain basis.
- Implements the ESSI Frame layer

TOH PROCESSING AND TESTING

- Supports transport overhead processing of ports in groups of 24.
- TOH extract clock and data interface capable of extracting a set of TOH bytes per ingress port. Selection of the bytes to be extracted is user programmable on a per 24-port group basis.
- TOH insert clock and data interface capable of overwriting a set of TOH bytes per egress port. Selection of the bytes to overwrite is user programmable on a per 24-port group basis.

GLOBAL FRAME SYNCHRONIZATION

- Supports frame synchronization via a global frame pulse input signal.
- Provides software readable registers that report the difference between the arrival time of the J0 byte and the time the device frame reference expects to read the J0 byte from the ingress port FIFO on a per ingress port basis.

DELAY MANAGEMENT

- Provides a 108 byte FIFO for each ingress port to support 102 byte maximum skew among the input links (1312 ns for 622 Mbit/s links and 328 ns for 2.488 Gbit/s links).
- Provides 13 delay management (DM) blocks that can be allocated to a subset of devices ports (1 through 25) as either input delay management (DMI) or output delay management (DMO). Each DM block processes a STS-48 signal for an aggregate delay management capacity of 32.5 Gbit/s.
- Supports ganging of 4 DM blocks to form a delay management group (DMG) capable of processing a STS-192 signal.

- Each DM block allocated as DMI supports arbitrary frame alignment of an STS-48 ingress signal to the frame alignment of the synchronous switching core.
- Each DM block allocated as DMO supports alignment of a switch core output to a user defined frame alignment.
- Provides a software configurable delay register to compensate for differences in frame boundary arrival times for ingress ports without DMI allocated.
- Provides 25 software configurable delay registers for ingress ports one through 25 to allow arbitrary alignment of ingress frames to the device frame timing when DMI is allocated to an ingress port.

BLOCK DIAGRAM
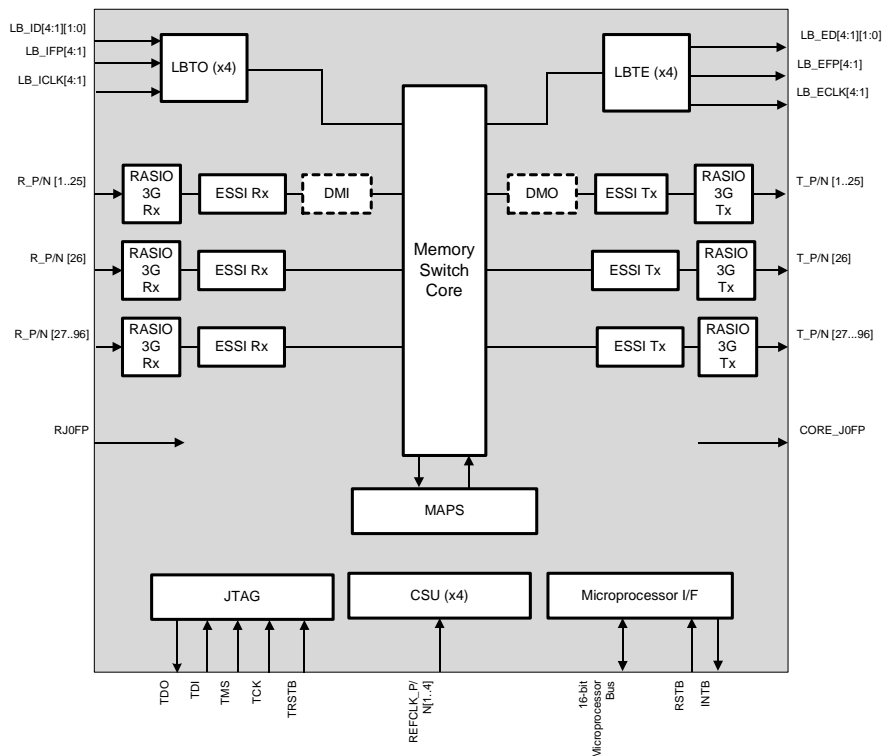
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- Provides 13 software configurable delay registers for delay management blocks 1 through 13 to allow arbitrary alignment of egress frames to the device frame timing when DMO is allocated to an egress port or group of ports.

PROTECTION SWITCHING

- Implements Message Assisted Protection Switching (MAPS) enabling hardware based protection decisions and switching.
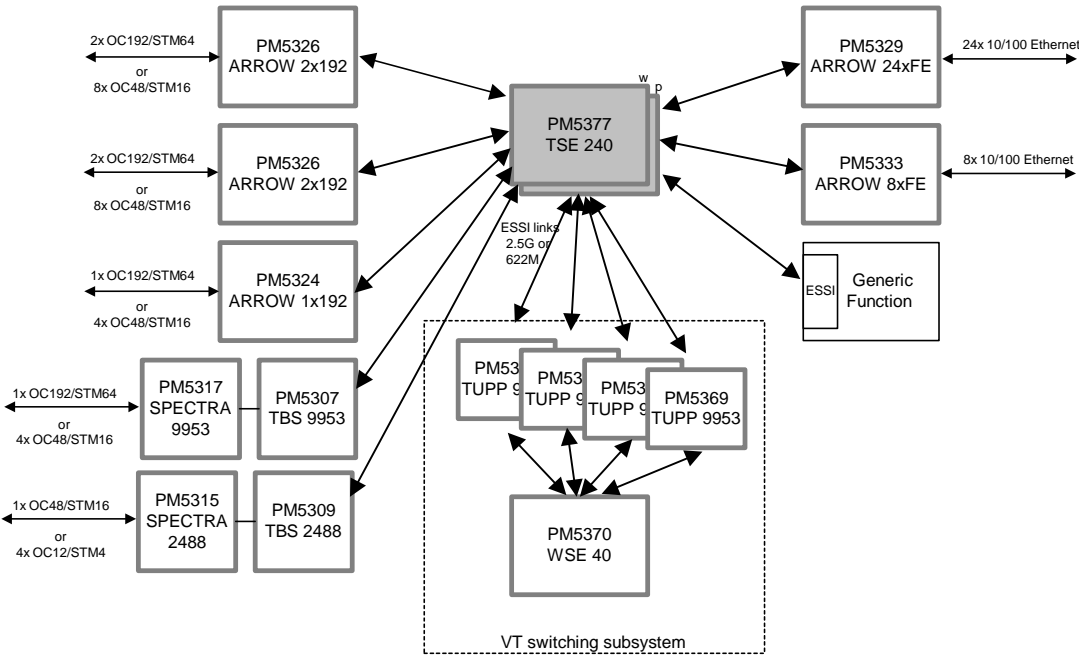
GENERAL

- RASIO 3G high-speed serial ingress and egress links.
- Low-power 1.2 V CMOS core logic with 2.5V digital outputs and 3.3V tolerant 2.5V digital inputs.
- 1152-pin FCBGA, 35 x 35 mm.
- Driven by a 155.52 MHz reference clock.
- Provides a standard five signal IEEE 1149.1 JTAG test port for boundary scan board test.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- 23 W typical power consumption when all features and links @ 2.488 Gbit/s are enabled and active.

APPLICATIONS

- SDH/SONET ADM
- MSPP
- Terminal Multiplexers
- Digital Cross-Connects

TYPICAL APPLICATION