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Title:	Datasheet for TPS653853-Q1		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:	Electrical Specification		

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

Changes from Revision B (November 2017) to Revision C (Janurary 2021) **Page**

- Added the Functional Safety-Compliant status to the *Features* section. 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed the descriptions in the *Pin Functions* section to add clarity. 12
- Added clarification on respect to the GND pin in the *Absolute Maximum Ratings*, *Recommended Operating Conditions* , *Electrical Characteristics* and *Timing Requirements* section 14
- Added a note in the *Electrical Characteristics — Supply Voltage and Current Consumption* section to clarify dependency of COLD_CRANK State exit on T_J, VDD6, VBAT_SAFING voltages and the slew rate of VBAT_SAFING recovery back to normal VBAT voltage levels..... 16
- Changed the description of capacitor for input and outputs to *Effective input or output capacitance from ceramic capacitor or capacitors* from *Value of input or output ceramic capacitor* in the *Electrical*

Characteristics table to clarify that more than one ceramic capacitor may be used in parallel or series, but the total effective capacitance must be in the specified range. 17

- Changed the description of capacitor ESR for input and outputs to *Effective ESR of input or output ceramic capacitor or capacitors* from *Value of ESR of input or output ceramic capacitor* in the *Electrical Characteristics* table to clarify that more than one ceramic capacitor may be used in parallel or series, but the total effective ESR must be in the specified range. 17
- Changed the description of inductor, L_{VDD6}, to *Effective inductance from inductor* from *Value of inductor* in the *Electrical Characteristics* table to clarify the total effective inductance must be in the specified range. 17
- Changed the description of inductor DCR to *Effective DCR of the inductor* from *Value of DCR of inductor* in the *Electrical Characteristics* table to clarify the total effective DCR must be in the specified range. 17
- Added C_{VBAT_SAFING} and ESR C_{VBAT_SAFING} (POS AN) in the *Electrical Characteristics — VDD6 Buck-Boost With Internal FETs* table.....17
- Changed the VDD6 output current in normal operation in boost mode (POS 1.3b, 1.3c) in the *Electrical Characteristics — VDD6 Buck-Boost With Internal FETs* table..... 17
- Added the minimum value, 2 A, for I_{VDD6_limit} (POS 1.5) in the *Electrical Characteristics — VDD6 Buck-Boost With Internal FETs* table.....17
- Changed the POS 1.13a and 1.13b and added POS 1.13c, 1.13d and 1.13e to VDD6 output voltage in low-power mode conditions for clarity since VDD6 output voltage in LPM depends on more than VSOUT2_LVL_LPSAM settings in the *Electrical Characteristics — VDD6 Buck-Boost With Internal FETs* table 17
- Changed the pulldown discharge resistance name from Rpd_{VDD6} to R_{PD_VDD6}, Rpd_{VDD5} to R_{PD_VDD5}, Rpd_{VDD3_5} to $R_{PD_VDD3/5}$, Rpd_{VSOUT1} to R_{PD_VSOUT1} and Rpd_{VSOUT2} to R_{PD_VSOUT2} for consistency in the *Electrical Characteristics* table.....17
- Changed the maximum value, from 5.4 V to 5.1 V, for $VDD5_{max}$ (POS 2.4) and removed test condition *No VDD5 UV or OV detection* in the *Electrical Characteristics — VDD6 Buck-Boost With Internal FETs* table.... 18
- Changed the maximum value for $VDD3/5_{max}$ (POS 3.5a and 3.5b) from 3.5 V to 3.38V (POS 3.5a) and from 5.4 V to 5.1 V (POS 3.5b) in the *Electrical Characteristics — VDD6 Buck-Boost With Internal FETs* table..... 19
- Changed the pulldown resistance name from $VTRACK_{pd}$ to R_{PD_VTRACK}, IGN_{Rpd} to R_{PD_IGN}, $CANWU_{Rpd}$ to R_{PD_CANWU}, R_{PULL_DOWN} to $R_{PD_SDI_SCLK}$ for consistency in the *Electrical Characteristics* table..... 20
- Changed the difference between $VBATL_UV_{on}$ and $VBATL_UV_{off}$ thresholds parameter, POS 7.3, in the *Electrical Characteristics — Voltage Monitor* table.....22
- Added POS 7.44, 7.45, 7.46, 7.47, 7.52a, 7.52b, 7.53, 7.54 and 7.55 to the *Electrical Characteristics — Voltage Monitor* table. 22
- Made the following changes in the *Electrical Characteristics - Ignition and CAN Wakeup* section for clarity of device operation. Added a note about LBIST run impact on IGN deglitch. Added POS 8.1a, IGN_WUP falling threshold and clarified POS 8.1 IGN_WUP threshold is rising. Added POS 8.2a, CAN_WUP falling threshold and clarified POS 8.1 IGN_WUP threshold is rising. Changed POS 8.3, WUP_hyst, to tighten hysteresis. ...24
- Changed the maximum external load current, I_{CP}, in the *Electrical Characteristics - Charge Pump Section* section. 24
- Changed the pullup resistance name from $R_{NRES_ENDRV_PU}$ to $R_{PU_NRES_ENDRV}$ and R_{PULL_UP} to R_{PU_NCS} for consistency in the *Electrical Characteristics* table.....24
- Changed the minimum value for f_{LPMclk} (POS 13.2) from 880 kHz to 891 kHz (POS 12.2) in the *Electrical Characteristics — VDD6 Buck-Boost With Internal FETs* table.....26
- Added VSAM_Input_FLOAT_SWsig_on (POS 16.26) and Ileak_SAM_Input_SWsig_on (POS 16.27) in the *Electrical Characteristics — Steering Angle Monitor* table 26
- Added t_{HSDI}, POS 15.2, the SDI hold time, in the *Electrical Characteristics — Timing Requirements -- Serial Interface* table.....28
- Changed the description for t_{HCS}, POS 15.9, the NCS hold time, in the *Electrical Characteristics — Timing Requirements -- Serial Interface* table for clarity.....28
- Deleted the duplicate specifications for POS 15.12, R_{PULL_UP} (updated R_{PU_NCS}), and POS 15.13, R_{PULL_DOWN} (updated to $R_{PD_SDI_SCLK}$) from the *Timing Requirements — Serial Interface* table since they are in the *Electrical Characteristics — Serial Interface* 28

- Changed the description for SPI input buffer delays, POS 15.14 to POS 15.19 and POS 15.22 to POS 15.23 in the *Electrical Characteristics — Timing Requirements -- Serial Interface* table for clarity. 28
- Changed the description for SDO output buffer rise and fall time in the *Electrical Characteristics — Timing Requirements -- Serial Interface* table for clarity of load on SDO pin is C_{SDO} as specified in other locations of this table. 28
- Updated SPI Timing Parameter Figure to clarify SDO behaviour at the beginning of the SPI frame. 29
- Changed the charge pump sub-block in the *TPS653853-Q1 Functional Block Diagram* section for clarity of device operation. 32
- Changed the battery power supply monitored by the VMON block from VBATP to VBATL in the *TPS653853-Q1 Functional Block Diagram* for clarity and consistency. 32
- Added passive components needed for VDD6 Buck-Boost Converter in the *VDD6 Buck-Boost Converter* section. 33
- Changed the average and peak current limit descriptions and added a note for clarity of operation in the *VDD6 Buck-Boost Converter* section. 33
- Changed the VSOUT1 tracking description for better clarity of the VSOUT1 operation in the *VSOUT1 Regulator* section. 35
- Changed the VSOUT2 tracking description for better clarity of the VSOUT2 operation in the *VSOUT2 Regulator* section. 36
- Added a note in the *VSOUT2 Linear Regulator* section to add clarification when the application uses low-power SAM mode VSOUT2 must be configured for non-tracking mode. 36
- Added a note in the *VSOUT2 Linear Regulator* section to add clarification when the application uses VSOUT2 configured for 5 V in active states and 3.3V with low-power SAM mode . 36
- Changed the description in the *Charge Pump* section to clarify device operation. 37
- Changed the *Charge Pump* section and the *Detailed Design Description, Charge Pump* section by adding C_{PUMP} and C_{STORE} references to clarify capacitance needed for charge pump. 37
- Added a note about LBIST run impact on IGN deglitch in the *Wakeup* section to clarity device operation. Added clarification on IGN wake up from OFF state versus STAND-BY state behavour and IGN_PWRL use in the *Wakeup* section to clarity device operation. 37
- Changed the VDDx label to VDD5 and VDD3/5 and modified the VDD5 and VDD3/5 start up timing for clarity in the *Power-Up and Power-Down Behavior.* figure. 40
- Changed the VDDx label to VDD5 and VDD3/5 for clarity in the *IGN Power Latch and POST-RUN Reset.* figure. 40
- Deleted the deglitch time from VDDIO Overvoltage in Table 5-1 of the *Voltage Monitor* section. 43
- Changed the monitoring detection thresholds for VDD5_OV, VDD3/5_UV and VDD3/5_OV minimums in the *Voltage Monitoring Overview: Supply Input and Outputs* table to match section 4.11 Electrical Characteristics — Voltage Monitor 43
- Changed the description in the *Main Clock Monitor (CLOCK_ERROR)* section to add clarity. 45
- Added a note not to run ABIST and LBIST at the same time in the *Built-In Self Tests* section. 45
- Changed the register name WD_QUESTION_FDBCK to WD_QUESTION_FDBK in all locations to provide a consistent register name and consistent bit names, FDBK[1:0], in the datasheet. 63
- Added the and clarified the timing formulas and timing diagrams in the *TMS570 Mode* and *PWM Mode* sections. 72
- Changed formula for SAFETY_ERR_PWM_LMIN to correct value of $t_{(LOW)}$min in the *ERROR Pin Monitor—PWM Mode Example With Correct and Incorrect Timing* figure in the *PWM Mode* section. 74
- Changed formula for SAFETY_ERR_PWM_LMIN to correct value of $t_{(LOW)}$min in the *ERROR Pin Monitor: PWM Mode Example With Correct and Incorrect Timing* figure in the *PWM Mode* section. 74
- Changed the *Device-Controller State Diagram* section for clarity. Changed the VDD6 output voltage and the COLD_CRANK state exit condition description in dependency on VDD6_LPM bit setting during COLD_CRANK state and exit condition. Clarified the wake up conditions from OFF state. 85
- Added a note in the *COLD_CRANK State* section to clarify dependency of COLD_CRANK State exit on T_J, VDD6, VBAT_SAFING voltages and the slew rate of VBAT_SAFING recovery back to normal VBAT voltage levels. 88

- Changed the signal comparators hysteresis for VSOUT2 voltage when 3.3V to (typical) to match the electrical characteristics in the *Signal Comparators (SAM_COMP)* section.....93
- Changed the SAM sampling in normal operating states to include NOS_SAM_PERIOD, NOS_SAM_IDLE and NOS_SAM_SAMPLE for clarity of operation and corrected the typical period and sampling times in the *Rotation Counter Change in Normal Operating States* section..... 95
- Changed the phrase "MCU must sent" to "MCU must send" to correct typo in the *Rotation Counter Change in Normal Operating States* section.....95
- Changed the description of when the the MCU writes the SAM counter registers to correctly describe when the SAM_COS_MSB and SAM_SIN_MSB register is updated with the written data in the *Rotation Counter Change in Normal Operating States* section..... 95
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- Added a note in the *SAM_VS2_PU* section to add clarification when the application uses VSOUT2 configured for 5 V in active states and 3.3V with low-power SAM mode. 100
- Changed fist to first to correct typo in STAT[6] bit and STAT[3] bit descriptions in the *Device Status Flag Byte Response* section..... 108
- Changed the titles of the SPI MCRC figures in the *Device SPI Master CRC (MCRC) and Device SPI Slave CRC (SCRC)* sections because Master CRC (MCRC) and Slave CRC (SCRC) were swapped in the Figure title descriptions. 110
- Changed the descriptions of note 3 in the *SPI Command Space* table to add clarity about commands impacting POWER_ON_RST register and STAT[5] bit. 113
- Clarified the commands in the *SPI Command Space* table. 113
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- Changed the description of VDD6_ILIM to include peak-overcurrent event in the *SAFETY_STAT_2* register description. 119
- Added a note not to run ABIST and LBIST at the same time in the *SAFETY_BIST_CTRL Register* section 119
- Changed bit type from R/W to R for the ERROR_PIN_FAIL bit and the WD_FAIL bit in the *SAFETY_ERR_STAT_1* register description. 119
- Changed bit type from R to R/W for the PWMHMAX[7:0] bits and the PWMHMIN[7:0] bits in the *SAFETY_ERR_PWM_HMAX* and *SAFETY_ERR_PWM_HMIN* register description. 119
- Changed the note in the *VSOUT2_MODE* bit description of the section *SENS_CTRL Register* to add clarification when the application uses low-power SAM modes that VSOUT2 must be configured in non-tracking mode (default)..... 119
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- Changed the guidelines the *Layout* section for clarity. 180

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The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS653853-Q1	SLVSC02B	SLVSC02C

The document is not available on the TI website. Please contact the TI Customer Quality Engineer (CQE) for a copy of the datasheet.

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:

None.

Product Affected:

O3853QDCARQ1	O3853QDCATQ1		

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