CY24293 Automotive

Two Outputs PCI-Express Clock Generator

Features

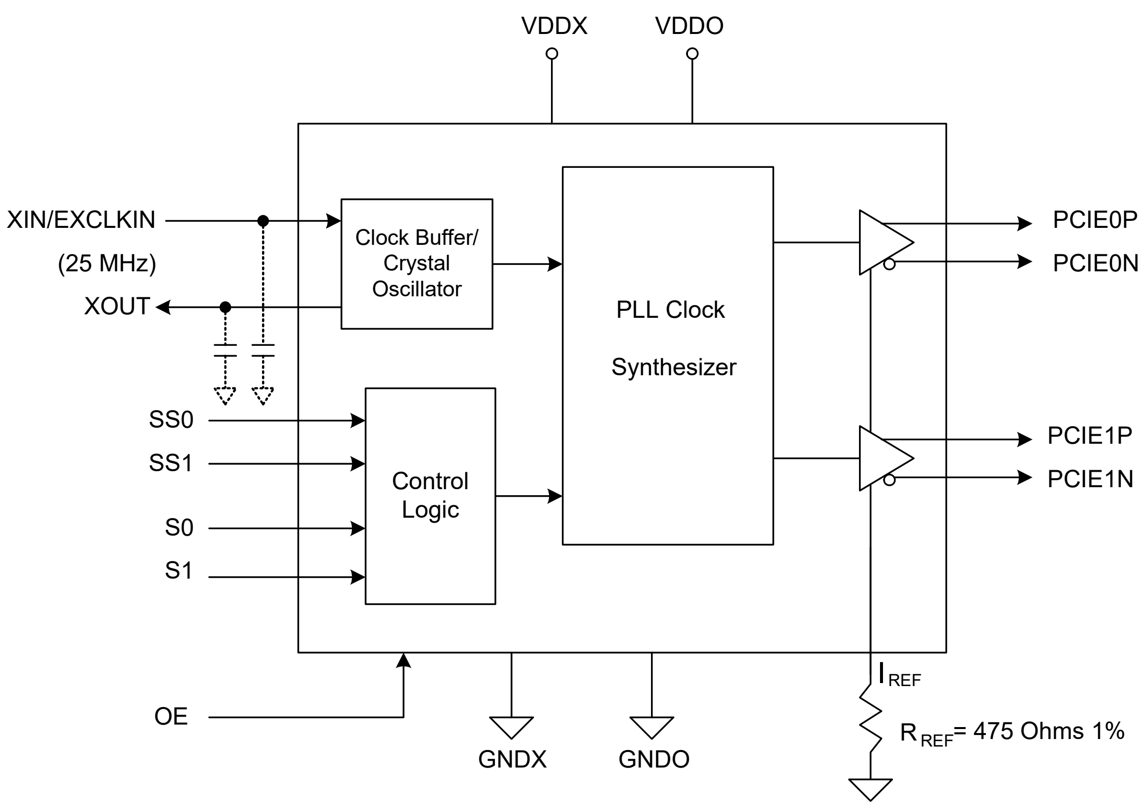
- 25 MHz crystal or clock input
- Two sets of differential PCI-Express clocks
- Pin selectable output frequencies
- Supports HCSL compatible output levels
- Spread Spectrum capability on all output clocks with pin selectable spread range
- 16-pin TSSOP package
- Operating voltage 3.3 V
- Automotive operating temperature range
- AEC-Q100 Qualified

Functional Description

CY24293 is a two output PCI-Express clock generator device intended for networking applications. The device takes 25 MHz crystal or clock input and provides two pairs of differential outputs at 25 MHz, 100 MHz, 125 MHz, or 200 MHz for HCSL signaling standard.

The device incorporates Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction. The spread type and amount can be selected using select pins.

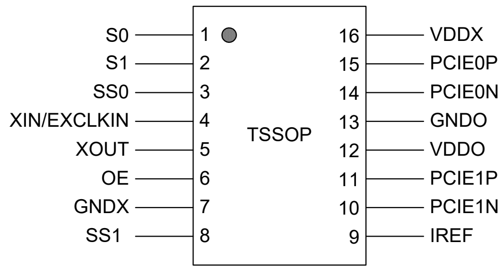
Logic Block Diagram



Contents

Pinouts

Figure 1. 16-pin TSSOP pinout



Pin Definitions

16-pin TSSOP

Pin Number	Pin Name	Pin Type	Description
1	S0	Input	Frequency select pin. Has internal weak pull-up. Refer to Output Frequency Selection Table on page 4.
2	S1	Input	Frequency select pin. Has internal weak pull-up. Refer to Output Frequency Selection Table on page 4.
3	SS0[1]	Input	Spread spectrum select pin 0. Has internal weak pull-up. Refer to Spread Selection Table on page 4.
4	XIN/EXCLKIN	Input	Crystal or clock input. 25 MHz fundamental mode crystal or clock input.
5	XOUT	Output	Crystal output. 25 MHz fundamental mode crystal input. Float for clock input.
6	OE	Input	High true output enable pin. When set low, PCI-E outputs are tri-stated. Has internal weak pull-up.
7	GNDX	Power	Ground
8	SS1[1]	Input	Spread spectrum select pin 1. Has internal weak pull-up. Refer to Spread Selection Table on page 4.
9	IREF	Output	Current set for all differential clock drivers. Connect 475 Ω resistor to ground.
10	PCIE1N	Output	Differential PCI-Express complementary clock output. Tristated when disabled.
11	PCIE1P	Output	Differential PCI-Express true clock output. Tristated when disabled.
12	VDDO[2]	Input	3.3 V power supply for output driver and analog circuits.
13	GNDO	Power	Ground
14	PCIE0N	Output	Differential PCI-Express complementary clock output. Tristated when disabled.
15	PCIE0P	Output	Differential PCI-Express true clock output. Tristated when disabled.
16	VDDX[2]	Input	3.3 V power supply for oscillator and digital circuits.

Notes
1. When powered up, state of SS1/SS0 pins should be held constant at the desired state.
2. VDDX must be supplied faster or equal to VDDO.

Output Frequency Selection Table

S1	S0	PCIE0[N,P], PCIE1[N,P]
0	0	25 MHz
0	1	100 MHz
1	0	125 MHz
1	1	200 MHz

Spread Selection Table

SS1 [3]	SS0 [3]	Spread%
0	0	No Spread
0	1	–0.5%
1	0	–0.75%
1	1	No Spread

Note
3. When powered up, the state of SS1/SS0 pins should be held constant at the desired state.

Application Information

Crystal Recommendations

CY24293 requires a parallel resonance crystal. Substituting a series resonance crystal causes the CY24293 to operate at the wrong frequency and violate the ppm specification. For most applications, there is a 300 ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 1. Crystal Recommendations

Frequency	Cut	Load Cap	Eff Series Rest (max)	Drive (max)	Tolerance (max)	Stability (max)	Aging (max)
25.00 MHz	Parallel	16 pF	30 Ω	1.0 mW	30 ppm	10 ppm	5 ppm/yr.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, consider the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

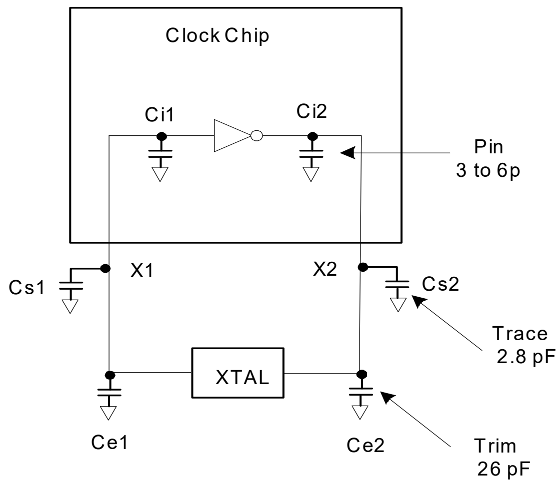
Figure 2 shows a typical crystal configuration using two trim capacitors. It is important to note that the trim capacitors in series with the crystal are not parallel. It is a common misconception that load capacitors are in parallel with the crystal and must be approximately equal to the load capacitance of the crystal. This is not true.

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading.

As mentioned in the previous section, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1, Ce2) must be calculated to provide equal capacitive loading on both sides.

Figure 2. Crystal Loading Example



Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2:

Load capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .... Crystal load capacitance

CLe .... Actual loading seen by crystal using standard value trim capacitors

Ce .... External trim capacitors

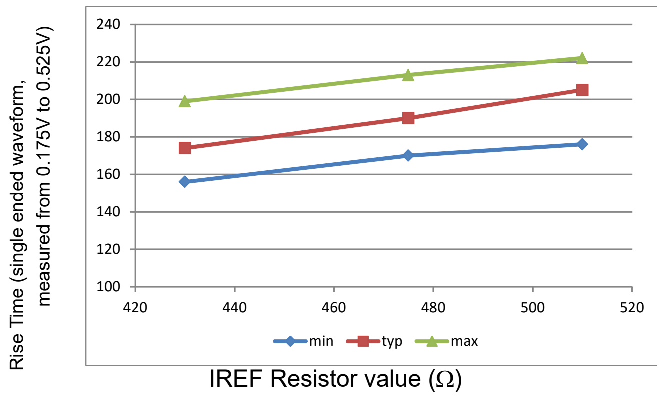
Cs .... Stray capacitance (terraced)

Ci .... Internal capacitance

Current Source (I_{REF}) Reference Resistor

If the board target trace impedance (Z) is 50 Ω, then for R_{REF} = 475 Ω (1%), provides IREF of 2.32 mA. The output current (I_{OH}) is equal to 6*I_{REF}. For other values of R_{REF}, refer to the following graph. It demonstrates the relationship of variation of IREF with reference to rise time/fall time (TR/TF).

Figure 3. IREF vs. TR/TF relationship (Typical)



Output Termination

The PCI-Express differential clock outputs of the CY24293 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are explained in Figure 4.

PCB Layout Recommendations

For optimum device performance and the lowest phase noise, the following guidelines must be observed:

1. Each 0.01 µF decoupling capacitor must be mounted on the component side of the board as close to the V_{DD} pin as possible.
2. No vias must be used between the decoupling capacitor and the V_{DD} pin.
3. The PCB trace to the V_{DD} pin and the ground via must be kept as short as possible. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces must be routed away from the CY24293. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Decoupling Capacitors

The decoupling capacitors of 0.01 µF must be connected between V_{DD} and GND as close to the device as possible. Do not share ground vias between components. Route power from the power source through the capacitor pad and then into the CY24293 pin.

PCI-Express (HCSL compatible) Layout Guidelines

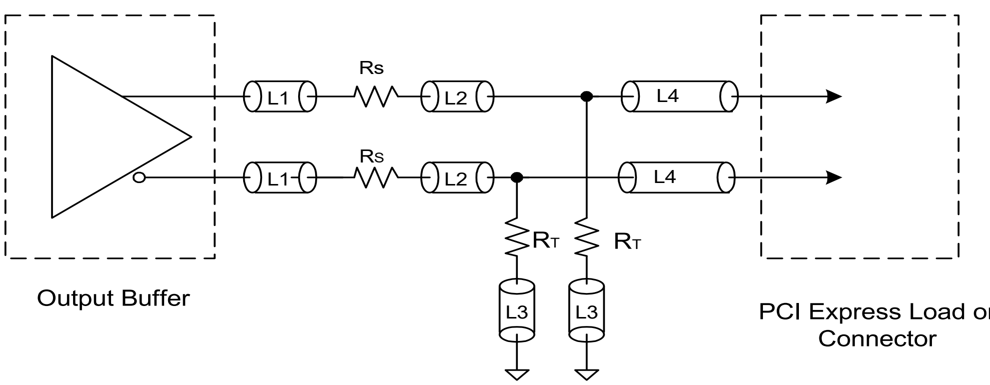
Table 2. Common Recommendations for Differential Routing

Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50 Ω trace	0.5 max	inch
L2 length, route as non-coupled 50 Ω trace	0.2 max	inch
L3 length, route as non-coupled 50 Ω trace	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω

Table 3. Differential Routing for PCI-Express Load or Connector

Differential Routing	Dimension or Value	Unit
L4 length, route as coupled microstrip 100 Ω differential trace	2 to 32	inch
L4 length, route as coupled stripline 100 Ω differential trace	1.8 to 30	inch

Figure 4. PCI-Express Differential Routing



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.6	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_J	Temperature, Junction	Non Functional	–65	+150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC EIA/JESD22-A114-E	2000	–	V
UL-94	Flammability rating	–	V-0 at 1/8 in.		
MSL	Moisture sensitivity level	–	3		

Recommended Operation Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply voltage	3.0	–	3.6	V
$T_{AI/AA}$	Automotive ambient temperature	–40	–	+85	°C
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

V_{DD} = 3.3 V ± 0.3 V, ambient temperature = –40 °C to +85 °C Automotive

Parameter [4]	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input low voltage	–	–0.3	–	0.8	V
V_{IH}	Input high voltage	–	2.0	–	V_{DD} + 0.3	V
V_{OL}	Output low voltage of PCIE0[P/N], PCIE1[P/N]	HCSL termination (R_S = 33 Ω, R_T = 49.9 Ω). See note 5	–0.2	0	0.05	V
V_{OH}	Output high voltage of PCIE0[P/N], PCIE1[P/N]	HCSL termination (R_S = 33 Ω, R_T = 49.9 Ω). See note 5	0.65	0.71	0.95	V
I_{DD}	Operating supply current	No load, OE = 1	–	45	60	mA
I_{DDOD}	Output disabled current	OE = 0	–	–	50	mA
C_{IN}	Input capacitance	All input pins	–	5	–	pF
R_{PU}	Pull-up resistance	S0, S1, SS0, SS1, OE	–	70k	–	Ω

Notes
4. Parameters are guaranteed by design and characterization. Not 100% tested in production.
5. Measurement taken from single-ended waveform.

Thermal Resistance

Parameter [6]	Description	Test Conditions	16-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	89	°C/W
θ_{JC}	Thermal resistance (junction to case)		12	°C/W

AC Electrical Characteristics

V_{DD} = 3.3 V ± 0.3 V, Ambient Temperature = –40 °C to +85 °C Automotive, Outputs HCSL terminated.

Parameter [7]	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input clock frequency (crystal or external clock)	–	–	25	–	MHz
F_{OUT}	Output frequency	HCSL termination	–	–	200	MHz
F_{ERR}	Frequency synthesis error	–	–	0	–	ppm
T_{CCJ}	Cycle-to-cycle jitter	See notes 8, 9	–	–	75	ps
$SP_{PROFILE}$	Spread modulation profile		–	–	Lexmark	type
SP_{MOD}	Spread modulation frequency		30	32	33	kHz
T_{DC}	Output clock duty cycle	See notes: 8, 10	45	50	55	%
T_{OEH}	Output enable time	OE going high to differential outputs becoming valid	–	–	200	ns
T_{OEL}	Output disable time	OE going low to differential outputs becoming invalid	–	–	200	ns
T_{LOCK}	Clock stabilization from power up	Measured from 90% of the applied power supply level	–	1	2	ms
T_R	Output rise time	Measured from 0.175 V to 0.525 V. See notes: 8, 11	130	–	700	ps
T_F	Output fall time	Measured from 0.525 V to 0.175 V. See notes: 8, 11	130	–	700	ps
DT_R	Rise time variation	F_{OUT} < 200 MHz, Max (T_R) – Min (T_R)	–	–	300	ps
DT_F	Fall time variation	F_{OUT} < 200 MHz, Max (T_F) – Min (T_F)	–	–	300	ps
T_{OSKEW}	Output skew	Measured at V_{CROSS} point. See note: 12	–	–	55	ps
V_{CROSS}	Absolute crossing point voltage	See notes: 10, 11, 13	0.25	0.35	0.55	V
V_{Xdelta}	Variation of V_{CROSS} over all rising clock edges	See notes: 10, 11, 14	–	–	140	mV

Notes
6. These parameters are guaranteed by design and are not tested.
7. Parameters are guaranteed by design and characterization. Not 100% tested in production.
8. Measured with Cload = 4 pF max. (scope probe + trace load).
9. Measurement taken from differential waveform (PCIEP minus PCIEN). Either single ended probes with math or a differential probe can be used.
10. Measured at crossing point where the instantaneous voltage value of the rising edge of PCIEP equals the falling edge of PCIEN.
11. Measurement taken from single ended waveform.
12. Measured at the rising 0 V point of the differential signal. Skew is the time difference of the rising 0 V point between any two differential signal pairs. The measurement is taken over 1000 samples, and the average value is used.
13. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
14. Defined as the total variation of all crossing voltages of Rising PCIEP and Falling PCIEN. This is the maximum allowed variance in V_{CROSS} for any particular system.

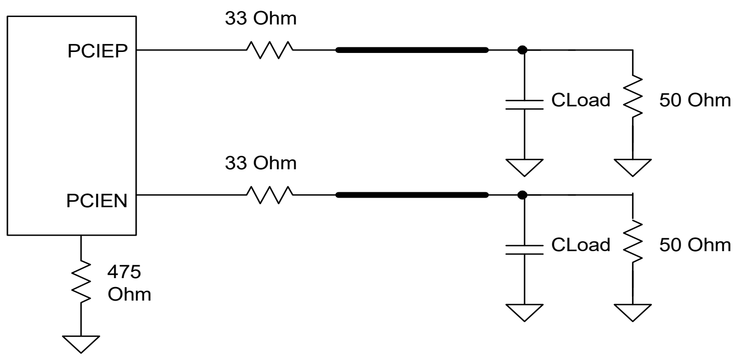
AC Electrical Characteristics

Differential 100 MHz, HCSL Terminated Outputs (Parameters for the PCI Express Specification. Use above AC Characteristics parameter where it is not listed in this section)

Parameter	Description	Test Conditions	Min	Typ	Max	Units
F_{OUT}	Output frequency		–	–	100	MHz
T_{PHJ}	Peak-to-peak phase jitter	10^{-6} BER. Note: 15	–	30	86	ps
ER_R	Rising edge rate	See notes: 16, 17	0.6	1.3	4.0	V/ns
ER_F	Falling edge rate	See notes: 16, 17	0.6	1.3	4.0	V/ns
$T_{PERIOD\ AVG}$	Average clock period accuracy	See notes: 16, 18	-300	–	2800	ppm
$T_{PERIOD\ ABS}$	Absolute clock period	See notes: 16, 19	9.847	–	10.203	ns
$RF_{MATCHING}$	Rising edge rate to falling edge rate matching	See note: 20, 21	–	–	20	%

Test and Measurement Setup

Figure 5. Test Load Configuration for Differential Output Signals



Notes

15. Phase jitter is determined using data captured on an oscilloscope at a sample rate of 20 GS/sec, for a minimum 100,000 continuous clock periods. This data is then processed using the ClockJitter 1.3.0 software from PCISIG, using the PCI_E_1_1 template.
16. Measurement taken from differential waveform (PCIEP minus PCIEN). Either single ended probes with math or a differential probe can be used.
17. Measured from -150 mV to +150 mV on the differential waveform (derived from PCIEP minus PCIEN). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
18. PPM refers to parts per million and is a DC absolute period accuracy specification. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum, there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread, resulting in a maximum average period specification of +2800 PPM.
19. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
20. Measurement taken from single ended waveform.
21. Matching applies to rising edge rate for PCIEP and falling edge for PCIEN. It is measured using a ± 75mV window centered on the median cross point where PCIEP rising meets PCIEN falling.

Ordering Information

Part Number	Type	Production Flow
Pb-Free		
CY24293ZXA	16-pin TSSOP	Automotive-A Grade, –40 °C to 85 °C
CY24293ZXAT	16-pin TSSOP – Tape and Reel	Automotive-A Grade, –40 °C to 85 °C

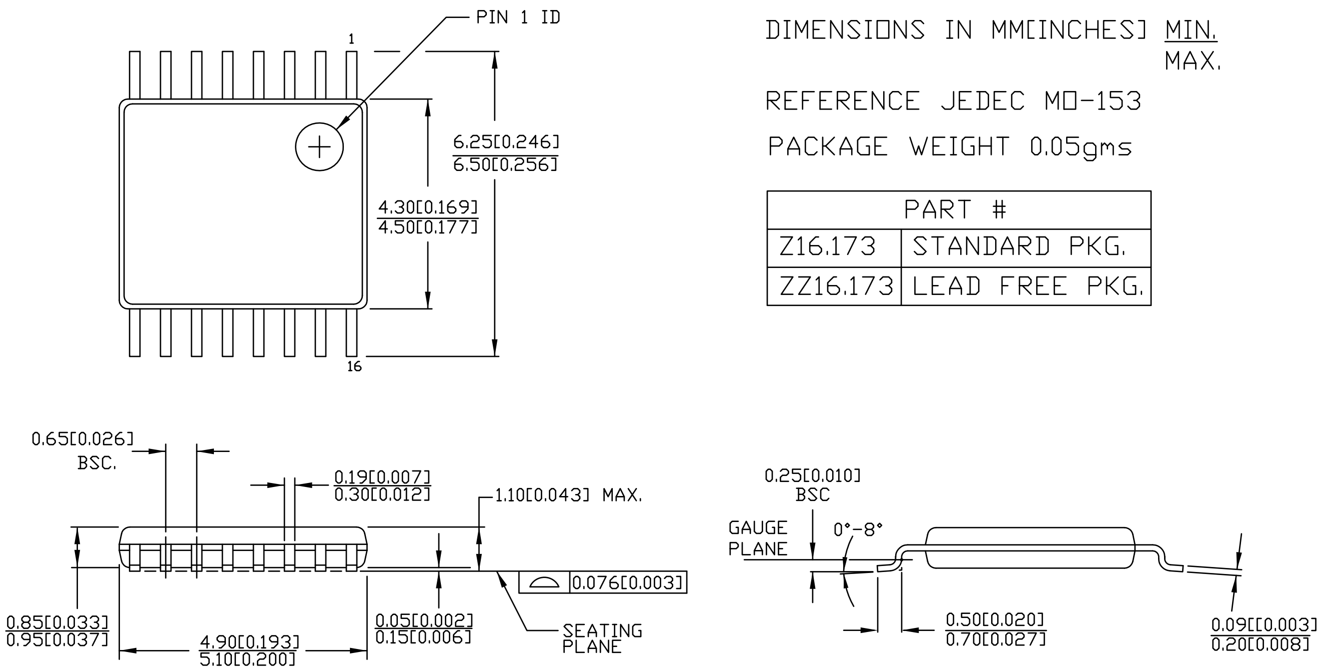
Ordering Code Definitions

CY 24293 Z X X X

- X = T or blank
  T = Tape and Reel; blank = Tube
- Temperature Range:
  A = Automotive-A Grade = –40 °C to 85 °C
- Pb-free
- Package Type:
  Z = 16-pin TSSOP
- Base Device Part Number
- Company ID: CY = Cypress

Package Diagram

Figure 6. 16-pin TSSOP 4.40 mm Body Z16.173/ZZ16.173 Package Outline, 51-85091



51-85091 *E

Acronyms

Acronym	Description
EIA	Electronic Industries Alliance
EMI	electromagnetic interference
ESD	electrostatic discharge
HCSL	high-speed current steering logic
JEDEC	Joint Electron Device Engineering Council
PCB	printed circuit board
PCI	peripheral component interconnect
PLL	phase-locked loop
TSSOP	thin shrunk small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µF	microfarad
mA	milliampere
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B	4881741	ANEE	08/12/2015	Changed status from Preliminary to Final.
*C	5279311	PSR	05/20/2016	Added Thermal Resistance. Updated to new template.
*D	6316873	XHT	09/21/2018	Updated to new template. Completing Sunset Review.

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