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Implementing the Teridian 73S8024RN in NDS Applications

1 Introduction

This application note highlights particular design considerations required to implement Conditional Access smart card interfaces in compliance with the NDS specification LC-T056I, when using the TERIDIAN 73S8024RN integrated circuit.

This note details in particular the design constraints related to the PCB layout and external components (choice and placement), and the typical tests that should be performed prior to submitting an application to NDS certification testing.

Reference document is the “IRD Interface Specifications for Use with NDS Smart Cards”, NDS document referenced LC-T056 Rev. I.

2 Demo Board

The data and chart measurements presented herein have been measured on a TERIDIAN 73S8024RN Demonstration Board, modified to meet NDS LC-T056I requirements. Refer to the “73S8024RN Demo Board User’s Manual” for general information about this board. Note that the electrical schematic of this board is by default designed to meet compliance with EMV4.0 specification. As a result, there are some minor differences between both electrical schematics. The TERIDIAN 73S8024RN configuration does not install components L1, C6 and C7. Other component differences are described in this note, and the NDS-compliant electrical schematic is described in the Figure 3.1

Note that the 73S8024RN Demo Board is available. Contact your TERIDIAN Semiconductor representative for further information concerning its availability.

3 Design Guide

3.1 Typical Electrical Schematic and Bill of Materials

The electrical schematic recommended for a typical NDS LC-T056I compliant smart card interface implementation is given in Figure 3-1, and its corresponding Bill of Materials is in Table 3-1. The jumpers represent the different configuration options for use with the 73S8024RN, and components references correspond to the Demo Board references.

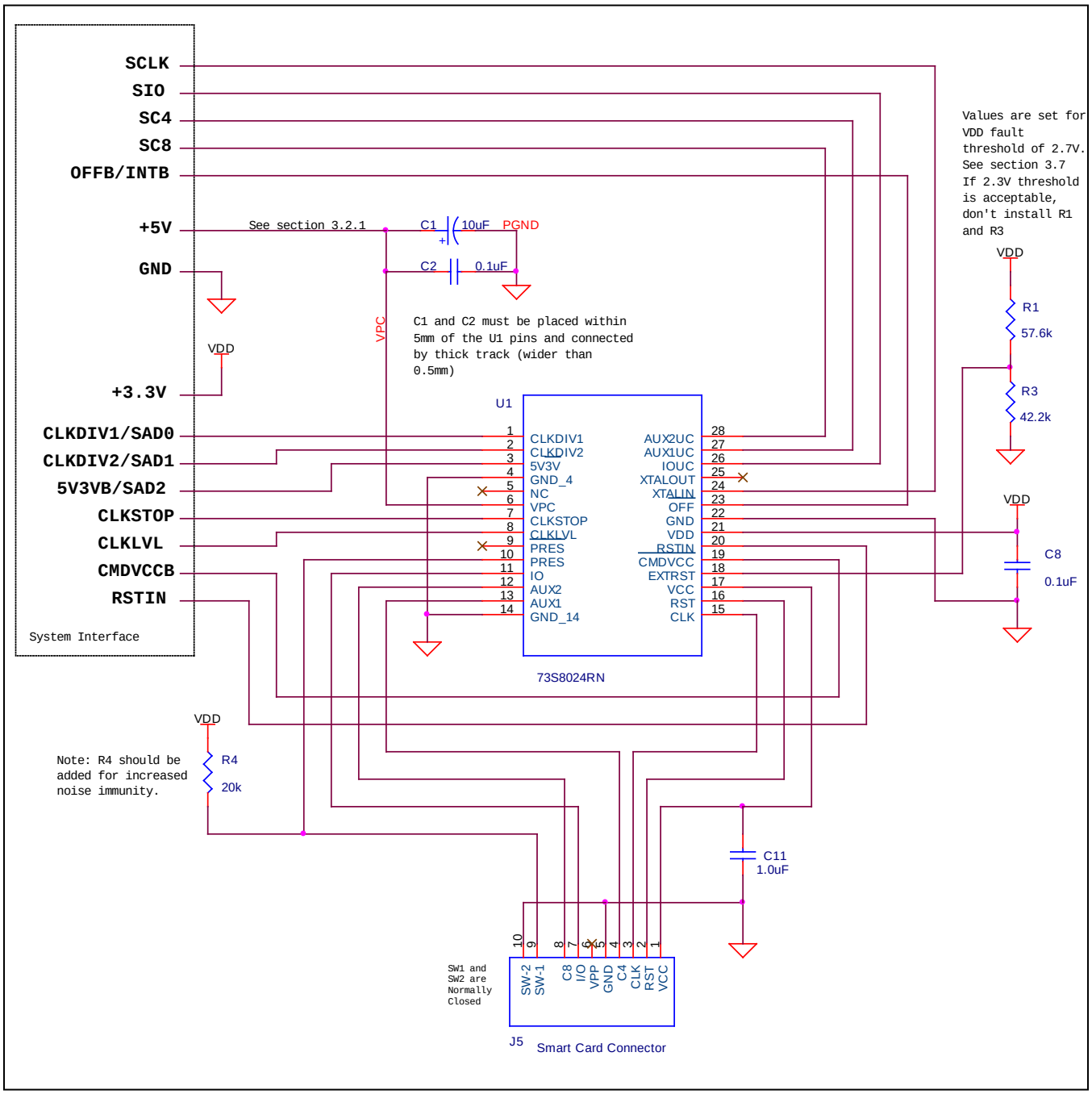


Figure 3-1: Typical Schematic using the 73S8024RN for NDS Applications

Item	Quantity	Reference	Part	PCB Footprint (see attached zip file)	Digikey part number	Part number	Manufactuer
1	1	C1	10µF	805	445-1363-1-ND	C2012X5R0J106M	TDK
2	1	C11	1µF (1)	603	445-1322-1-ND	C1608X5R0J105K	TDK
3	2	C2,C8	0.1µF	603	445-1317-1-ND	C1608X7R1C104K	TDK
4	1	J5	Smart Card Connector	ITT_CCM02-2504	ccm02-2504-ND	ccm02-2504	ITTCannon
5	1	R4	20k	603	P20KGCT-ND	ERJ-3GEYJ203V	Panasonic
6	1	U1	73S8024RN	28SOP	X	73S8024RN	TERIDIAN

Table 3-1: BOM for NDS-compliant configuration

3.2 Power Supply:

3.2.1 Analog Power Supply V_{PC}:

The 73S8024RN incorporates a Low-Drop-Out voltage regulator to generate the card power supply V_{CC}. The VPC pin is the power supply input of this regulator, and the correct V_{PC} voltage must be asserted on this pin in order to ensure proper generation of V_{CC} to the card.
Depending on the card voltage required, the V_{PC} power supply input can eventually be different, as follows:

Power supply V_{PC}, to support both 3V and 5V smart cards:
V_{PC} must be 5V nominal, and the following condition must be respected: **$4.85V \leq V_{PC} \leq 5.5V$**

Decoupling and PCB Layout:

The 73S8024R Demo Board and the recommended Electrical Schematic has 2 decoupling capacitors on V_{PC}. The larger capacitor is 10 µF and the small capacitor is 0.1µF (respectively C1 and C2). The smaller capacitor should be placed very close to the 73S8024RN. V_{PC} should be routed on a plane for best results. If no plane is possible, the larger capacitor should be as close as possible to the 73S8024RN.

3.2.2 Digital Power Supply:

The 73S8024RN has a separate power supply input V_{DD}, that powers the internal digital circuitry. V_{DD} is also the reference voltage to interface with the host microcontroller.
Operating V_{DD} voltage for implementing the 73S8024RN in NDS applications is **$2.7V \leq V_{DD} \leq 5.5V$**

3.3 Operating Temperature

The operating temperature range for implementing the 73S8024RN in NDS applications is between -40°C and 85°C.

3.4 Generation of the Smart Card Clock – CLK Signal

3.4.1 General

The 73S8024RN provides an oscillator that can generate a clock signal from an external crystal, connected to the pins XTALIN and XTALOUT. Alternatively, it can also accept an external clock signal presented on the XTALIN pin. When the external clock signal is used, XTALOUT must be left unconnected.

3.4.2 NDS Adherence

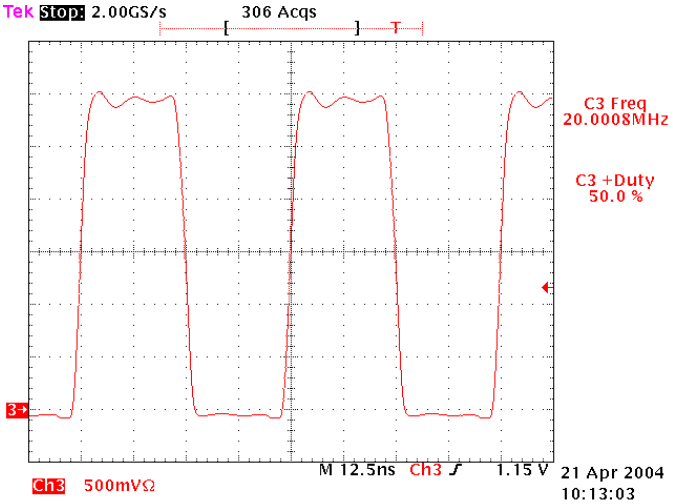
In order to use the 73S8024RN and meet full NDS compliance, typical hardware must be set up identically for all configurations. Typical NDS Conditional Access applications require card clock frequencies of 4.5MHz, 6.75MHz and 13.5MHz to be supported. The same hardware configuration is required for both Class A and Class B (5V and 3V smart card) operation. The NDS specification also requires the card clock duty-cycle to be in the range 45% to 55%.

3.4.3 73S8024RN Operational Configuration

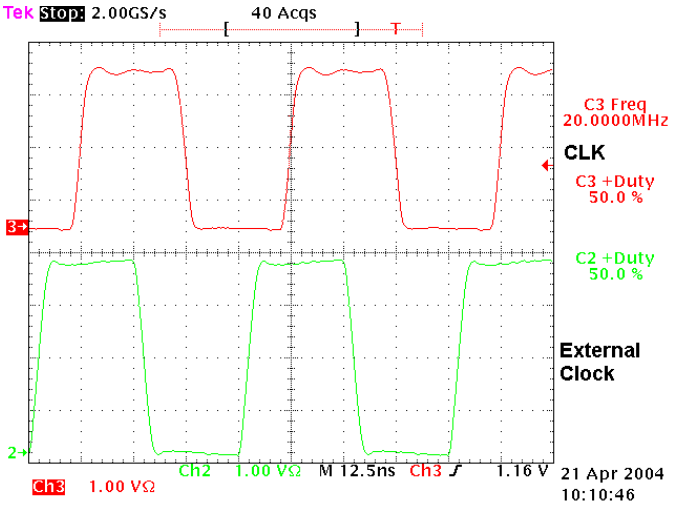
The typical NDS card clock frequencies of 4.5, 6.75 and 13.5MHz are derived from the maximum frequency of 13.5MHz divided by 1, 2 and 3 (13.5, 6.75 and 4.5). The 73S8024R supports a divide by 1, 2, 4 and 8 internal clock divider, but not divide by 3. As a result, a crystal that is used with the oscillator circuit will not be able to generate all three frequencies. If all three frequencies are required then an external clock source must be provided to generate them. If the clock divider rates of 1,2,4 and 8 are acceptable for a particular application then a crystal may be used.

Generation of the smart card clock signal (CLK) at the above-mentioned three NDS frequencies can be done in one of two ways, as long as the frequency of the signal applied on XTALIN is stable and doesn't exceed 27MHz. The first way uses the NDS clock frequencies of 4.5, 6.75 and 13.5 input directly to the 8024RN using the divide by one divider. The second way is to use of an external clock source that provides frequencies of 9, 13.5 and 27MHz. When the divide by 2 clock divider is configured, the NDS operational frequencies of 4.5, 6.75 and 13.5MHz are output to the smart card.

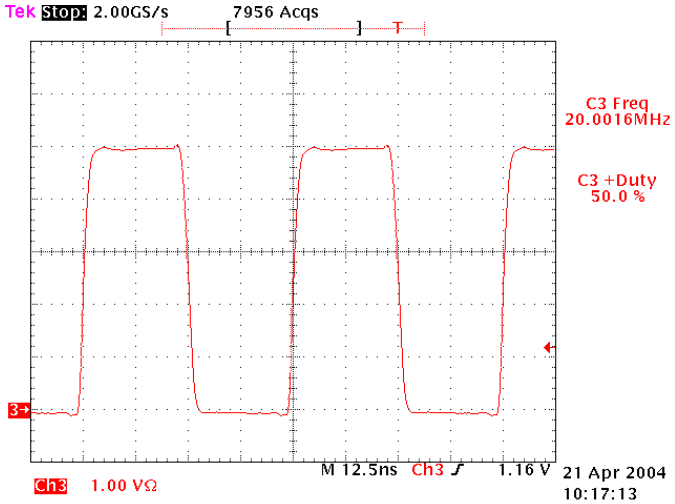
For applications that require higher smart card clock frequencies, the maximum external input clock/crystal speed is 27MHz. Between 20 and 27MHz the divide by 1 clock divider is not recommended. In order to get smart card frequencies up to 20MHz, use the divide by 1 divider for either the crystal oscillator or external clock input. The following scope capture diagrams show the smart card CLK for each configuration running at 20MHz.



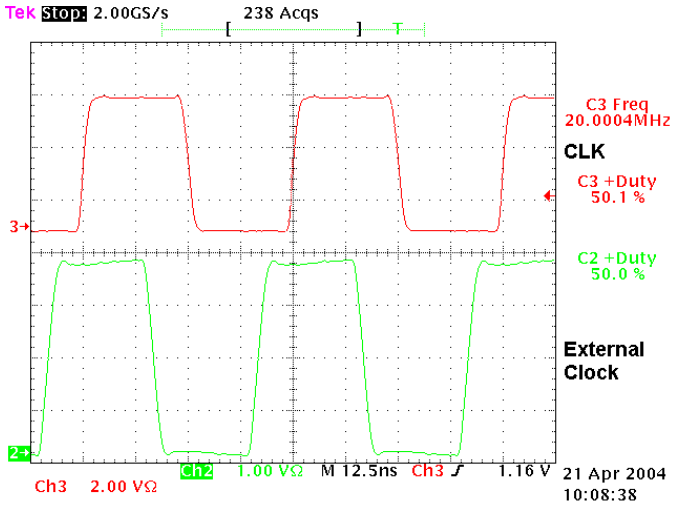
20MHz crystal clock source at 3V



20MHz external clock source at 3V



20MHz crystal source at 5V



20MHz external clock source at 5V

3.5 Crystal Load Capacitors

In order to insure the proper operation of the crystal oscillator circuit, the crystal load capacitors must be chosen appropriately. The crystal load capacitance (C_L as specified by the crystal manufacturer) must equal the series load capacitance (C_P) plus the stray board capacitance (C_S).

$C_L = C_S + C_P$. Where $C_P = (1 / (1/C1 + 1/C2))$

C1 and C2 are the load capacitors. If a balanced crystal load capacitors are used (recommended) then C1 = C2 and $C_P = C1 / 2$.

If C_L = 20 pF (from the crystal mfr spec) and the stray capacitance is assumed to be 5.0 pF, then

$C1 = 2 * (C_L - C_S) = 2 * (20pF – 5pF) = 30pF$.

Note: If the loading is any higher then the oscillator circuit may not generate the output clock properly. As a result, it is not recommended to use this oscillator circuit to drive any other circuitry.

3.6 VCC Output

The 73S8024RN Demo Board is configured with 2 output capacitors on the V_{CC} output, C9 and C11. A typical NDS implementation only requires 1 capacitor. C9 is not necessary and the value of C11 must be 1µF ± 50%. (If fitting the 1µF capacitor into an existing application is problematic, both C9 and C11 can be populated with 0.47µF ± 50% capacitors.) This capacitor should be placed as close to the card connector. This V_{CC} output configuration meets the NDS specifications for both voltage and current consisting of constant and dynamic loads. The ripple is shown to be less than 35 mV for DC loads and less than 60 mV for dynamic loads (typical). Figures 3.2 and 3.3 show V_{CC} ripple for 5V and 3V interfaces respectively.

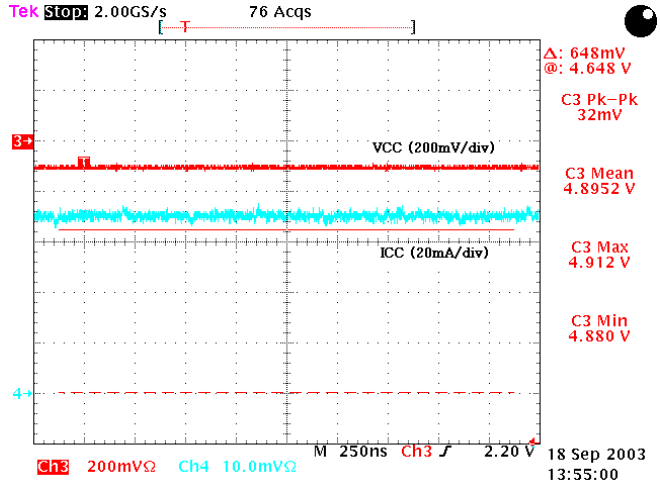


Figure 3-2: C11 (5V) w/65mA dc load current

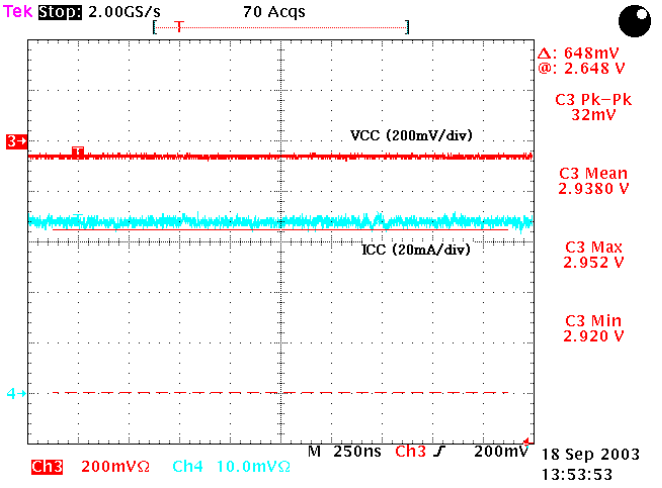


Figure 3-3: C11 (3V) w/65mA dc load current

According to NDS LC-T056I specification, deactivation time for V_{CC} must be less than 100µs. Figures 3.4 and 3.5 show actual measurements carried out on the 73S8024RN Demo Board using capacitor values of 0.47µF and 1.47µF for V_{CC} output decoupling (C11). The deactivation time is less than 80µs. It demonstrates that C11 = 1µF ±50% allows the 73S8024RN to meet the 100µs requirement.

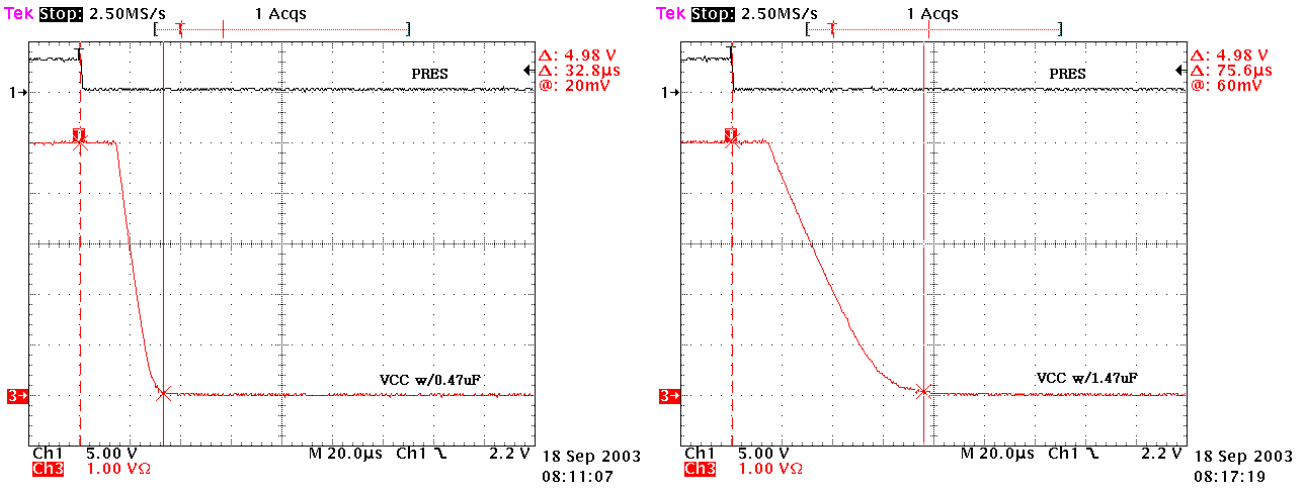


Figure 3-4: Deactivation time (0.47µF @VCC) Figure 3-5: Deactivation time (1.47µF @VCC)

3.7 Power Supply Threshold Detection

The 73S8024RN contains 3 different voltage supervisors. They monitor the voltages on V_{PC}, V_{CC} and V_{DD}. . Any voltage drop on any of these 3 signals is immediately detected and it initiates an automated card deactivation sequence that protects the card. V_{PC} and V_{CC} threshold voltages (also called fault voltages) are internally set. The voltage threshold of the V_{DD} voltage supervisor is internally set by default to 2.3V nominal. However, it may be desirable, in some applications, to modify this threshold value. For instance, when using a host controller that has a voltage operating range of 2.7V to 3.6V, the 73S8024RN will be, by default, still expecting the host to be able to exchange information with him whereas the host is actually powered down,. In such a case, the V_{DD} fault threshold voltage should be set to 2.7V, to automatically deactivate the smart card at the same time that the host is down. The pin VDDF_ADJ is used to connect an external resistor divider between VDD and GND to modify VDD-Fault. Figure 3.12 shows the connection of the external resistors.

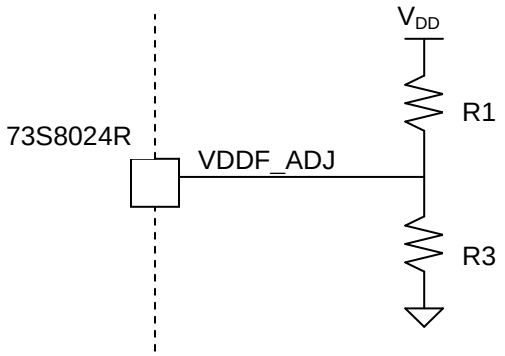


Figure 3-6: External resistor divider for setting V_{DDTH}

In order to set the new threshold voltage, the equivalent resistance must be determined. This resistance value will be designated K_x which is defined as R3 / (R1+R3), and is calculated as:

$$\mathbf{K_x = (2.789 / V_{TH}) - 0.6125}$$ where V_{TH} is the desired new threshold voltage.

To determine the values of R1 and R3, use the following formulas:

$$\mathbf{R1 = 24000 / K_x} \qquad \mathbf{R3 = R1*(K_x / (1 – K_x))}$$

Taking the example above, where a V_{DD} fault threshold voltage of 2.7V is desired, solving for K_x gives:
→ K_x = (2.789 / 2.7) - 0.6125 = 0.42046.
Solving for R1 gives: → R1 = 24000 / 0.42046 = 57080.
Solving for R3 gives: → R3 = 57080 *(0.42046 / (1 – 0.42046)) = 41412.
Using standard 1 % resistor values gives R1 = 57.6KΩ and R3 = 42.4KΩ.
These values give an equivalent resistance of K_x = 0.4228, a 0.6% error.

If the 2.3V default threshold is acceptable, this pin must be left unconnected.