TPS2115A-Q1 Auto-Switching Power Multiplexer

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 3: –40°C to 85°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4A
- Two-Input One-Output Power Multiplexer With Low $r_{DS(on)}$ Switch...84 mΩ (Typical)
- Reverse and Cross-Conduction Blocking
- Wide Operating Voltage Range...2.8 V to 5.5 V
- Low Standby Current...0.5 µA (Typical)
- Low Operating Current...55 µA (Typical)
- Adjustable Current Limit
- Controlled Output-Voltage Transition Times Limit Inrush Current and Minimize Output Voltage Hold-Up Capacitance
- CMOS- and TTL-Compatible Control Inputs
- Manual and Auto-Switching Operating Modes
- Thermal Shutdown
- Available in TSSOP-8 (PW) Package

2 Applications

- Automotive Power Multiplexing Applications
- Infotainment
- Navigation
- Multimedia Functions: Digital Radios, MP3 Players, Phone Chargers
- Camera Applications

3 Description

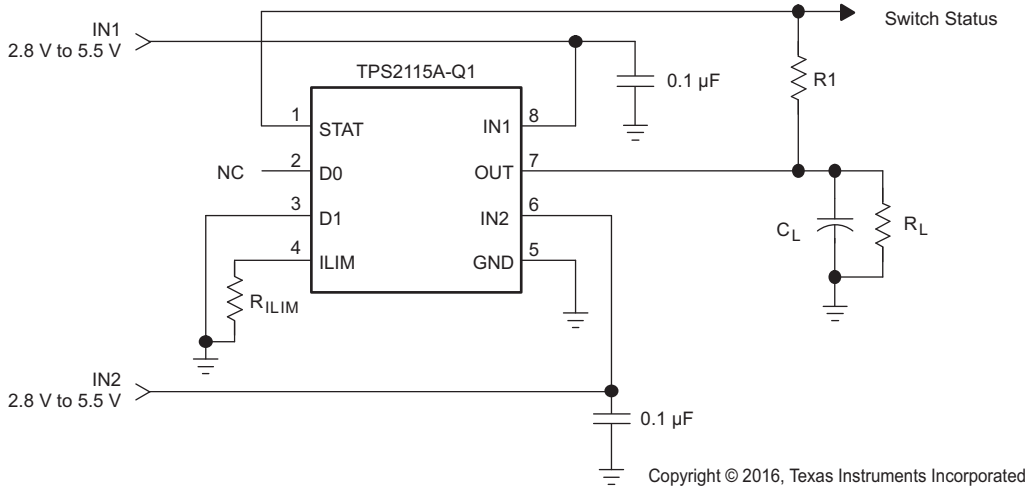
The TPS2115A-Q1 power multiplexer enables seamless transition between two power supplies, such as a two supply rails or a battery and AC to DC wall adapter. Each supply operates at 2.8 V to 5.5 V and the output can deliver up to 1 A. The TPS2115A-Q1 device includes extensive protection circuitry including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2115A-Q1	TSSOP (8)	4.40 mm × 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

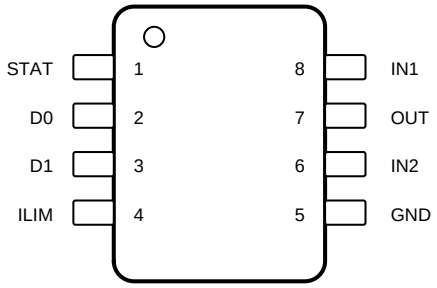
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2008) to Revision A **Page**

- Changed Applications list ... 1
- Changed TPS2115A to TPS2155A-Q1 throughout document ... 1
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed Continuous output current from 1.5mA to 1.5A in Absolute Maximum Ratings table ... 3
- Moved Figure 1 to *Switching Characteristics* section ... 6
- Moved test circuits from *Typical Characteristics* to *Parameter Measurement Information* section ... 7
- Changed info in D0 column with info from D1 column and moved table to *Device Functional Modes* section ... 12

5 Pin Configuration and Functions

PW Package
8-Pin TSSOP
Top View



Pin Functions

PIN		Type	DESCRIPTION
NAME	NO.		
D0	2	I	TTL- and CMOS-compatible input pins. Each pin has a 1-μA pullup. The *Truth Table* shows the functionality of D0 and D1.
D1	3	I	
GND	5	GND	Ground
IN1	8	PWR	Primary supply power-switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
IN2	6	PWR	Secondary supply power-switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
ILIM	4	I	A resistor R_{ILIM} from ILIM to GND sets the current limit I_L to $500/R_{ILIM}$.
OUT	7	O	Power switch output
STAT	1	O	Open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (that is EN is equal to logic 0).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_I	Input voltage range	IN1, IN2, D0, D1, ILIM	–0.3	6	V
V_O	Output voltage range	OUT, STAT	–0.3	6	V
$I_{O(sink)}$	Output sink current	STAT		5	mA
I_O	Continuous output current	OUT		1.5	A
P_D	Continuous total-power dissipation			See *Thermal Information*	
T_A	Operating free-air temperature range		–40	85	°C
T_J	Operating virtual-junction temperature range		–40	125	°C
T_{lead}	Lead temperature soldering		1,6 mm (1/16 inch) from case for 10 seconds	260	°C
Storage temperature, T_{stg}			–65	150°	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±500	

6.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
V_I	Input voltage	IN1	$V_{I(IN2)} \geq 2.8$ V	1.5		5.5	V
			$V_{I(IN2)} < 2.8$ V	2.8		5.5	
		IN2	$V_{I(IN1)} \geq 2.8$ V	1.5		5.5	
			$V_{I(IN1)} < 2.8$ V	2.8		5.5	
		D0, D1		0		5.5	
V_{IH}	High-level input voltage	D0, D1		2			V
V_{IL}	Low-level input voltage	D0, D1				0.7	V
I_O	Current limit adjustment range	OUT		0.63		1.25	A
T_A	Operating free-air temperature			–40		85	°C
T_J	Operating virtual-junction temperature range			–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS2115A-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	159.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{ILIM} = 400$ Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH [1]							
$r_{DS(on)}$	Drain-source on-state resistance (INx to OUT)	$T_A = 25°C$, $I_L = 500$ mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V		84	110	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V		84	110	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V		84	110	
		$T_A = 85°C$, $I_L = 500$ mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V			150	
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V			150	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V			150	
LOGIC INPUTS (D0 AND D1)							
I_I	Input current at D0 or D1	D0 or D1 = high, sink current				1	µA
		D0 or D1 = low, source current		0.5	1.4	5	
SUPPLY AND LEAKAGE CURRENTS							
Supply current from IN1 (operating)		D1 = high, D0 = low (IN1 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A			55	90	µA
		D1 = high, D0 = low (IN1 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A			1	12	
		D0 = D1 = low (IN2 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A				75	
		D0 = D1 = low (IN2 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A				1	

(1) The TPS2115A-Q1 device can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

Electrical Characteristics (continued)

over operating free-air temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{ILIM} = 400\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply current from IN2 (operating)		D1 = high, D0 = low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A				1	µA
		D1 = high, D0 = low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A				75	
		D0 = D1 = low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A			1	12	
		D0 = D1 = low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A			55	90	
Quiescent current from IN1 (standby)		D0 = D1 = high (inactive), $I_{O(OUT)}$ = 0 A	$V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V		0.5	2	µA
			$V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V			1	
Quiescent current from IN2 (standby)		D0 = D1 = high (inactive), $I_{O(OUT)}$ = 0 A	$V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V			1	µA
			$V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V		0.5	2	
Forward leakage current from IN1 (measured from OUT to GND)		D0 = D1 = high (inactive), $V_{I(IN1)}$ = 5.5 V, IN2 open, $V_{O(OUT)}$ = 0 V (shorted), T_A = 25°C			0.1	5	µA
Forward leakage current from IN2 (measured from OUT to GND)		D0 = D1= high (inactive), $V_{I(IN2)}$ = 5.5 V, IN1 open, $V_{O(OUT)}$ = 0 V (shorted), T_A = 25°C			0.1	5	µA
Reverse leakage current to INx (measured from INx to GND)		D0 = D1 = high (inactive), $V_{I(INx)}$ = 0 V, $V_{O(OUT)}$ = 5.5 V, T_A = 25°C			0.3	5	µA
CURRENT LIMIT CIRCUIT							
	Current limit accuracy	R_{ILIM} = 400 Ω		0.95	1.25	1.56	A
		R_{ILIM} = 700 Ω		0.47	0.71	0.99	
t_d	Current limit settling time	Time for short-circuit output current to settle within 10% of its steady state value			1		ms
I_I	Input current at ILIM	$V_{I(ILIM)}$ = 0 V, $I_{O(OUT)}$ = 0 A		–15		0	µA
UVLO							
IN1 and IN2 UVLO		Falling edge		1.15	1.25		V
		Rising edge			1.30	1.35	
IN1 and IN2 UVLO hysteresis				30	57	65	mV
Internal VDD UVLO (the higher of IN1 and IN2)		Falling edge		2.4	2.53		V
		Rising edge			2.58	2.8	
Internal VDD UVLO hysteresis				30	50	75	mV
UVLO deglitch for IN1, IN2		Falling edge			110		µs
REVERSE CONDUCTION BLOCKING							
$\Delta V_{IO(blk)}$	Minimum input-to-output voltage difference to block switching	D0 = D1 = high, $V_{I(INx)}$ = 3.3 V. Connect OUT to a 5-V supply through a series 1-kΩ resistor. Set D0 = low. Slowly decrease the supply voltage until OUT connects to IN1.		80	100	120	mV
THERMAL SHUTDOWN							
Thermal shutdown threshold		TPS2115A-Q1 device is in current limit.		135			°C
Recovery from thermal shutdown		TPS2115A-Q1 device is in current limit.		125			°C
Hysteresis					10		°C
IN2-IN1 COMPARATORS							
Hysteresis of IN2-IN1 comparator				0.1		0.2	V
Deglitch of IN2-IN1 comparator (both ↑↓)				10	20	50	µs
STAT OUTPUT							
I_{leak}	Leakage current	$V_{O(STAT)}$ = 5.5 V			0.01	1	µA
V_{sat}	Saturation voltage	$I_{I(STAT)}$ = 2 mA, IN1 switch is on			0.13	0.4	V
t_d	Deglitch time (falling edge only)				150		µs

6.6 Switching Characteristics

over operating free-air temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{ILIM} = 400\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Switch							
t_r	Output rise time from an enable	$V_{I(IN1)} = V_{I(IN2)} = 5$ V	$T_A = 25°C$, $C_L = 1$ µF, $I_L = 500$ mA, See Figure 1(a)	1	1.8	3	ms
t_f	Output fall time from a disable	$V_{I(IN1)} = V_{I(IN2)} = 5$ V	$T_A = 25°C$, $C_L = 1$ µF, $I_L = 500$ mA, See Figure 1(a)	0.5	1	2	ms
t_t	Transition time	IN1 to IN2 transition, $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5$ V	$T_A = 85°C$, $C_L = 10$ µF, $I_L = 500$ mA [Measure transition time as 10%-90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$], See Figure 1(b)		40	60	µs
		IN2 to IN1 transition, $V_{I(IN1)} = 5$ V, $V_{I(IN2)} = 3.3$ V			40	60	
t_{PLH1}	Turn-on propagation delay from enable	$V_{I(IN1)} = V_{I(IN2)} = 5$ V, Measured from enable to 10% of $V_{O(OUT)}$	$T_A = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(a)		1		ms
t_{PHL1}	Turn-off propagation delay from a disable	$V_{I(IN1)} = V_{I(IN2)} = 5$ V, Measured from disable to 90% of $V_{O(OUT)}$	$T_A = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(a)		5		ms
t_{PLH2}	Switch-over rising propagation delay	Logic 1 to Logic 0 transition on D1, $V_{I(IN1)} = 1.5$ V, $V_{I(IN2)} = 5$ V, $V_{I(D0)} = 0$ V, Measured from D1 to 10% of $V_{O(OUT)}$	$T_A = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(c)		40	100	µs
t_{PHL2}	Switch-over falling propagation delay	Logic 0 to Logic 1 transition on D1, $V_{I(IN1)} = 1.5$ V, $V_{I(IN2)} = 5$ V, $V_{I(D0)} = 0$ V, Measured from D1 to 90% of $V_{O(OUT)}$	$T_A = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(c)	2	5	10	ms

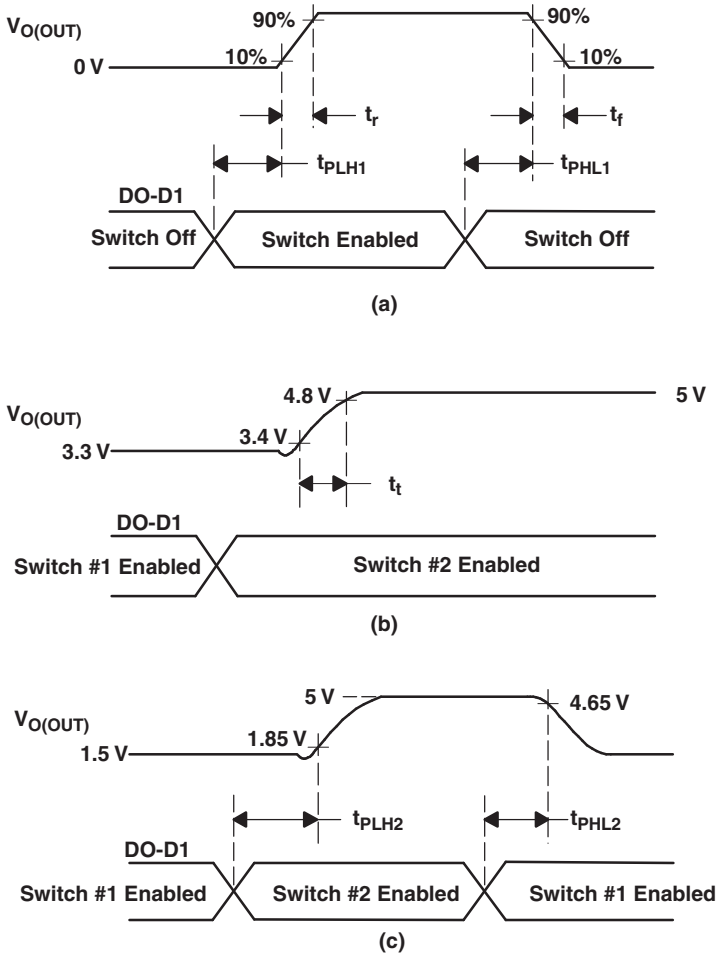
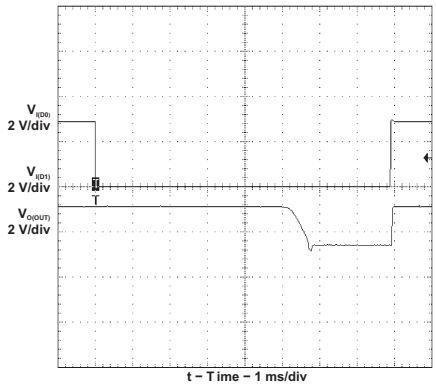


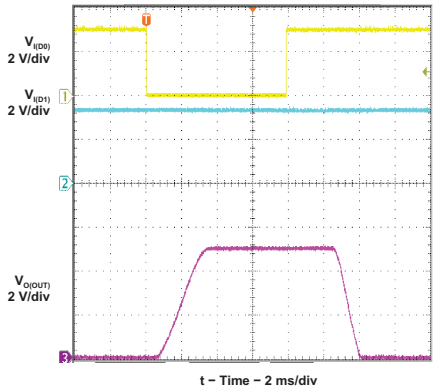
Figure 1. Propagation Delays and Transition Timing Waveforms

6.7 Typical Characteristics



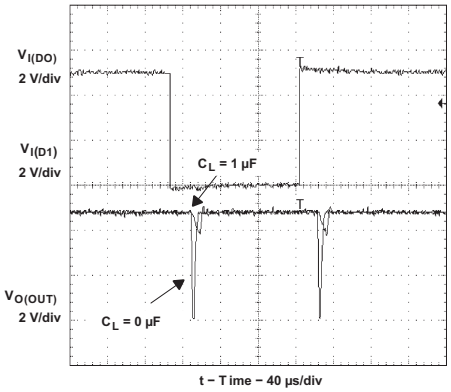
Input to D1: f=28 Hz, 78% Duty Cycle See Figure 14 for test circuit

Figure 2. Output Switchover Response



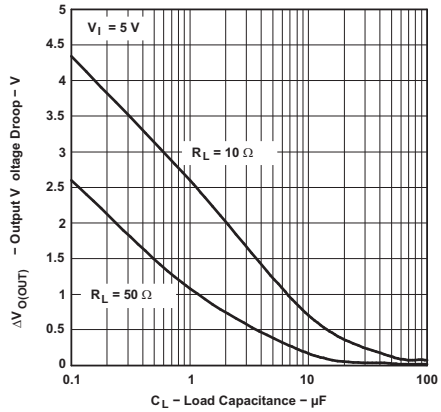
Input to D0: f=28 Hz, 78% Duty Cycle See Figure 15 for test circuit

Figure 3. Output Turn-On Response



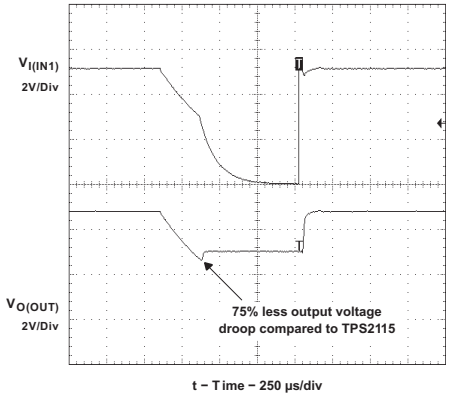
Input to D1: f = 580 Hz, 90% duty cycle See Figure 16 for test circuit

Figure 4. Output Switchover Voltage Droop



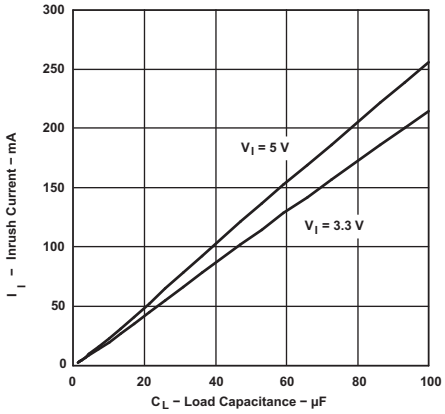
Input to D1: f = 28 Hz, 50% duty cycle See Figure 17 for test circuit

Figure 5. Output Switchover Voltage Droop vs Load Capacitance



Input to IN1 through switch: f = 220 Hz, 20% duty cycle See Figure 18 for test circuit

Figure 6. Auto Switchover Voltage Droop



Input to D0: f=28 Hz 90% duty cycle See Figure 19 for test circuit

Figure 7. Inrush Current vs Load Capacitance

Typical Characteristics (continued)

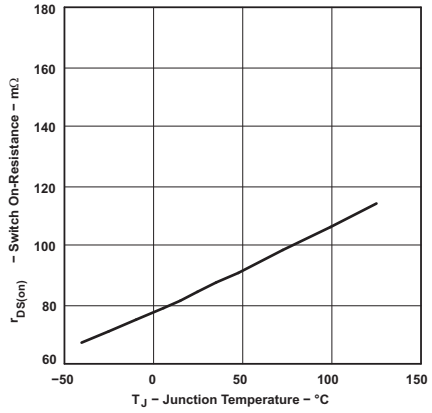


Figure 8. Switch On-Resistance vs Junction Temperature

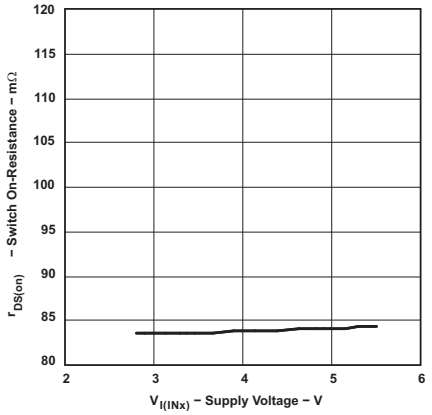
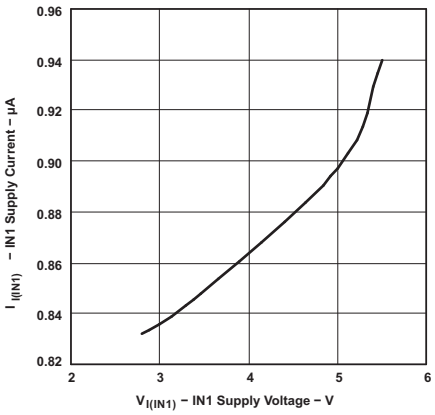
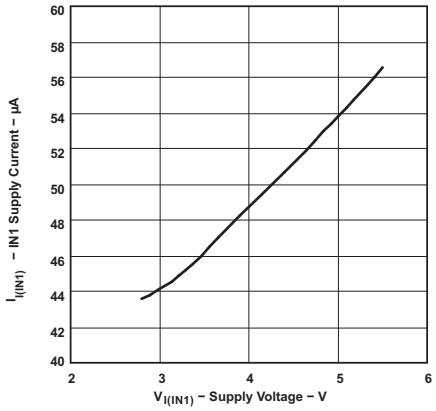


Figure 9. Switch On-Resistance vs Supply Voltage



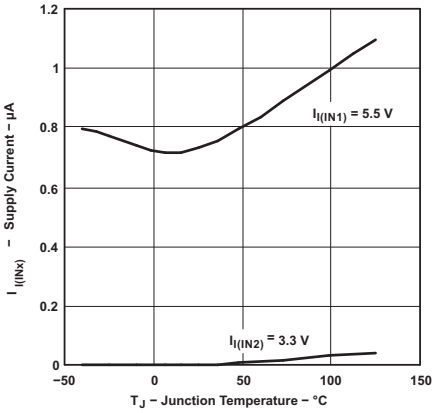
$V_{I(IN2)}$ = 0 V $I_{O(OUT)}$ = 0 A

Figure 10. IN1 Supply Current vs Supply Voltage (Device Disabled)



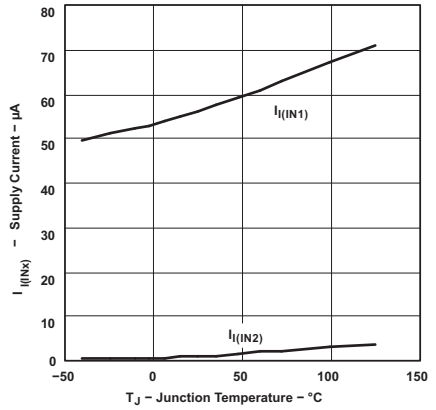
$V_{I(IN2)}$ = 0 V $I_{O(OUT)}$ = 0 A

Figure 11. IN1 Supply Current vs Supply Voltage (IN1 Switch ON)



$V_{I(IN1)}$ = 5.5 V $V_{I(IN2)}$ = 3.3 V $I_{O(OUT)}$ = 0 A

Figure 12. Supply Current vs Junction Temperature (Device Disabled)



$V_{I(IN1)}$ = 5.5 V $V_{I(IN2)}$ = 3.3 V $I_{O(OUT)}$ = 0 A

Figure 13. Supply Current vs Junction Temperature (IN1 Switch ON)

7 Parameter Measurement Information

7.1 Test Circuits

The following figures are the test circuits for the graphs in the *Typical Characteristics* section.

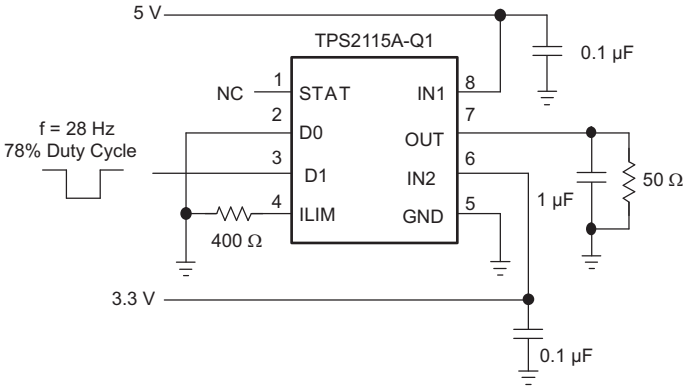


Figure 14. Output Switchover Response Test Circuit

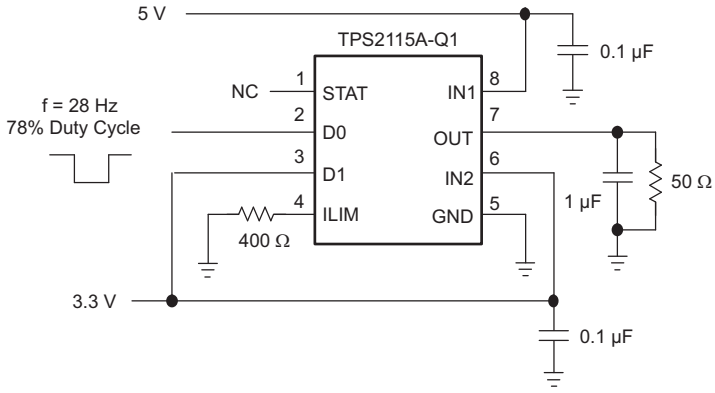


Figure 15. Output Turn-On Response Test Circuit

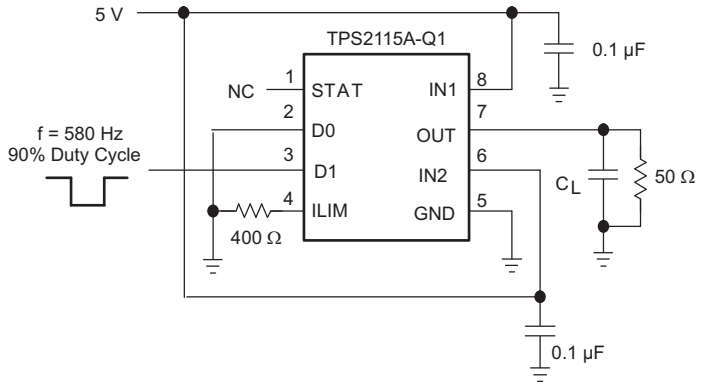


Figure 16. Output Switchover Voltage Droop Test Circuit

Test Circuits (continued)

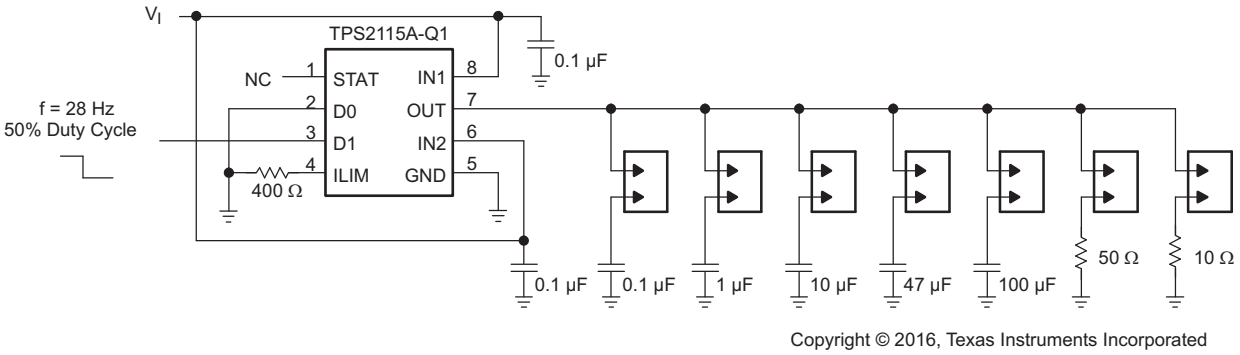


Figure 17. Output Switchover Voltage Droop vs Load Capacitance Test Circuit

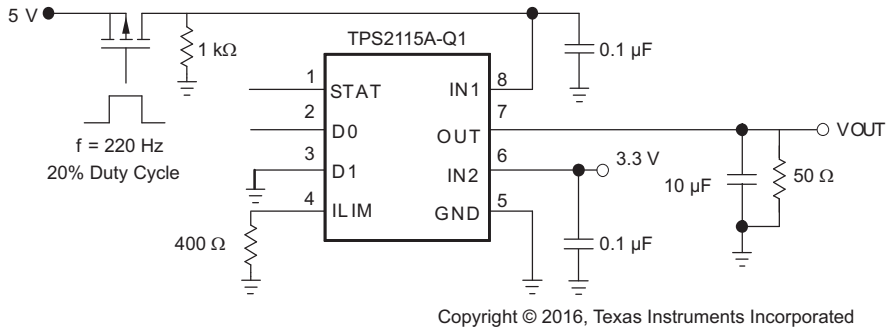


Figure 18. Auto Switchover Voltage Drop Test Circuit

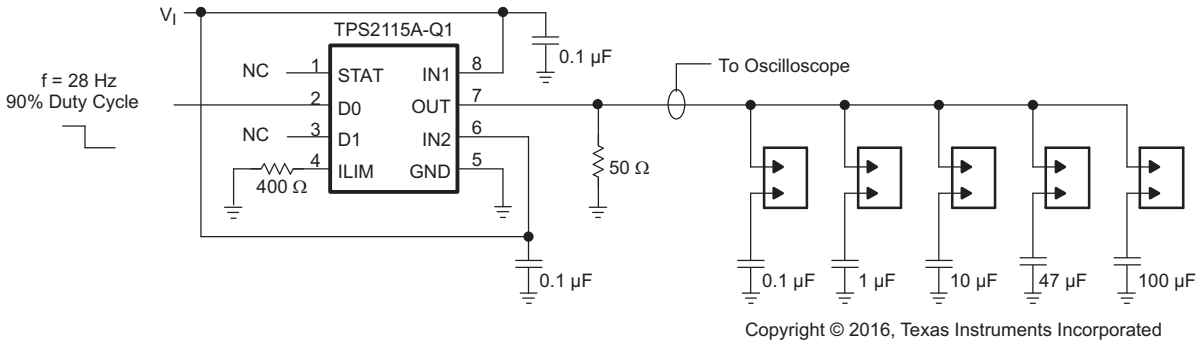


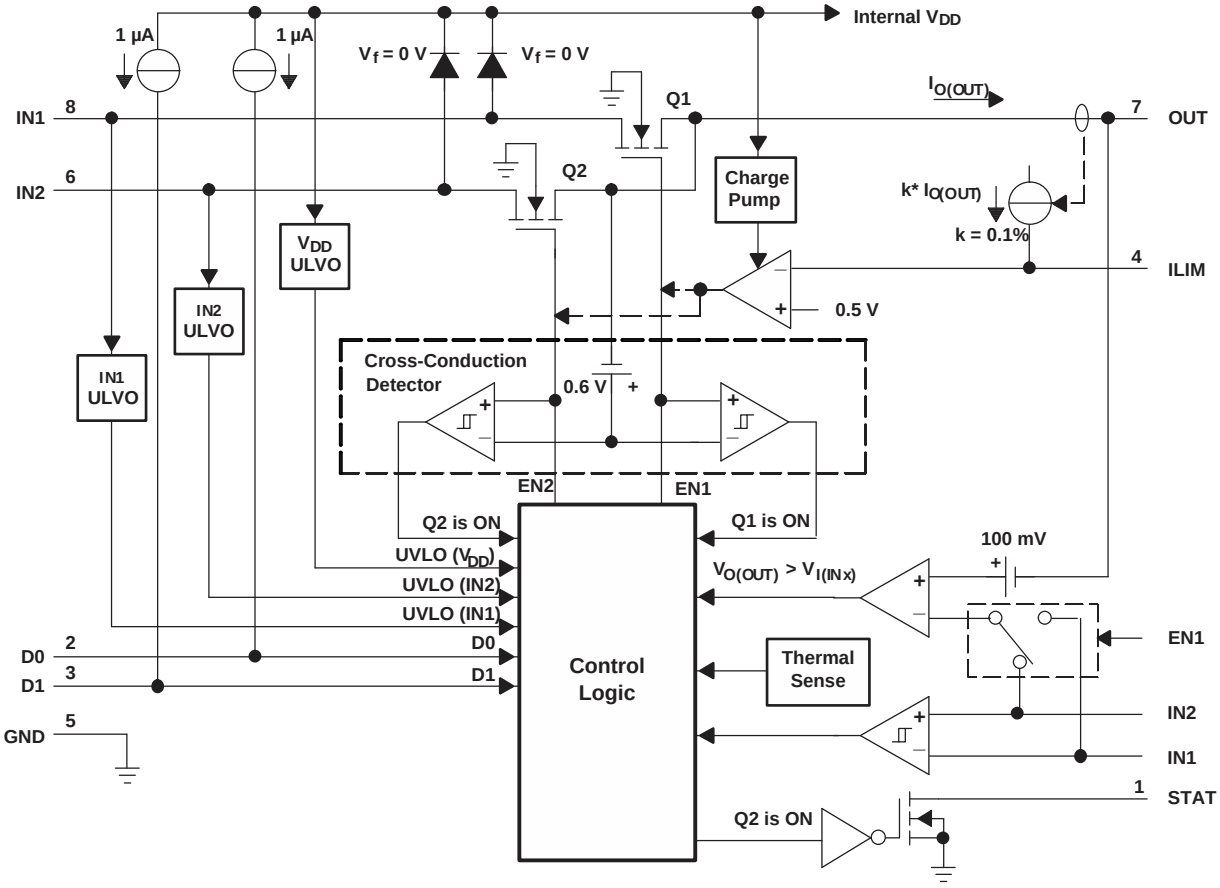
Figure 19. Output Capacitance Inrush Current vs Load Capacitance Test Circuit

8 Detailed Description

8.1 Overview

The TPS2115A-Q1 power multiplexer enables seamless transition between two power supplies, such as a two supply rails or a battery and AC-to-DC wall adapter. Each supply operates at 2.8 V to 5.5 V and the output can deliver up to 1 A. The TPS2115A-Q1 device includes extensive protection circuitry including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 N-Channel MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

8.3.2 Cross-Conduction Blocking

The switching circuitry ensures that both power switches never conducts at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

Feature Description (continued)

8.3.3 Reverse-Conduction Blocking

When the TPS2115A-Q1 device switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS2115A-Q1 device does not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, the supply remains connected regardless of output voltage.

8.3.4 Charge Pump

The higher voltage of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current-limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

8.3.5 Current Limiting

A resistor R_{ILIM} from ILIM to GND sets the current limit to ((500 Ω) / R_{ILIM}) A. It is recommended to keep the current limit set to 1.25 A or lower (R_{ILIM} ≥ 400 Ω). Setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

8.3.6 Output Voltage Slew-Rate Control

The TPS2115A-Q1 device slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see Table 1). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues such as pitting the connector power contacts when hot-plugging a load such as a PCI card. The TPS2115A-Q1 device slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

8.4 Device Functional Modes

Table 1 is the Truth Table for the TPS2115A-Q1 power multiplexer.

Table 1. Truth Table

D1	D0	$V_{I(IN2)} > V_{I(IN1)}$ (1)	STAT	OUT(2)
0	0	X	Hi-Z	IN2
0	1	No	0	IN1
0	1	Yes	Hi-Z	IN2
1	0	X	0	IN1
1	1	X	0	Hi-Z

(1) X = don't care
(2) The undervoltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1 or IN2 UVLO, or if neither of the supplies exceeds the internal V_{DD} UVLO.

8.4.1 Auto-Switching Mode

D0 equal to logic 1 and D1 equal to logic 0 selects the auto-switching mode. In this mode, OUT connects to the higher of IN1 and IN2.

8.4.2 Manual Switching Mode

D0 equal to logic 0 selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic 1, otherwise OUT connects to IN2.

9 Application and Information

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Some applications have two energy sources, one of which should be used in preference to another. The TPS2115A-Q1 allows either manual or automatic selection of the input supply depending on the device configuration and use in the specific application.

Figure 20 shows a circuit that connects IN1 to OUT until IN1 falls below a user-specified value. Once the voltage on IN1 falls below this value, the TPS2115A-Q1 device selects the higher of the two supplies. This usually means the TPS2115A-Q1 device swaps to the IN2 supply.

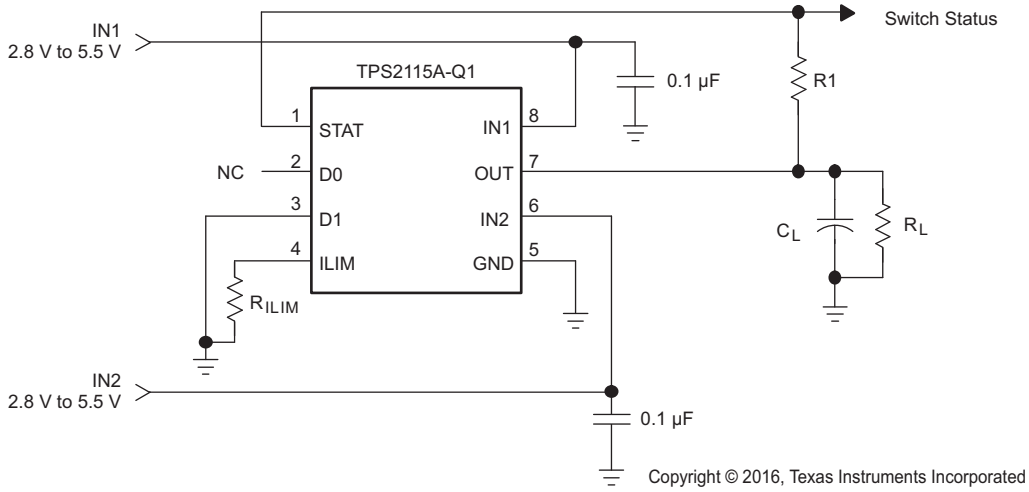


Figure 20. Auto-Selecting for a Dual Power Supply Application

In Figure 21, the multiplexer selects between two power supplies based upon the D1 logic signal. OUT connects to IN1 if D1 is logic 1; otherwise, OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.

Application Information (continued)

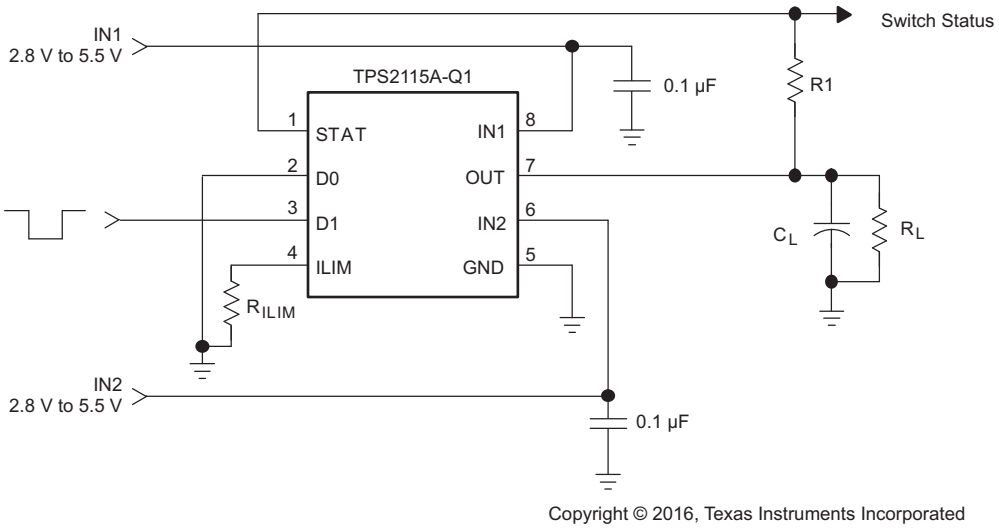


Figure 21. Manually Switching Power Sources

9.2 Typical Application

Figure 22 shows a circuit that connects IN1 to OUT until the voltage at IN1 falls below the voltage at IN2. Once the voltage on IN1 falls below the voltage on IN2, the TPS2115A-Q1 device selects IN2 since it is the higher of the two supplies.

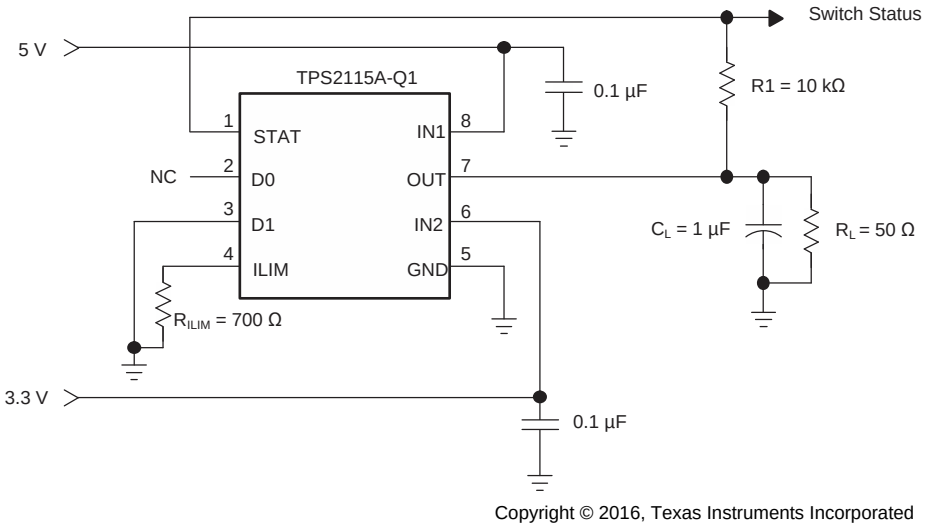


Figure 22. Auto-Selecting for a Dual Power Supply Application with 5 V for Normal Operation and 3.3 V Low Power Mode

9.2.1 Design Requirements

The application has two supply rails, the main supply is for normal operation with higher system current, bias current, and operation at 5 V. In this system, the second supply is needed for lower voltage, 3.3 V, with lower bias current during low-power mode. In addition, when the system enters low power mode, the other loads on the main supply need to be off. A power multiplexer is needed to connect the load automatically to the second supply when the system enters low-power mode keeping the load powered in low-power mode with minimal bias current. The load is equivalent to 50 Ω and the current limit should be set no higher than 1 A.

Typical Application (continued)

9.2.2 Detailed Design Procedure

The following steps are the detailed design procedure.

1. Connect the main power supply, 5 V, to IN1.
2. Connect the second 3.3-V supply to IN2 for the low-power mode.
3. Place local bypass capacitors of 0.1 µA on IN1 and IN2 to GND to minimize ripple during transition between the power supply inputs.
4. Leave D0 floating (unconnected). The internal pullup current source to Internal V_{DD} puts a logic high on the D0 pin.
5. Connect D1 to GND, logic low. The logic combination on D0 and D1 puts the device into Auto-Switching Mode.
6. The application load, R_L, is 50 Ω as given in the design requirements. Use a bulk capacitance, C_L, of 1 µF to buffer the output voltage from dropping on OUT during the transition between IN1 and IN2.

During normal operation of the system, the main power supply connected to IN1 is on and supplies 5 V. The voltage on IN1 is higher than IN2, so the path automatically selects IN1 to OUT and the device supplies the load, R_L (50 Ω), from IN1.

For low-power mode, the system turns off the main supply. The device automatically switches to the path of IN2 to OUT and the device supplies the load, R_L (50 Ω), from IN2 as soon as the voltage on IN1 is lower than the voltage on IN2.

To return to normal operation, the system turns on the main supply and when the voltage on IN1 is higher than the voltage on IN2, the path automatically selects IN1 to OUT and the device supplies the load, R_L (50 Ω), from IN1.

1. To set the current limit below 1 A, use an R_{ILIM} of 700 Ω according to Equation 1.

$$I_{LIM} = \left(\frac{500\ \Omega}{R_{ILIM}}\right) A = \left(\frac{500\ \Omega}{700\ \Omega}\right) A = 0.71\ A\ (typical) \quad (1)$$

2. Using the current limit accuracy in the electrical characteristics section, using R_{ILIM} of 700 Ω has a maximum current limit of 0.99 A, which is below the design requirement of 1 A.

Connect a pullup resistor, R_1, of 10 kΩ, to the host processor to monitor which input supply is selected.

9.2.3 Application Curve

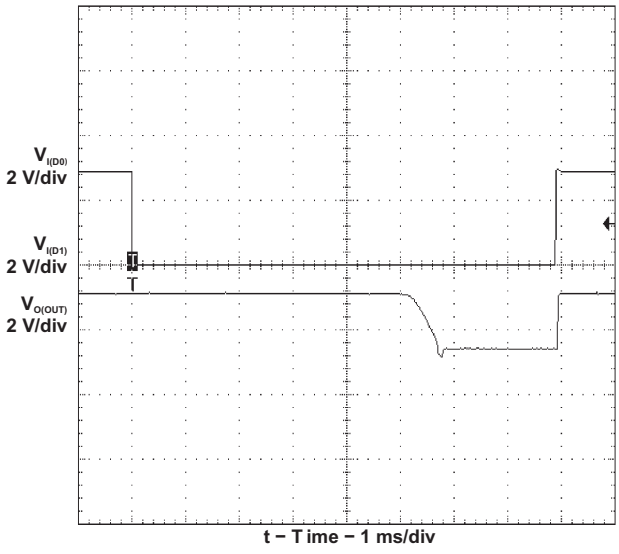


Figure 23. Output Switchover Response

10 Power Supply Recommendations

Use well-regulated supplies on IN1 and IN2 that have sufficient capacitance for the application load transients. As close as possible to the device, use a 0.1-µF ceramic bypass capacitor between IN1 and GND for the first power supply input and a 0.1-µF ceramic bypass capacitor between IN2 and GND for the second power supply input. The recommendation is to place a high-value capacitor between OUT and GND when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input or voltage drops during load transients or supply input transitions. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor may reduce high-frequency emissions.

11 Layout

11.1 Layout Guidelines

- For the first supply input (IN1), place the 0.1-µF bypass capacitor between the IN1 and GND as close as possible ensuring a low-impedance trace.
- For the second supply input (IN2), place the 0.1-µF bypass capacitor between the IN2 and GND as close as possible ensuring a low-impedance trace.
- Place a high-value capacitor and a 0.1-µF bypass capacitor between OUT and GND. The recommendation is to use the high-value capacitor when expecting large-load transients on the output. This trace should be low-impedance to the load.
- Place the resistor used to set the current limit between ILIM and GND. Make sure the traces routing the R_{ILIM} resistor to the device are as short as possible to reduce parasitic effects on the current limit accuracy.

11.2 Layout Example

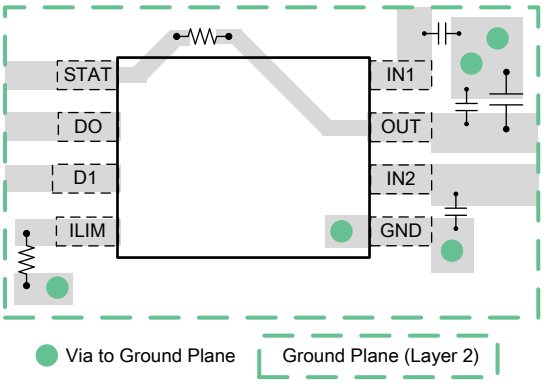


Figure 24. TPS2115A-Q1 Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

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All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2115AIPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	2115AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS2115A-Q1 :

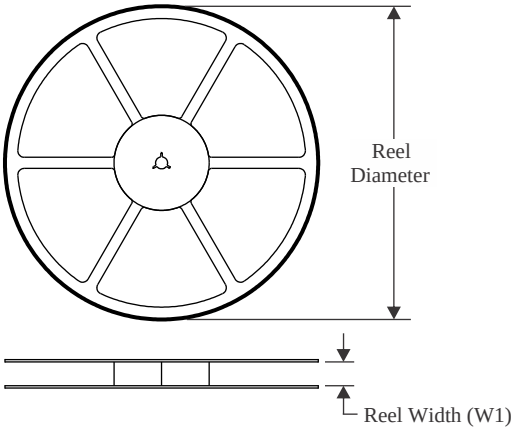
- Catalog: TPS2115A

NOTE: Qualified Version Definitions:

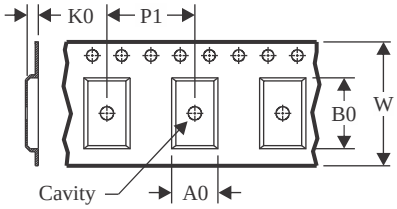
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

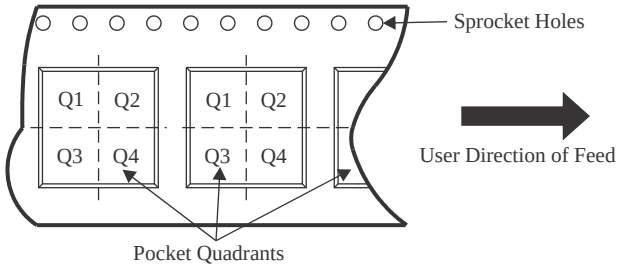


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

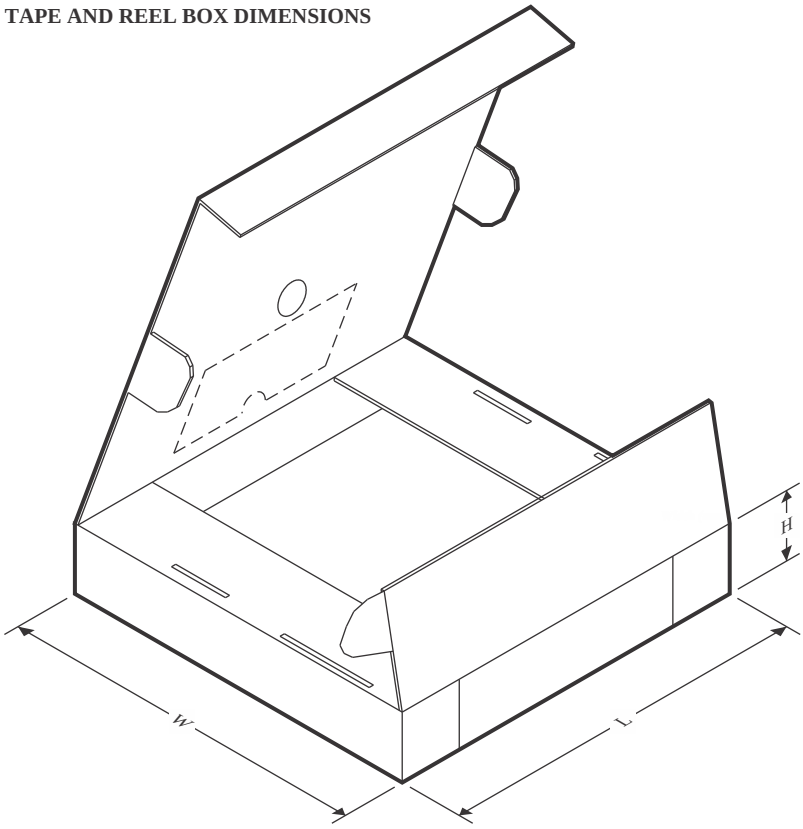
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2115AIPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

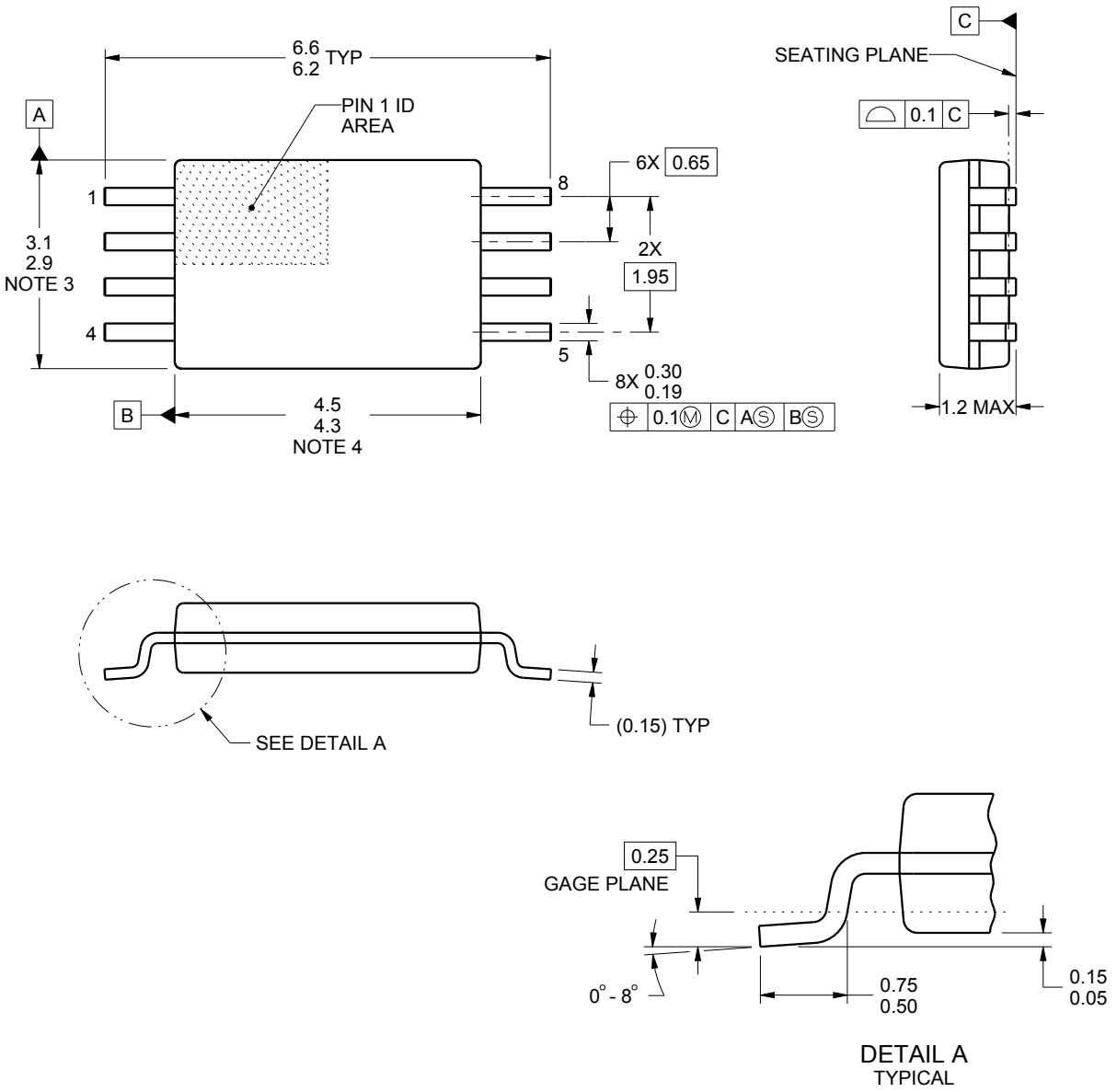
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2115AIPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0008A

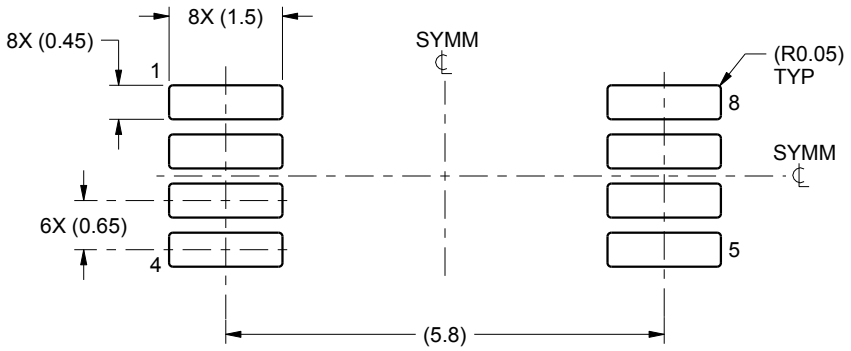
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

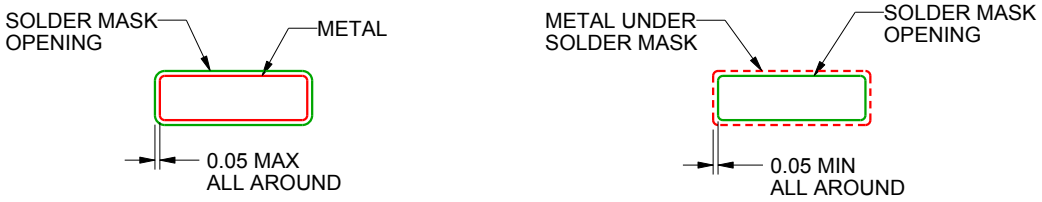


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

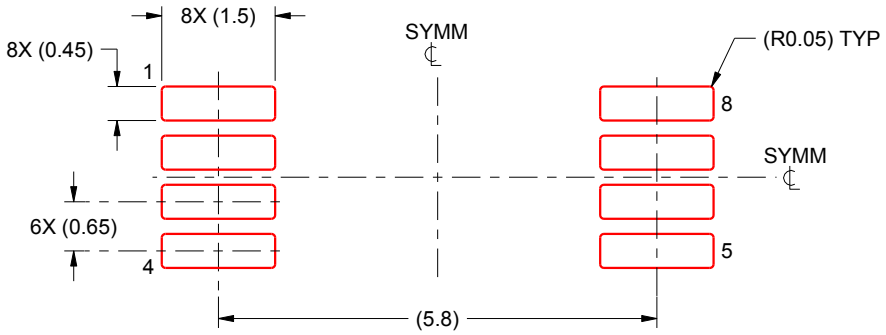


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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