PCN Number:	20200203003	PCN Date:	Mar. 4, 2020
Title:	Datasheet for DP83867IR, DP83867CR		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:		
☐ Assembly Site	☐ Design	☐ Wafer Bump Site
☐ Assembly Process	☒ Data Sheet	☐ Wafer Bump Material
☐ Assembly Materials	☐ Part number change	☐ Wafer Bump Process
☐ Mechanical Specification	☐ Test Site	☐ Wafer Fab Site
☐ Packing/Shipping/Labeling	☐ Test Process	☐ Wafer Fab Materials
		☐ Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DP83867IR, DP83867CR

SNLS484F – FEBRUARY 2015 – REVISED DECEMBER 2019

Changes from Revision E (March 2017) to Revision F	Page
• Added "Time Sensitive Network (TSN) Compliant" to Features	1
• Changed "Fast Link up / Link Drop Modes" to "Fast Link Drop Mode" in Features	1
• Added "Field Bus Support" to Applications	1
• Deleted "NOTE: Internal Pull-Up/Pull-Down resistors on the IO pins are disabled when the device enters functional mode after power up." from Pin Functions	10
• Changed 'TX_EN / TX_CTRL' pin type in Pin Functions	11
• Added XI pin voltage ratings to Absolute Maximum Ratings	14
• Added XI Input Voltage section to Electrical Characteristics	15
• Changed links to RGMII timing diagrams in RGMII Timing (4)	18
• Changed T_{holdR} parameter description in RGMII Timing (4)	18
• Added table note explaining how Duty Cycle % must be interpreted in RGMII Timing (4)	18
• Added table note explaining how Duty Cycle % must be interpreted in RGMII Timing (4)	18
• Changed Figure 10	23
• Changed statement about PHY address in Serial Management Interface	37
• Added Figure 23	41
• Deleted "The BIST allows full control of the packet lengths and of the IPG." from BIST Configuration	43
• Deleted mention of ALCD from Cable Diagnostics	43
• Deleted subsection describing ALCD from Cable Diagnostics	43
• Changed all mentions of "Fast Link Down" to "Fast Link Drop" in Fast Link Drop (FLD)	44

- Added statement on disabling and re-enabling FLD in Fast Link Drop (FLD) 44
- Added statement on effects of pin strapping to FLD configuration in Fast Link Drop (FLD) 44
- Added sentence about the polarity of MDI signals in Mirror Mode 45
- Changed notes after Table 5 to be table notes referenced within the table. 50
- Added definition for register Bit Name type 'Strap' in Register Maps 56
- Deleted Advanced Link Cable Diagnostics Control Register (ALCD_CTRL) 56
- Added PAP package default for '1000BASE-T FULL DUPLEX' in 1000BASE-T Configuration Register (CFG1) 66
- Changed 'MDI_CROSSOVER' default in PHY Control Register (PHYCR) 69
- Added PAP package default for 'SPEED_OPT_EN' in Configuration Register 2 (CFG2) 76
- Added Robust Auto MDIX Timer Configuration Register (AMDIX_TMR_CFG) 85
- Changed descriptions of 'FORCE_DROP' and 'FLD_EN' in Fast Link Drop Configuration Register (FLD_CFG) 86
- Added Fast Link Drop Threshold Configuration Register (FLD_THR_CFG) 87
- Added 'INT_TST_MODE_1' to Configuration Register 4 (CFG4) 87
- Changed 'PORT_MIRROR_EN' default in Configuration Register 4 (CFG4) 87
- Added PAP package default for 'RGMII_EN' in RGMII Control Register (RGMIICTL) 87
- Added Viterbi Module Configuration (VTM_CFG) 90
- Changed description of 'STRAP_FLD' from "Fast Link Detect" to "Fast Link Drop" in Strap Configuration Status Register 2 (STRAP_STS2) 92
- Added BIST Control and Status Register 3 (BICSR3) 93
- Added BIST Control and Status Register 4 (BICSR4) 93
- Added RGZ package default for 'RGMII_TX_DELAY_CTRL' in RGMII Delay Control Register (RGMIIDCTL) 94
- Added RGZ package default for 'RGMII_RX_DELAY_CTRL' in RGMII Delay Control Register (RGMIIDCTL) 94
- Added PLL Clock-out Control Register (PLLCTL) 94
- Added DSP Feedforward Equalizer Configuration (DSP_FFE_CFG) 95
- Added Programmable Gain Register (PROG_GAIN) 114
- Changed capacitor value in Figure 31 and added footnotes 117
- Added requirements for 2.5-V clock source capacitors in Clock In (XI) Recommendation 119
- Added Figure 33 119
- Added "RMS Jitter" to Table 131 119
- Added Clock Out (CLK_OUT) Phase Noise 121
- Changed capacitor placement in Figure 36 and footnote about decoupling capacitor placement 123
- Changed capacitor placement in Figure 37 and footnote about decoupling capacitor placement 124

The datasheet number will be changing.

Device Family	Change From:	Change To:
DP83867IR, DP83867CR	SNLS484E	SNLS484F

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DP83867IR

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DP83867CRRGZR	DP83867CRRGZT	DP83867IRPAPR	DP83867IRPAPT
DP83867IRRGZR	DP83867IRRGZT		

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