Bulletin #1409081

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Bulletin Date: 9/8/2014	**Bulletin Effective Date:** 9/8/2014	
Title: C8051F55x_C8051F56x_C8051F57x_Rev1.2_Data_Sheet_Product_Change_Notice		
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Bulletin Details

Description:
Silicon Labs is pleased to announce that version 1.2 of the C8051F55x/56x/57x data sheet is now available. The revision includes:

Power-On Reset may fail for devices shipped prior to date code 1124

- Added a note regarding an issue with /RST low time on some older devices to "Power-On Reset" on page 140.

This issue was previously documented in the errata and has now been moved to the data sheet. It has been removed from the errata.

Note: For devices with a date code before year 2011, work week 24 (1124), if the /RST pin is held low for more than 1 second while power is applied to the device, and then /RST is released, a percentage of devices may lock up and fail to execute code. Toggling the /RST pin does not clear the condition. The condition is cleared by cycling power. Most devices that are affected will show the lock up behavior only within a narrow range of temperatures (a 5 to 10 degrees C window). Parts with a date code of year 2011, work week 24 (1124) or later do not have any restrictions on /RST low time. The date code of a device is a four-digit number on the bottom-most line of each device with the format YYWW, where YY is the two-digit calendar year and WW is the two digit work week.

Use VDD Monitor low threshold setting during normal operation

– Added the note regarding the voltage regulator and VDD monitor in the high setting from "Power-Fail Reset/VDD Monitor" on page 140 to "Voltage Regulator (REG0)" on page 80 and "VDD Maintenance and the VDD monitor" on page 130.

This note already existed in the data sheet in the Reset Sources chapter, and it's been added to additional locations to make it more prominent.

Note: The output of the internal voltage regulator is calibrated by the MCU immediately after any reset event. The output of the un-calibrated internal regulator could be below the high threshold setting of the VDD Monitor. If this is the case and the VDD Monitor is set to the high threshold setting and if the MCU receives a non-power on reset (POR), the MCU will remain in reset until a POR occurs (i.e., VDD Monitor will keep the device in reset). A POR will force the VDD Monitor to the low threshold setting which is guaranteed to be below the un-calibrated output of the internal regulator. The device will then exit reset and resume normal operation. It is for this reason Silicon Labs strongly recommends that the VDD Monitor is always left in the low threshold setting (i.e. default value upon POR).

Use VDD Monitor high setting only when writing Flash

– Updated step 4 in "VDD Maintenance and the VDD monitor" on page 130 to mention using the VDD monitor in the high setting during flash write/erase operations.

This step previously mentioned using the VDD monitor, but did not specify that the VDD monitor must be in the high setting in order to write to flash.

Note: When programming the Flash in-system, the VDD Monitor must be set to the high threshold setting. For the highest system reliability, the time the VDD Monitor is set to the high threshold setting should be
minimized (e.g., setting the VDD Monitor to the high threshold setting just before the Flash write operation
and then changing it back to the low threshold setting immediately after the Flash write operation).

Set ZTCEN before entering oscillator suspend

– Updated the SUSPEND bit description in OSCICN (SFR Definition 18.2) to mention that firmware must set the ZTCEN bit in REF0CN (SFR Definition 7.1) before entering suspend.

This information was already present as a note in section 15.3 Suspend Mode, and it's been added to the bit description to make it more prominent.

> ZTCEN Zero Temperature Coefficient Bias Enable
> Bit.
> This bit must be set to 1b before entering
> oscillator suspend mode.

IFRDY flag does not accurately reflect the state of the oscillator

– Added a note to the IFRDY flag in the OSCICN register (SFR Definition 18.2) that the flag may not accurately reflect the state of the oscillator.

> IFRDY Internal Oscillator Frequency Ready Flag.
> Note: This flag may not accurately reflect the state of the oscillator. Firmware should not use this flag to determine if the oscillator is running.

VREGIN ramp time max 1 ms for power on specification

– Added VREGIN Ramp Time max 1 ms for Power On spec to Table 5.4, "Reset Electrical Characteristics," on page 41.

– Updated "VDD Maintenance and the VDD monitor" on page 130 to refer to 1 ms VREGIN ramp time instead of 1 ms VDD ramp time.

This specification was previously mentioned in the Flash Write and Erase Guidelines section. It is now added to the electrical specifications to make it more prominent.

Limited cold programming temperature range for industrial grade (-I) devices

– Added a note regarding programming at cold temperatures on –I devices to "Programming The Flash Memory" on page 125 and added Temperature during Programming Operations specification to Table 5.5, "Flash Electrical Characteristics," on page 41.

This specification was previously documented in the errata and has now been moved to the data sheet. It has been removed from the errata.
For –I (Industrial Grade) parts, parts programmed at a cold temperature below 0 °C may exhibit weakly programmed flash memory bits. If programmed at 0 °C or higher, there is no problem reading Flash across the entire temperature range of -40 °C to 125 °C. This temperature restriction does not apply to –A (Automotive Grade) devices.

VREF pin cannot operate as open-drain when VDD selected as reference source

– Added a note regarding P0.0/VREF when VDD is used as the reference to Table 19.1, "Port I/O Assignment for Analog Functions," on page 172 and to the description of the REFSL bit in REF0CN (SFR Definition 7.1).

This issue was previously documented in the errata and has now been moved to the data sheet. It has been removed from the errata.

> If VDD is selected as the voltage reference in the REF0CN register and the ADC is enabled in the ADC0CN register, the P0.0/VREF pin cannot operate as a general purpose I/O pin in open-drain mode. With the above settings, this pin can operate in push-pull output mode or as an analog input.

GPIO may have indeterminate state for fast VIO ramp

– Added a note regarding a potential unknown state on GPIO during power up if VIO ramps significantly before VDD to "Port Input/Output" on page 170 and "Reset Sources" on page 139.

Note: When VIO rises faster than VDD, which can happen when VREGIN and VIO are tied together, a delay created between GPIO power (VIO) and the logic controlling GPIO (VDD) results in a temporary unknown state at the GPIO pins. When VIO rises faster than VDD, the GPIO may enter the following states: floating, glitch low, or glitch high. Cross coupling VIO and VDD with a 4.7 µF capacitor mitigates the root cause of the problem by allowing VIO and VDD to rise at the same rate.

Set FLEWT bit before writing or erasing flash

– Added steps to set the FLEWT bit in the FLSCL register (SFR Definition 14.3) in the flash write/erase procedures in "Flash Erase Procedure" on page 126, "Flash Write Procedure" on page 126, and "Flash Write Optimization" on page 127.

This requirement was previously documented in the bit description for the FLEWT bit, and it's been added to the procedures to make it more prominent.

> FLEWT Flash Erase Write Time Control.
> This bit should be set to 1b before Writing or Erasing Flash.
> 0: Short Flash Erase / Write Timing.
> 1: Extended Flash Erase / Write Timing.

VDD monitor may trigger on fast VDD changes

– Added a note regarding fast changes on VDD causing the VDD Monitor to trigger to “Power-Fail Reset/VDD Monitor” on page 140.

Note: The VDD Monitor may trigger on fast changes in voltage on the VDD pin, regardless of whether the voltage increased or decreased.

UART TX THRE0 bit may return incorrect status

– Added notes regarding UART TX and RX behavior in “Data Transmission” on page 239, “Data Reception” on page 239, and the THRE0 description in the SCON0 register (SFR Definition 23.1).

Note: THRE0 can have a momentary glitch high when the UART Transmit Holding Register is not empty. The glitch will occur sometime after SBUF0 was written with the previous byte and does not occur if THRE0 is checked in the instruction(s) immediately following the write to SBUF0. When firmware writes SBUF0 and SBUF0 is not empty, TX0 will be stuck low until the next device reset. Firmware should use or poll on TI0 rather than THRE0 for asynchronous UART writes that may have a random delay in between transactions.

UART RX may overrun on simultaneous FIFO read/write

– Added notes regarding UART TX and RX behavior in “Data Transmission” on page 239, “Data Reception” on page 239, and the THRE0 description in the SCON0 register (SFR Definition 23.1).

Note: The UART Receive FIFO pointer can be corrupted if the UART receives a byte and firmware reads a byte from the FIFO at the same time. When this occurs, firmware will lose the received byte and the FIFO receive overrun flag (OVR0) will also be set to 1. Systems using the UART Receive FIFO should ensure that the FIFO isn’t accessed by hardware and firmware at the same time. In other words, firmware should ensure to read the FIFO before the next byte is received.

Reason:
Clarification of device behavior and inclusion of data sheet version 1.1 errata.

Product Identification:

C8051F550-IM	C8051F550-IMR
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Customer Actions Needed:
Review latest revision of the data sheet.

