NXP Semiconductors
Data Sheet: Technical Data

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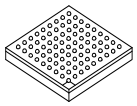
MCIMX6Q5ExxxxD
MCIMX6Q7CxxxxD
MCIMX6Q5ExxxxE
MCIMX6Q7CxxxxE
MCIMX6D5ExxxxD
MCIMX6D7CxxxxD
MCIMX6D5ExxxxE
MCIMX6D7CxxxxE

i.MX 6Dual/6Quad Applications Processors Consumer - PoP



Package Information
Plastic Package
12 x 12 mm, 0.4 mm pitch

Ordering Information
See Table 1

1 Introduction

The i.MX 6Dual/6Quad processors are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The i.MX 6Dual/6Quad processors feature advanced implementation of the quad Arm® Cortex®-A9 core, which operates at speeds up to 800 MHz. They include 2D and 3D graphics processors, 1080p video processing, and integrated power management. Each processor provides a 2 × 32-bit LPDDR2-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth®, GPS, hard drive, displays, and camera sensors.

The i.MX 6Dual/6Quad processors are specifically useful for applications such as the following:

- High-end mobile Internet devices (MID)
- High-end PDAs
- High-end portable media players (PMP) with HD video capability

- Gaming consoles
- Portable navigation devices (PND)

The i.MX 6Dual/6Quad processors offers numerous advanced features, such as:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. The Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon® MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES .0 3D graphics accelerator with four shaders (up to MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, SATA-II, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on nxp.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see nxp.com/imx6series or contact your NXP representative.

Table 1. Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed Grade	Temperature Grade	Package
MCIMX6Q5EZK08AD	i.MX 6Quad	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q5EZK08AE	i.MX 6Quad	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q7CZK08AD	i.MX 6Quad	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q7CZK08AE	i.MX 6Quad	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D5EZK08AD	i.MX 6Dual	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D5EZK08AE	i.MX 6Dual	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D7CZK08AD	i.MX 6Dual	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D7CZK08AE	i.MX 6Dual	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)

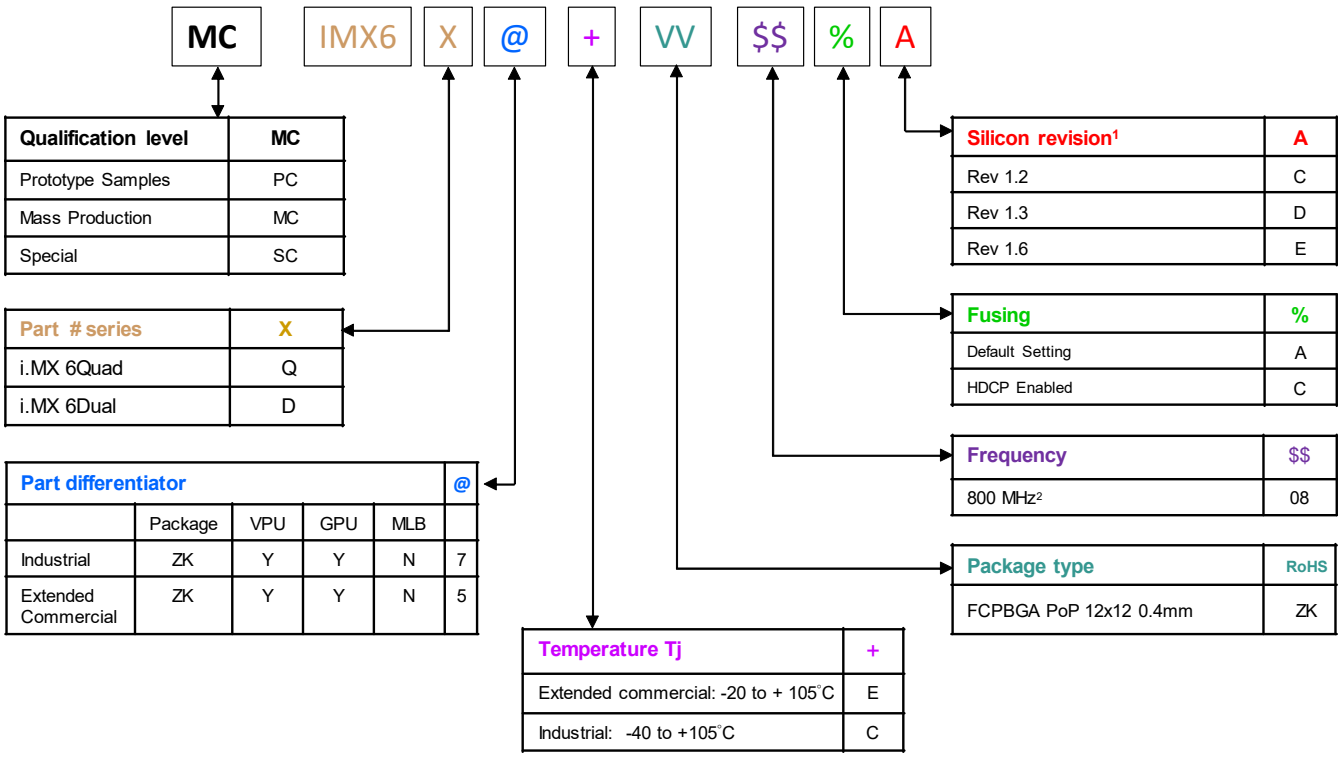
Figure 1 describes the part number nomenclature to identify the characteristics of the specific part number you have (for example, cores, frequency, temperature grade, fuse options, silicon revision). Figure 1 applies to the i.MX 6Dual/6Quad.

The two characteristics that identify which data sheet a specific part applies to are the part number series field and the temperature grade (junction) field:

- The i.MX 6Dual/6Quad Automotive and Infotainment Applications Processors data sheet (IMX6DQAEC) covers parts listed with “A (Automotive temp)”
- The i.MX 6Dual/6Quad Applications Processors for Consumer Products data sheet (IMX6DQCEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)”

- The i.MX 6Dual/6Quad Applications Processors for Consumer Products data sheet (IMX6DQCPOPEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)” and that uses the Package-on-Package.
- The i.MX 6Dual/6Quad Applications Processors for Industrial Products data sheet (IMX6DQIEC) covers parts listed with “C (Industrial temp)”

Ensure that you have the right data sheet for your specific part by checking the temperature grade (junction) field and matching it to the right data sheet. If you have questions, see nxp.com/imx6series or contact your NXP representative.



1. See the nxp.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.

Figure 1. Part Number Nomenclature—i.MX 6Dual PoP and 6Quad PoP

1.2 Features

The i.MX 6Dual/6Quad processors are based on Arm Cortex-A9 MPCore platform, which has the following features:

- Arm Cortex-A9 MPCore 4xCPU processor (with TrustZone®)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The Arm Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 6.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
- Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 2 × 32-bit, LPDDR2-800 channels supporting DDR interleaving mode
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps
- Displays—Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 170 Mpixels/sec (for example, WUXGA at 60 Hz) or two ports up to 85 MP/sec each
  - HDMI 1.4 port
  - MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
  - Parallel Camera port (up to 20 bit and up to 240 MHz peak)

  - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6Dual/6Quad processor has four lanes.
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed PHY
    - Two HS hosts with integrated High Speed Inter-Chip (HS-IC) USB PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - SSI block capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - ESAI is capable of supporting audio sample frequencies up to 260 kHz in I2S mode with 7.1 multi channel outputs
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while the other four support 4-wire. This is due to the SoC IOMUX limitation, because all UART IPs are identical.
  - Five eCSPI (Enhanced CSPI)
  - Three I2C, supporting 400 kbps
  - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
  - Two Controller Area Network (FlexCAN), 1 Mbps each
  - Two Watchdog timers (WDOG)

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

— Audio MUX (AUDMUX)

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for Arm and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPUs)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES .0)
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- Arm TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

1.3 Signal Naming Convention

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Standardized Signal Name Map* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

The signal names of the i.MX6 series of products are standardized to align the signal names within the family and across the documentation. Benefits of this standardization are as follows:

- Signal names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- Signal names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This standardization applies only to signal names. The ball names are preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

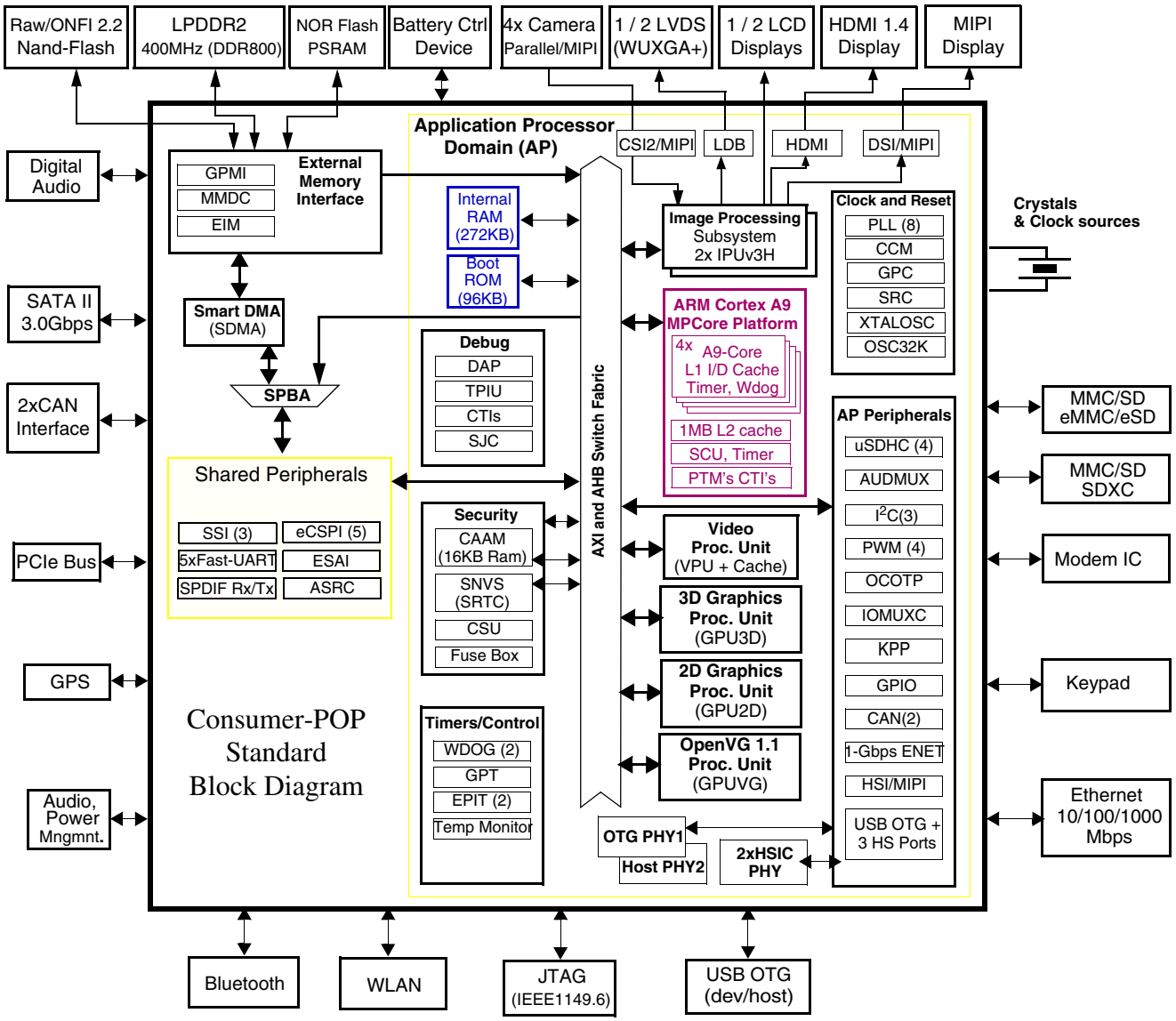


Figure 2. i.MX 6Dual/6QuadConsumer Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6Dual/6Quad processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Dual/6Quad Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
512 x 8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Dual/6Quad processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	System Control Peripherals	DMA controller used for GPMI2 operation.
Arm	Arm Platform	Arm	The Arm Cortex-A9 platform consists of 4x (four) Cortex-A9 cores version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC error correction for NAND Flash controller (GPMI).
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Dual/6Quad processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	MIPI CSI-2 Interface	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports up to 1 Gbps for up to 3 data lanes and up to 800 Mbps for 4 data lanes.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Dual/6Quad platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Dual/6Quad processor has two such modules, one for each IPU.
DSI	MIPI DSI interface	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
eCSPI1-5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX 6Dual/6Quad processors also consist of hardware assist for IEEE 1588 standard. For details, see the ENET chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM). **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC error correction for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver. 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPU3Dv4	Graphics Processing Unit-3D, ver. 4	Multimedia Peripherals	The GPU2Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports dual x32 for LPDDR2-800 • Supports up to 4 GByte DDR memory space

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controllers.
ROM 96 KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 MHz • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6Dual/6Quad specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Conforms to the SD Host Controller Standard Specification version 3.0 • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC-level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card Detection” and “Write Protection” pads and do not support hardware reset. • Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
VDOA	VDOA	Multimedia Peripherals	The Video Data Order Adapter (VDOA) is used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for complete list of VPU’s decoding/encoding capabilities.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual (IMX6DQRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused analog interfaces," of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Dual/6Quad processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the SoC. See Table 3 for a quick reference to the individual tables and sections.

Table 3. i.MX 6Dual/6Quad Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 20
PoP Package Thermal Resistance	on page 21
Operating Ranges	on page 22
External Clock Sources	on page 24
Maximum Measured Supply Currents	on page 26
Low Power Mode Supply Currents	on page 27
USB PHY Current Consumption	on page 29
SATA Typical Power Consumption	on page 29
PCIe 2.0 Maximum Power Consumption	on page 30
HDMI Maximum Power Consumption	on page 31

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 4 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply input voltage (LDO enabled)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.6	V
Core supply input voltage (LDO bypass)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.4	V
Core supply output voltage (LDO enabled)	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP NVCC_PLL_OUT	-0.3	1.4	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.7	V
DDR I/O supply voltage	NVCC_DRAM	-0.4	1.975 (See note 1)	V
GPIO I/O supply voltage	NVCC_CSI NVCC_EIM NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD NVCC_JTAG	-0.5	3.7	V
HDMI, PCIe, and SATA PHY high (VPH) supply voltage	HDMI_VPH PCIE_VPH SATA_VPH	-0.3	2.85	V
HDMI, PCIe, and SATA PHY low (VP) supply voltage	HDMI_VP PCIE_VP SATA_VP	-0.3	1.4	V
LVDS and MIPI I/O supply voltage (2.5V supply)	NVCC_LVDS_2P5 NVCC_MIPI	-0.3	2.85	V
PCIe PHY supply voltage	PCIE_VPTX	-0.3	1.4	V
RGMII I/O supply voltage	NVCC_RGMII	-0.5	2.725	V
SNVS IN supply voltage (Secure Non-Volatile Storage and Real Time Clock)	VDD_SNVS_IN	-0.3	3.4	V
USB I/O supply voltage	USB_H1_DN USB_H1_DP USB_OTG_DN USB_OTG_DP USB_OTG_CHD_B	-0.3	3.73	V
USB VBUS supply voltage	USB_H1_VBUS USB_OTG_VBUS	—	5.35	V
V_{in}/V_{out} input/output voltage range (non-DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.3 (See note 2)	V
V_{in}/V_{out} input/output voltage range (DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.4 (See notes 1 & 2)	V
ESD immunity (HBM)	V_{esd_HBM}	—	2000	V
ESD immunity (CDM)	V_{esd_CDM}	—	500	V
Storage temperature range	$T_{storage}$	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

4.1.2.1 FCPBGA Package Thermal Resistance

4.1.2.2 PoP Package Thermal Resistance

Table 5 provides the PoP package thermal resistance data.

Table 5. PoP Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient[1] (natural convection)	Single layer board (1s)	$R_{\theta JA}$	41	°C/W
	Four layer board (2s2p)	$R_{\theta JA}$	26	°C/W
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	33	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	22	°C/W
Junction to Board[2]	—	$R_{\theta JB}$	13	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	2	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4.1.3 Operating Ranges

Table 6 provides the operating ranges of the i.MX 6Dual/6Quad processors.

Table 6. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN[3]	1.275[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.150 V minimum for operation up to 792 MHz.
		1.05[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.350[4]	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275[4,7]	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed[8]	VDD_ARM_IN VDD_ARM23_IN[3]	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925	—	1.3	V	LDO bypassed for operation up to 396 MHz.
	VDD_SOC_IN	1.225	—	1.3	V	264 MHz < VPU ≤ 352 MHz.
		1.15	—	1.3	V	VPU ≤ 264 MHz.
Standby/DSM Mode	VDD_ARM_IN VDD_ARM23_IN[3]	0.9	—	1.3	V	See Table 9, “Stop Mode Current and Power Consumption,” on page 27.
	VDD_SOC_IN	0.9	—	1.3	V	
VDD_HIGH internal Regulator	VDD_HIGH_IN[9]	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[9]	2.8	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
Supply for RGMII I/O power group[10]	NVCC_RGMII	1.15	—	2.625	V	• 1.15 V – 1.30 V in HSIC 1.2 V mode • 1.43 V – 1.58 V in RGMII 1.5 V mode • 1.70 V – 1.90 V in RGMII 1.8 V mode • 2.25 V – 2.625 V in RGMII 2.5 V mode

Table 6. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
GPIO supplies[10]	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	Isolation between the NVCC_EIMx and NVCC_SDx different supplies allow them to operate at different voltages within the specified range. Example: NVCC_EIM1 can operate at 1.8 V while NVCC_EIM2 operates at 3.3 V.
	NVCC_LVDS_2P5[11] NVCC_MIPI	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.3	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.3	V	—
SATA Supply voltages	SATA_VP	0.99	1.1	1.3	V	—
	SATA_VPH	2.25	2.5	2.75	V	—
Junction temperature Extended Commercial	T_J	-20	—	105	°C	See *i.MX 6Dual/6Quad Product Lifetime Usage Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.
Junction temperature Industrial	T_J	-40	—	105	°C	See *i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 See the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the *_CAP supply outputs.

3 For Quad core system, connect to VDD_ARM_IN. For Dual core system, may be shorted to GND together with VDD_ARM23_CAP to reduce leakage.

4 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

5 VDD_ARM_CAP must not exceed VDD_CACHE_CAP by more than +50 mV. VDD_CACHE_CAP must not exceed VDD_ARM_CAP by more than 200 mV.

6 VDD_SOC_CAP and VDD_PU_CAP must be equal.

7 In LDO enabled mode, the internal LDO output set points must be configured such that the:

VDD_ARM LDO output set point does not exceed the VDD_SOC LDO output set point by more than 100 mV.

VDD_SOC LDO output set point is equal to the VDD_PU LDO output set point.

The VDD_ARM LDO output set point can be lower than the VDD_SOC LDO output set point, however, the minimum output set points shown in this table must be maintained.

[8] In LDO bypassed mode, the external power supply must ensure that VDD_ARM_IN does not exceed VDD_SOC_IN by more than 100 mV. The VDD_ARM_IN supply voltage can be lower than the VDD_SOC_IN supply voltage. The minimum voltages shown in this table must be maintained.

[9] To set VDD_SNVS_IN voltage with respect to Charging Currents and RTC, see the *Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors* (IMX6DQ6SDLHDG).

[10] All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

[11] This supply also powers the pre-drivers of the DDR I/O pins; therefore, it must always be provided, even when LVDS is not used.

4.1.4 External Clock Sources

Each i.MX 6Dual/6Quad processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, that can be used instead of RTC_XTALI when accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration should be given to the timing implications on all of the SoC modules dependent on this clock.

Table 7 shows the interface frequency requirements.

Table 7. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

[1] External oscillator or a crystal with internal oscillator amplifier.

[2] The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 7 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance

  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, an internal ring oscillator is used. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator.
  - If no external crystal is present, then the ring oscillator is used.

The decision to choose a clock source should be based on real-time clock use and precision timeout.

4.1.5 Maximum Measured Supply Currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use case that requires maximum supply current is not a realistic use case.

To help illustrate the effect of the application on power consumption, data was collected while running industry standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Description of test conditions:

- The Power Virus data shown in Table 8 represent a use case designed specifically to show the maximum current consumption possible for the Arm core complex. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited, if any, practical use case, and be limited to an extremely low duty cycle unless the intention was to specifically cause the worst case power consumption.
- EEMBC CoreMark: Benchmark designed specifically for the purpose of measuring the performance of a CPU core. More information available at www.eembc.org/coremark. Note that this benchmark is designed as a core performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a computationally-intensive application rather than the Power Virus.
- 3DMark Mobile 2011: Suite of benchmarks designed for the purpose of measuring graphics and overall system performance. Note that this benchmark is designed as a graphics performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a very graphics-intensive application.
- Devices used for the tests were from the high current end of the expected process variation.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 8, however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for more details on typical power consumption under various use case definitions.

Table 8. Maximum Supply Currents

Power Supply	Conditions	Maximum Current		Unit
		Power Virus	CoreMark	
i.MX 6Quad: VDD_ARM_IN + VDD_ARM23_IN	• ARM frequency = 792 MHz • ARM LDOs set to 1.3V • T_j = 105°C	3270	2090	mA
i.MX 6Dual: VDD_ARM_IN	• ARM frequency = 792 MHz • ARM LDOs set to 1.3V • T_j = 105°C	1960	1250	mA
i.MX 6Dual or i.MX 6Quad: VDD_SOC_IN	• GPU frequency = 600 MHz • SOC LDO set to 1.3 V • T_j = 105°C	2370		mA
VDD_HIGH_IN	—	125[1]		mA
VDD_SNVS_IN	—	275[2]		µA
USB_OTG_VBUS/ USB_H1_VBUS (LDO 3P0)	—	25[3]		mA
Primary Interface (IO) Supplies				
NVCC_DRAM	—	(see note[4])		
NVCC_ENET	N=10	Use maximum IO equation[5]		
NVCC_LCD	N=29	Use maximum IO equation[5]		
NVCC_GPIO	N=24	Use maximum IO equation[5]		
NVCC_CSI	N=20	Use maximum IO equation[5]		
NVCC_EIM0	N=19	Use maximum IO equation[5]		
NVCC_EIM1	N=14	Use maximum IO equation[5]		
NVCC_EIM2	N=20	Use maximum IO equation[5]		
NVCC_JTAG	N=6	Use maximum IO equation[5]		
NVCC_RGMII	N=6	Use maximum IO equation[5]		
NVCC_SD1	N=6	Use maximum IO equation[5]		
NVCC_SD2	N=6	Use maximum IO equation[5]		
NVCC_SD3	N=11	Use maximum IO equation[5]		
NVCC_NANDF	N=26	Use maximum IO equation[5]		
NVCC_MIPI	—	25.5		mA
NVCC_LVDS2P5	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5.		

Table 8. Maximum Supply Currents (continued)

Power Supply	Conditions	Maximum Current		Unit
		Power Virus	CoreMark	
MISC				
DRAM_VREF	—	1		mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

2 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown Table 8. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors such as external signal termination. DRAM power calculators are typically available from memory vendors which take into account factors such as signal termination.
See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note* (AN4509) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 9 shows the current core consumption (not including I/O) of the i.MX 6Dual/6Quad processors in selected low power modes.

Table 9. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• Arm, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.4 V)	6	mA
		VDD_SOC_IN (1.4 V)	23	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_ON	• Arm LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	22	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW

Table 9. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Unit
STOP_OFF	• Arm LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	13.5	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	• Arm and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	13	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	• Arm and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	2	mA
		VDD_HIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors, typical condition. Table 10 shows the USB interface current consumption in power down mode.

Table 10. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 SATA Typical Power Consumption

Table 11 provides SATA PHY currents for certain Tx operating modes.

NOTE

Tx power consumption values are provided for a single transceiver. If T = single transceiver power and C = Clock module power, the total power required for N lanes = N x T + C.

Table 11. SATA PHY Current Drain

Mode	Test Conditions	Supply	Typical Current	Unit
P0: Full-power state[1]	Single Transceiver	SATA_VP	11	mA
		SATA_VPH	13	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	
P0: Mobile[2]	Single Transceiver	SATA_VP	11	mA
		SATA_VPH	11	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	
P0s: Transmitter idle	Single Transceiver	SATA_VP	9.4	mA
		SATA_VPH	2.9	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	

Table 11. SATA PHY Current Drain (continued)

Mode	Test Conditions	Supply	Typical Current	Unit
P1: Transmitter idle, Rx powered down, LOS disabled	Single Transceiver	SATA_VP	0.67	mA
		SATA_VPH	0.23	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	
P2: Powered-down state, only LOS and POR enabled	Single Transceiver	SATA_VP	0.53	mA
		SATA_VPH	0.11	
	Clock Module	SATA_VP	0.036	
		SATA_VPH	0.12	
PDDQ mode[3]	Single Transceiver	SATA_VP	0.13	mA
		SATA_VPH	0.012	
	Clock Module	SATA_VP	0.008	
		SATA_VPH	0.004	

1 Programmed for 1.0 V peak-to-peak Tx level.

2 Programmed for 0.9 V peak-to-peak Tx level with no boost or attenuation.

3 LOW power non-functional.

4.1.9 PCIe 2.0 Maximum Power Consumption

Table 12 provides PCIe PHY currents for certain operating modes.

Table 12. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
P0: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
P0s: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	

Table 12. PCIe PHY Current Drain (continued)

Mode	Test Conditions	Supply	Max Current	Unit
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.1.10 HDMI Maximum Power Consumption

Table 13 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data pattern and Power-down modes.

Table 13. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down	—	HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- The SRC_POR_B signal controls the processor POR and must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and can be powered at any time.

4.2.2 Power-Down Sequence

There are no special restrictions for i.MX 6Dual/6Quad SoC.

4.2.3 Power Supplies Usage

- All I/O pins must not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see the “Power Group” column of Table 85, “12 x 12 mm Functional Contact Assignments”.
- When the SATA interface is not used, the SATA_VP and SATA_VPH supplies should be grounded. The input and output supplies for rest of the ports (SATA_REXT, SATA_PHY_RX_N, SATA_PHY_RX_P, and SATA_PHY_TX_N) can remain unconnected. It is recommended not to turn OFF the SATA_VPH supply while the SATA_VP supply is ON, as it may lead to excessive

power consumption. If boundary scan test is used, SATA_VP and SATA_VPH must remain powered.

- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can remain unconnected. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

Optionally LDO_SOC/VDD_SOC_CAP can be used to power the HDMI, PCIe, and SATA PHY's through external connections.

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1 / NVCC_PLL_OUT

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V

to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the 24 MHz oscillator, PLLs, and USB PHY. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. The LDO_2P5 supplies the SATA PHY, USB PHY, LVDS PHY, HDMI PHY, MIPI PHY, E-fuse module and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 14. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 16. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 17. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 Arm PLL

Table 18. Arm PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux.

Table 19. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA must be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2
- LVDS I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

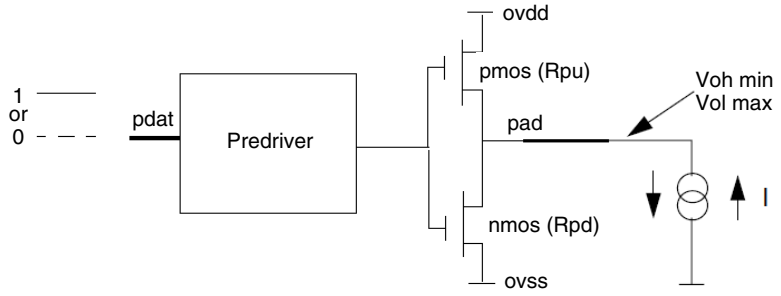


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 20 shows the DC parameters for the clock inputs.

Table 20. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1 (See note 1)	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage current at startup	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 24 MHz clock at 1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 General Purpose I/O (GPIO) DC Parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 21. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage[1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage[1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+[3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–[3, 4]	VT–	—	—	0.5 × OVDD	V

Table 21. GPIO I/O DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1	1	µA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	µA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	µA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	µA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	µA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	175	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2.

4.6.4 RGMII I/O 2.5V I/O DC Electrical Parameters

The RGMII interface complies with the RGMII standard version 1.3. The parameters in Table 22 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 22. RGMII I/O 2.5V I/O DC Electrical Parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1 mA (DSE=001,010) Ioh= -1.0 mA (DSE=011,100,101,110,111)	OVDD-0.15	—	V
Low-level output voltage[1]	V_{OL}	Iol= 0.1 mA (DSE=001,010) Iol= 1.0 mA (DSE=011,100,101,110,111)	—	0.15	V
Input Reference Voltage	V_{ref}	—	0.49xOVDD	0.51xOVDD	V
High-Level input voltage [2, 3]	V_{IH}	—	0.7xOVDD	OVDD	V
Low-Level input voltage [2, 3]	V_{IL}	—	0	0.3xOVDD	V
Input Hysteresis(OVDD=1.8V)	$V_{HYS\_HighVDD}$	OVDD=1.8V	250	—	mV
Input Hysteresis(OVDD=2.5V)	$V_{HYS\_HighVDD}$	OVDD=2.5V	250	—	mV

Table 22. RGMII I/O 2.5V I/O DC Electrical Parameters[1] (continued)

Schmitt trigger VT+ [3, 4]	V_{TH+}	—	0.5xOVDD	—	mV
Schmitt trigger VT- [3, 4]	V_{TH-}	—	—	0.5xOVDD	mV
Pull-up resistor (22 kΩ PU)	R_{PU_22K}	V_{in}=0V	—	212	µA
Pull-up resistor (22 kΩ PU)	R_{PU_22K}	V_{in}=OVDD	—	1	µA
Pull-up resistor (47 kΩ PU)	R_{PU_47K}	V_{in}=0V	—	100	µA
Pull-up resistor (47 kΩ PU)	R_{PU_47K}	V_{in}=OVDD	—	1	µA
Pull-up resistor (100 kΩ PU)	R_{PU_100K}	V_{in}=0V	—	48	µA
Pull-up resistor (100 kΩ PU)	R_{PU_100K}	V_{in}=OVDD	—	1	µA
Pull-down resistor (100 kΩ PD)	R_{PD_100K}	V_{in}=OVDD	—	48	µA
Pull-down resistor (100 kΩ PD)	R_{PD_100K}	V_{in}=0V	—	1	µA
Keeper Circuit Resistance	R_{keep}	—	105	165	kΩ
Input current (no pull-up/down)	I_{in}	V_I = 0,VI = OVDD	-2.9	2.9	µA

1 Input Mode Selection: SW_PAD_CTL_GRP_DDR_TYPE_RGMII = 10 (1.8V Mode)
SW_PAD_CTL_GRP_DDR_TYPE_RGMII = 11 (2.5V Mode).

2 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled (register IOMUXC_SW_PAD_CTL_PAD_RGMII_TXC[HYS]= 0).

4.6.4.1 LPDDR2 Mode I/O DC Parameters

For details on supported DDR memory configurations, see Section 4.10.2, "MMDC Supported LPDDR2 Configurations."

The parameters in Table 23 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 23. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA	0.9 × OVDD	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	0.1 × OVDD	V
Input reference voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	Vref-0.13V	V
Differential Input Logic High	Vih(diff)	—	0.26	See Note [2]	—
Differential Input Logic Low	Vil(diff)	—	See Note [2]	-0.26	—
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.5	2.5	µA

Table 23. LPDDR2 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
Pull-up/pull-down impedance mismatch	MMpupd	—	-15	+15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 27).

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

Table 24 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 24. LVDS I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	V_{OD}	Rload=100 Ω between padP and padN	250	450	mV
Output High Voltage	V_{OH}	I_{OH} = 0 mA	1.25	1.6	V
Output Low Voltage	V_{OL}	I_{OL} = 0 mA	0.9	1.25	
Offset Voltage	V_{OS}	—	1.125	1.375	

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

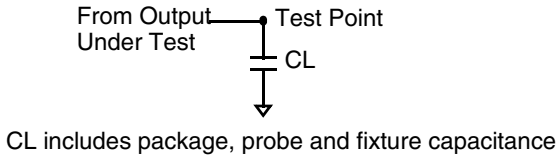


Figure 4. Load Circuit for Output

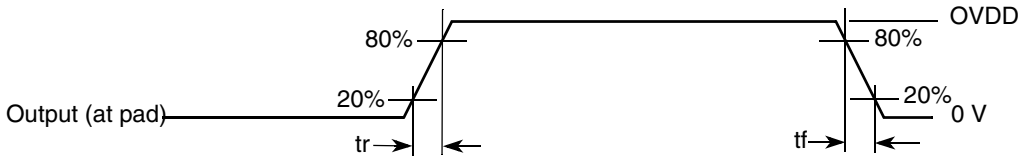


Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 25 and Table 26, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 25. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 26. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

For details on supported DDR memory configurations, see Section 4.10.2, "MMDC Supported LPDDR2 Configurations."

Table 27 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 27. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.2	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

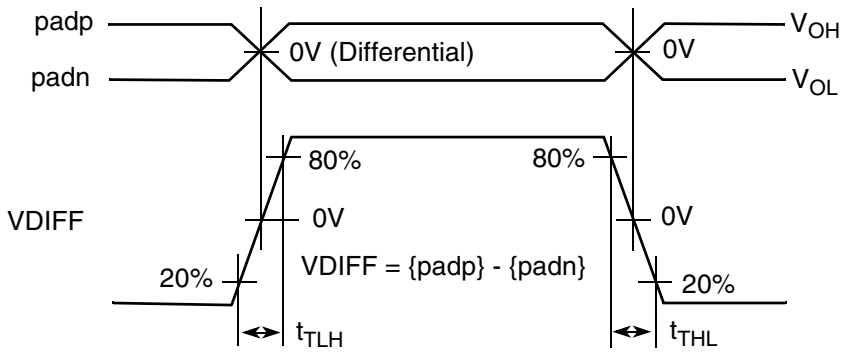


Figure 6. Differential LVDS Driver Transition Time Waveform

Table 28 shows the AC parameters for LVDS I/O.

Table 28. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} – t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20–80% from output voltage.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Dual/6Quad processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

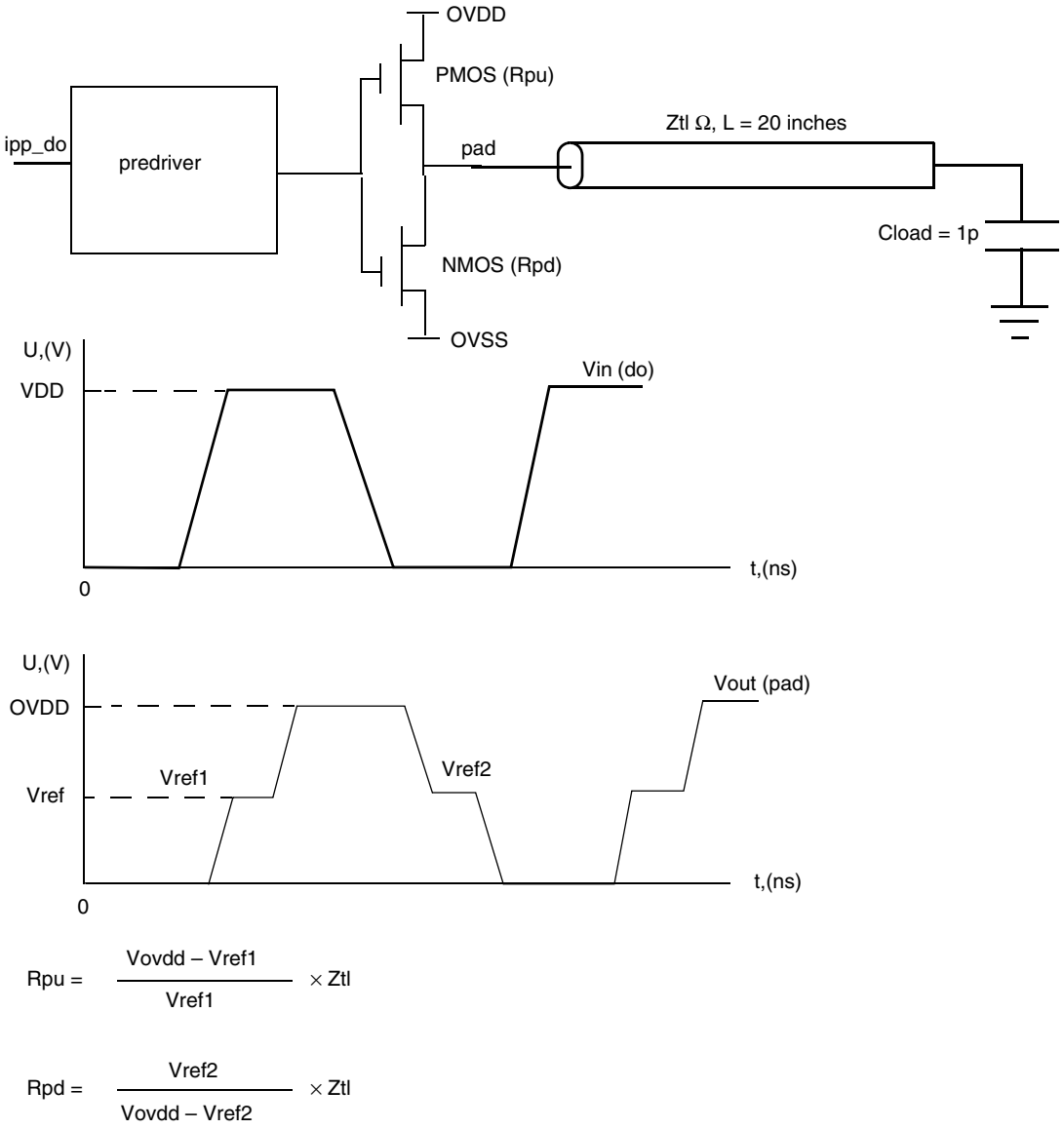


Figure 7. Impedance Matching Load for Measurement

4.8.1 GPIO Output Buffer Impedance

Table 29 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 29. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 30 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 30. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see Section 4.10.2, "MMDC Supported LPDDR2 Configurations."

Table 31 shows DDR I/O output buffer impedance of i.MX 6Dual/6Quad processors.

Table 31. LPDDR2 I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical NVCC_DRAM=1.2 V DDR_SEL=10	Unit
Output Driver Impedance	Rdrv	Drive Strength (DSE) = 000 001 010 011 100 101 110 111	 Hi-Z 240 120 80 60 48 40 34	Ω

Note:
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Dual/6Quad processor.

4.9.1 Reset Timing Parameters

Figure 8 shows the reset timing and Table 32 lists the timing parameters.

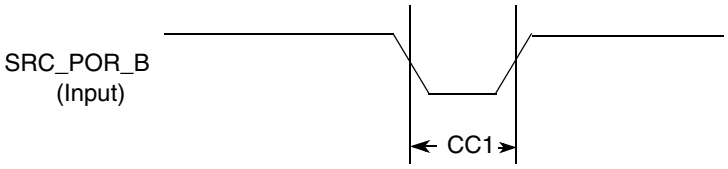


Figure 8. Reset Timing Diagram

Table 32. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid	1	—	XTALOSC_RTC_ XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 33 lists the timing parameters.

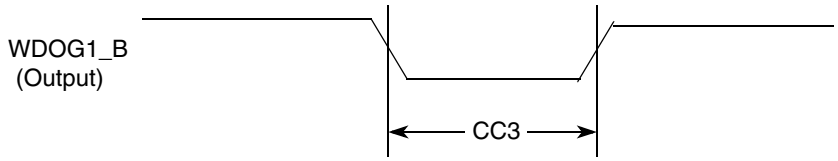


Figure 9. WDOG1_B Timing Diagram

Table 33. WDOG1_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	XTALOSC_RTC_ XTALI cycle

NOTE

XTALOSC_RTC_XTALI is approximately 32 kHz.
XTALOSC_RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 34 provides EIM interface pads allocation in different modes.

Table 34. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

[1] For more information on configuration ports mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 35 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

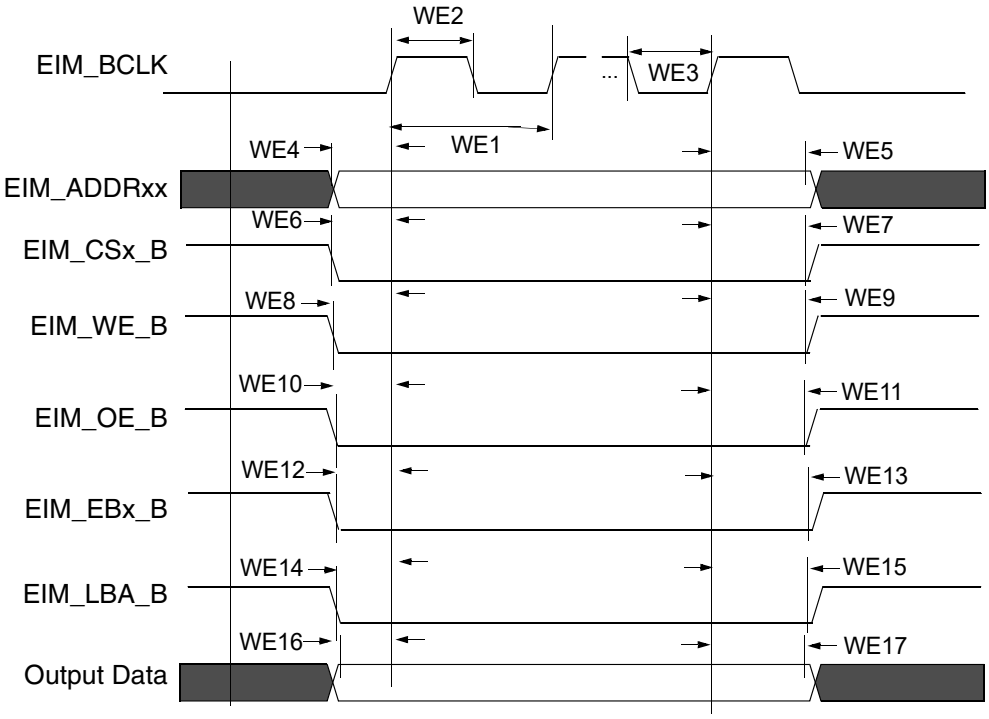


Figure 10. EIM Output Timing Diagram

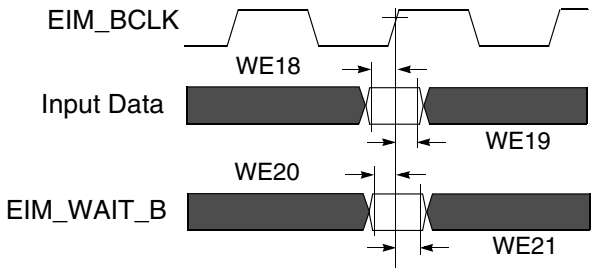


Figure 11. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 35. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns

Table 35. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE4	Clock rise to address valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE5	Clock rise to address invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE8	Clock rise to EIM_WE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE9	Clock rise to EIM_WE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE11	Clock rise to EIM_OE_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE12	Clock rise to EIM_EBx_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) - 1.25	-0.5 × t × (k+1) + 2.25	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) - 1.25	0.5 × t × (k+1) + 2.25	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

1 k represents register setting BCD value.

2 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

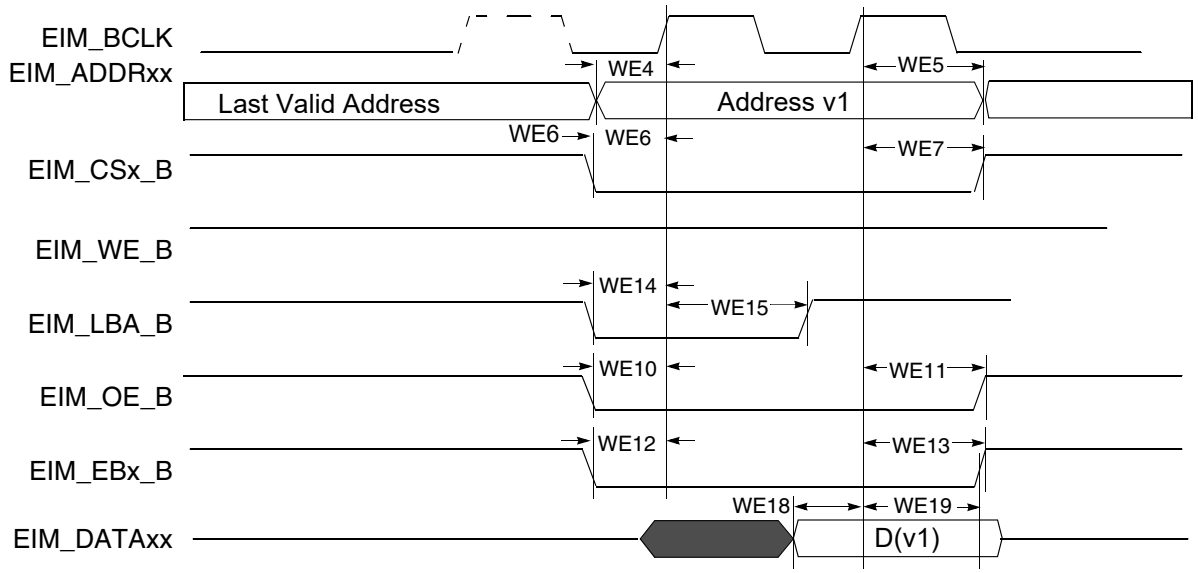


Figure 12. Synchronous Memory Read Access, WSC=1

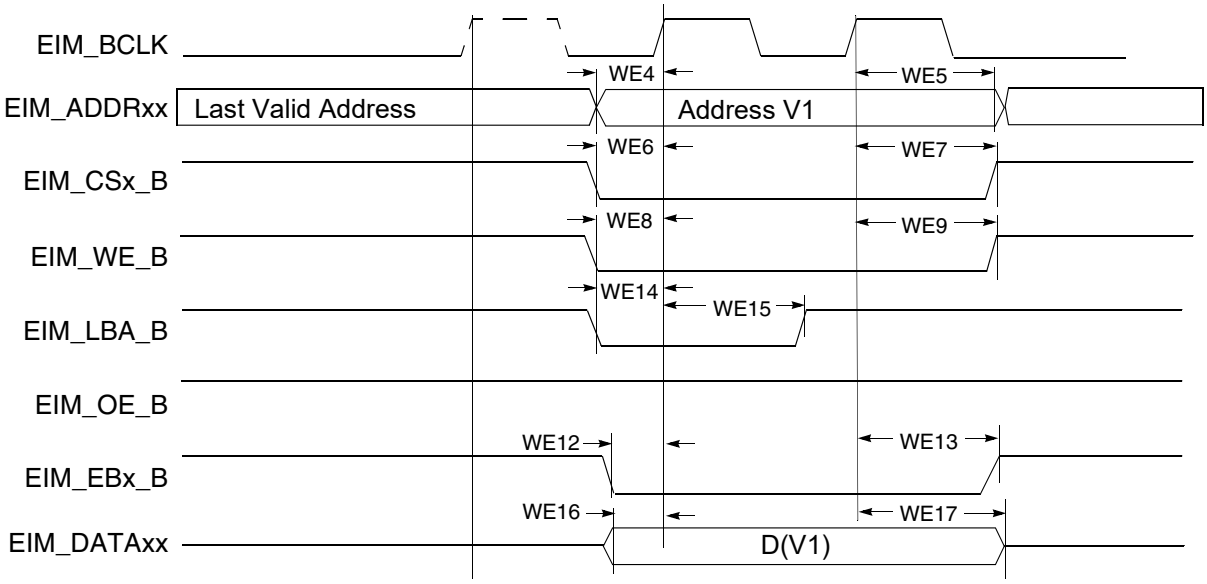


Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

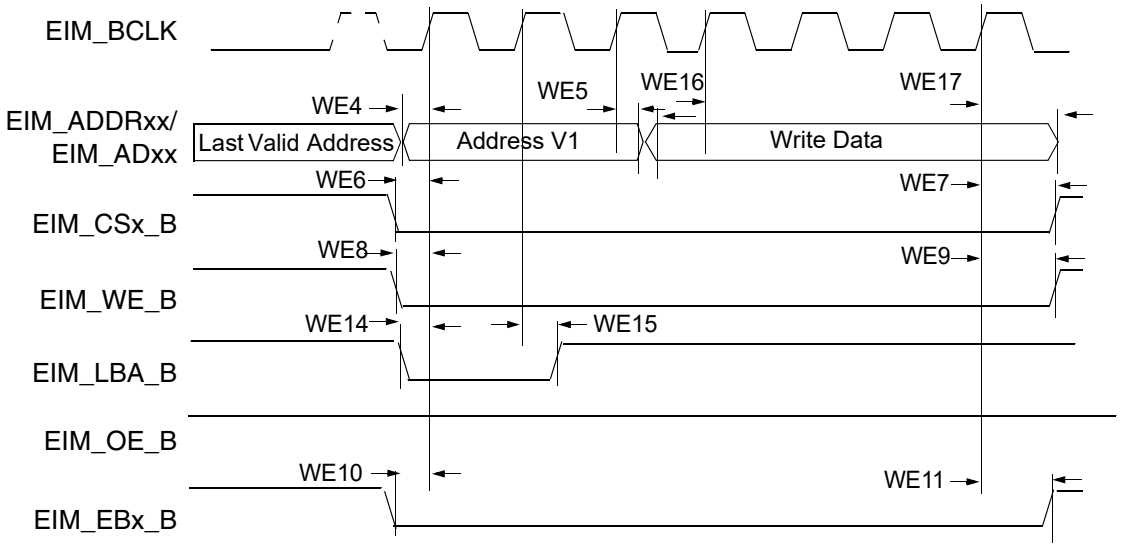


Figure 14. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

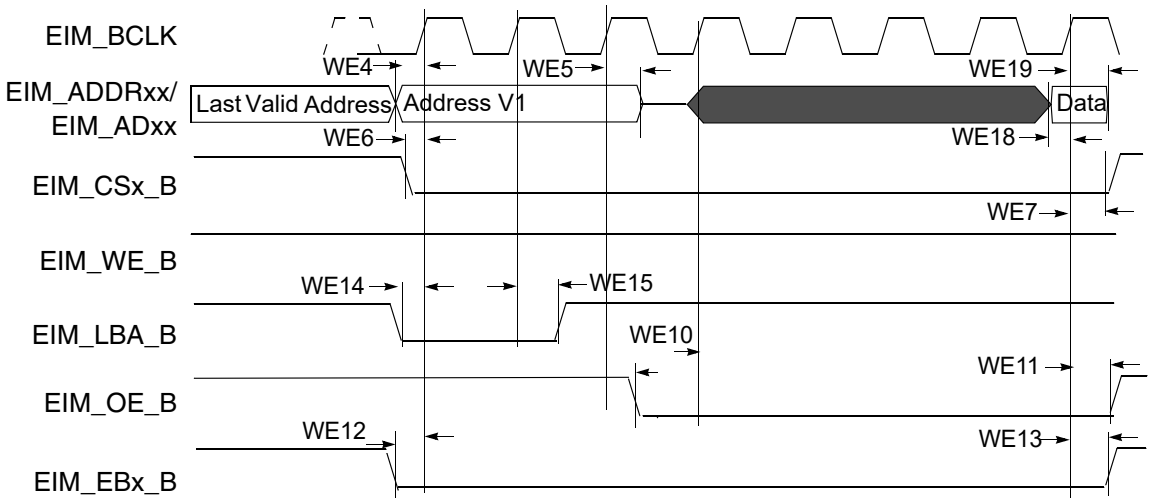


Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20 and Table 36 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for the EIM programming model.

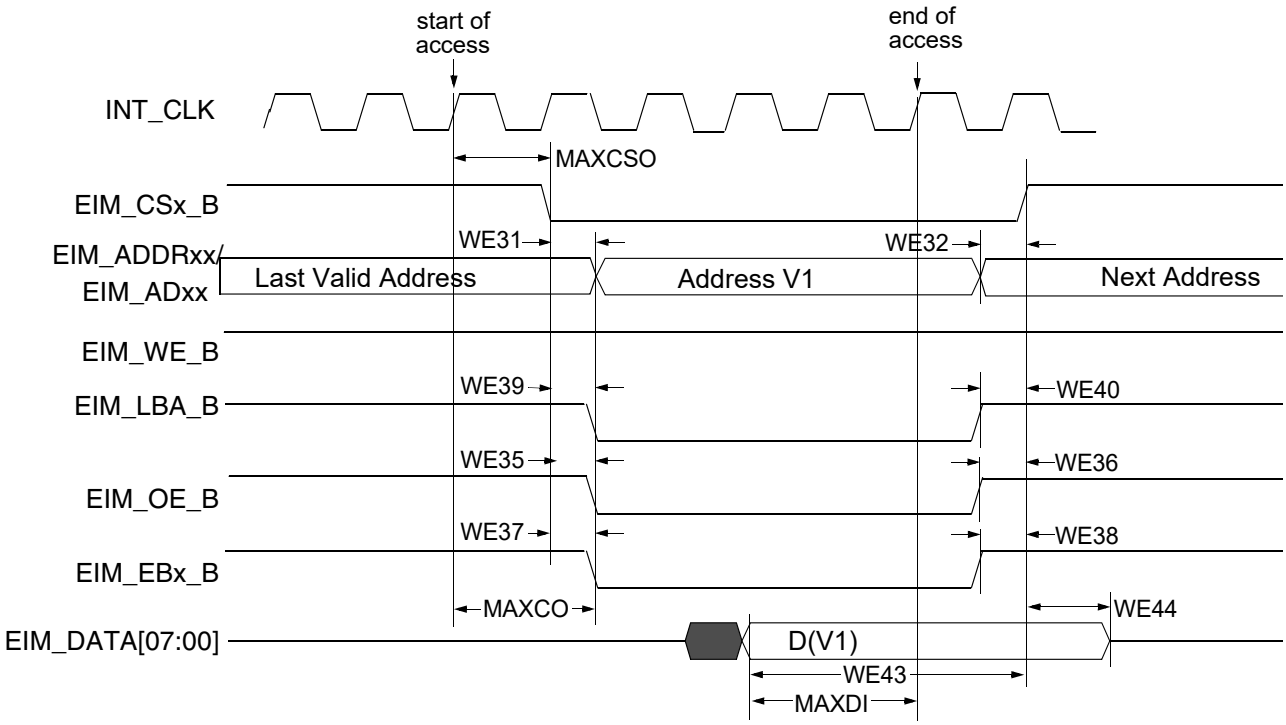


Figure 16. Asynchronous Memory Read Access (RWSC = 5)

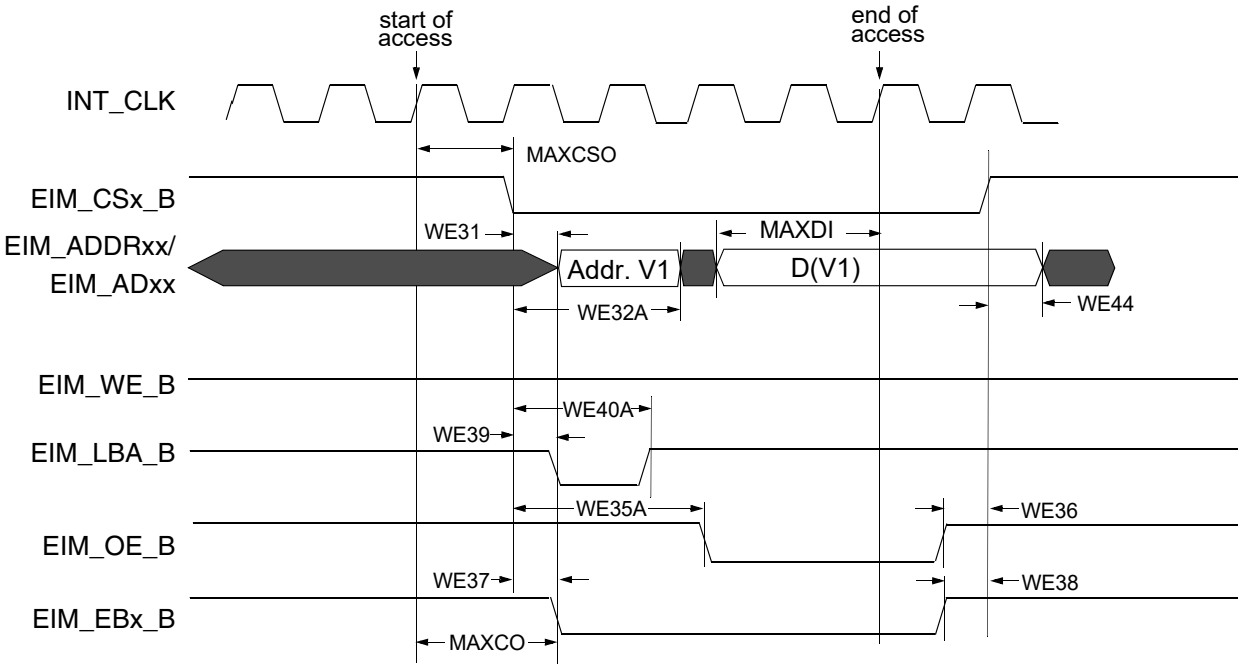


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

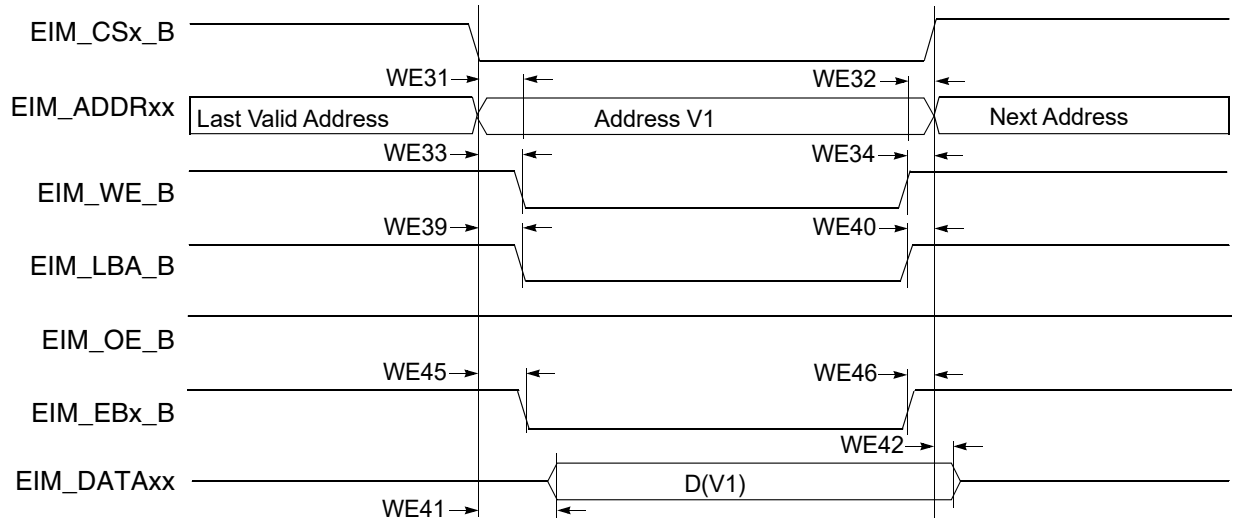


Figure 18. Asynchronous Memory Write Access

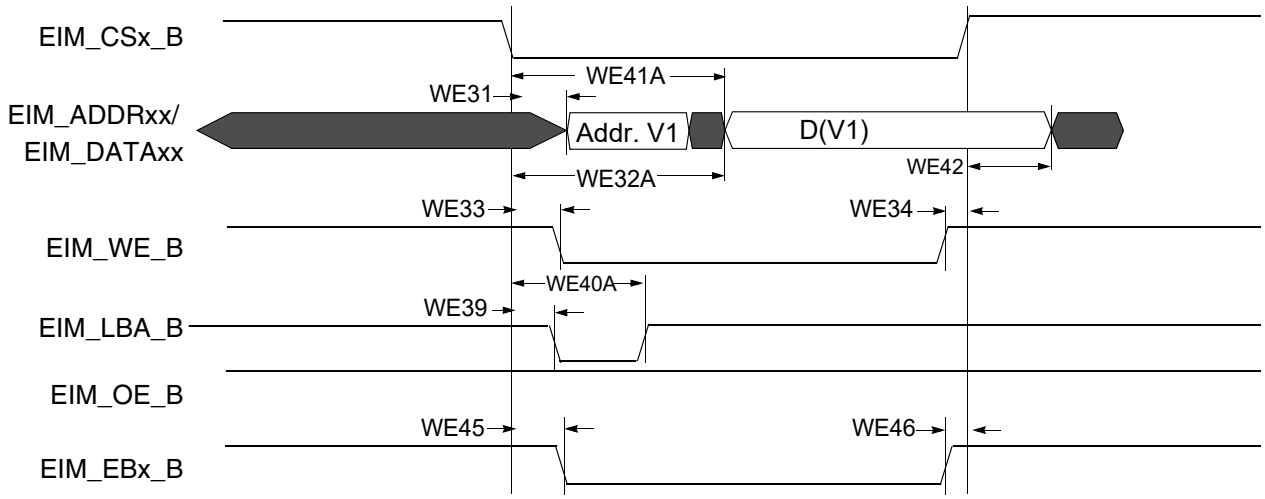


Figure 19. Asynchronous A/D Muxed Write Access

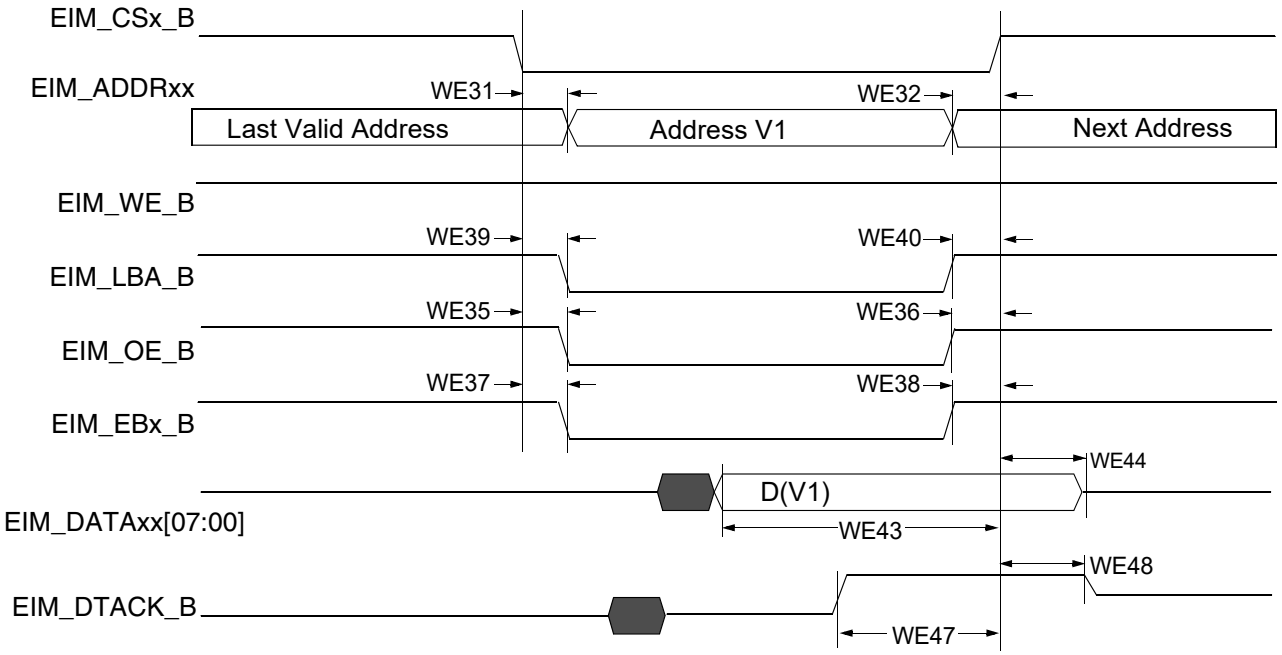


Figure 20. DTACK Mode Read Access (DAP=0)

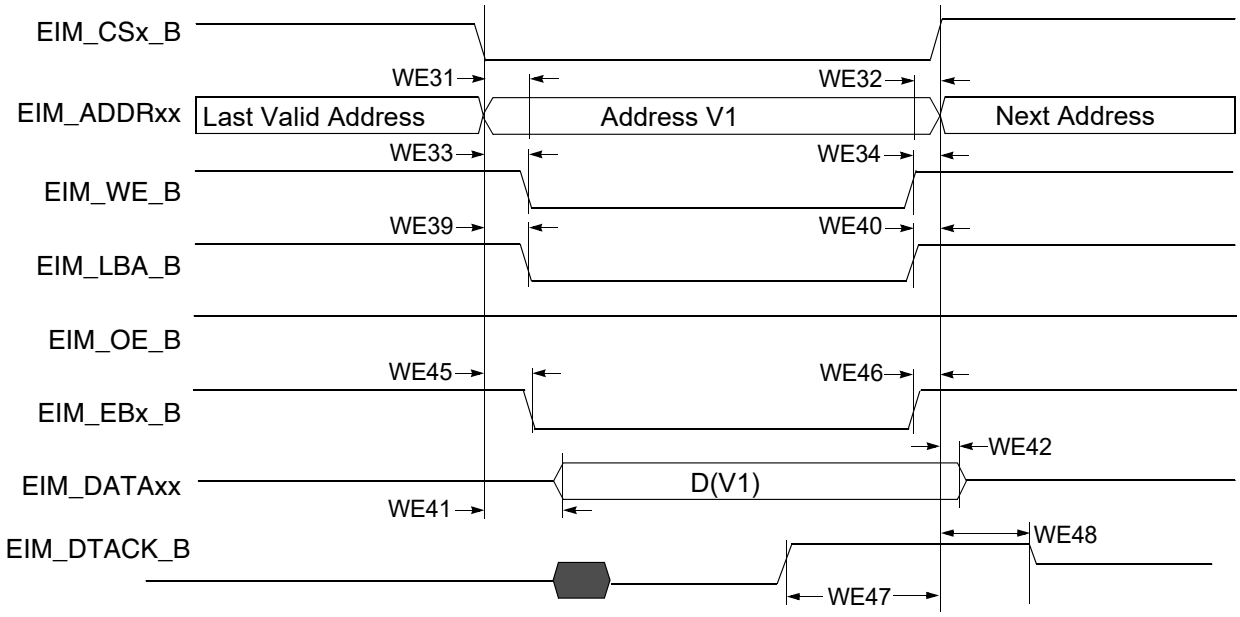


Figure 21. DTACK Mode Write Access (DAP=0)

Table 36. EIM Asynchronous Timing Parameters Relative to Chip Select[1, 2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4-WE6-CSA×t	-3.5-CSA×t	3.5-CSA×t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7-WE5-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t+WE4-WE7+ (ADVN+ADVA+1-CSA)×t	t - 3.5+(ADVN+ADVA+1-CSA)×t	t + 3.5+(ADVN+ADVA+ 1-CSA)×t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8-WE6+(WEA-WCSA)×t	-3.5+(WEA-WCSA)×t	3.5+(WEA-WCSA)×t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7-WE9+(WEN-WCSN)×t	-3.5+(WEN-WCSN)×t	3.5+(WEN-WCSN)×t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10- WE6+(OEA-RCSA)×t	-3.5+(OEA-RCSA)×t	3.5+(OEA-RCSA)×t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	-3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7-WE11+(OEN-RCSN)×t	-3.5+(OEN-RCSN)×t	3.5+(OEN-RCSN)×t	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12-WE6+(RBEA-RCSA)× t	-3.5+(RBEA- RCSA)×t	3.5+(RBEA - RCSA)×t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7-WE13+(RBEN-RCSN)×t	-3.5+ (RBEN-RCSN)×t	3.5+(RBEN-RCSN)×t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14-WE6+(ADVA-CSA)×t	-3.5+ (ADVA-CSA)×t	3.5+(ADVA-CSA)×t	ns

Table 36. EIM Asynchronous Timing Parameters Relative to Chip Select[1, 2] (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7-WE15-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14-WE6+(ADVN+ADVA+1-CSA)×t	-3.5+(ADVN+ADVA+1-CSA)×t	3.5+(ADVN+ADVA+1-CSA)×t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16-WE6-WCSA×t	-3.5-WCSA×t	3.5-WCSA×t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16-WE6+(WADVN+WADVA+ADH+1-WCSA)×t	-3.5+(WADVN+WADVA+ADH+1-WCSA)×t	3.5+(WADVN+WADVA+ADH+1-WCSA)×t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17-WE7-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs.	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out.	10	—	10	ns
MAXDI	EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDI	MAXCO-MAXCSO+MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12-WE6+(WBEA-WCSA)×t	-3.5+(WBEA-WCSA)×t	3.5+(WBEA-WCSA)×t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7-WE13+(WBEN-WCSN)×t	-3.5+(WBEN-WCSN)×t	3.5+(WBEN-WCSN)×t	ns
MAXDTI	Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization	10	—	10	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDTI	MAXCO-MAXCSO+MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

[2] In this table:
- t means clock period from axi_clk frequency.
- CSA means register setting for WCSA when in write operations or RCSA when in read operations.
- CSN means register setting for WCSN when in write operations or RCSN when in read operations.
- ADVN means register setting for WADVN when in write operations or RADVN when in read operations.
- ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-Mode DDR Controller (MMDC)

The Multi-mode DDR Controller is a dedicated interface to LPDDR2 SDRAM.

4.10.1 MMDC Compatibility with JEDEC-Compliant SDRAMs

The i.MX 6Dual/6Quad MMDC supports the following memory type:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG).

4.10.2 MMDC Supported LPDDR2 Configurations

The table below shows the supported LPDDR2 configurations:

Table 37. i.MX 6Dual/6Quad Supported LPDDR2 Configurations

Parameter	LPDDR2
Clock frequency	400 MHz
Bus width	32-bit per channel
Channel	Dual
Chip selects	2 per channel

4.11 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

4.11.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 22 through Figure 25 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 38 describes the timing parameters (NF1–NF17) that are shown in the figures.

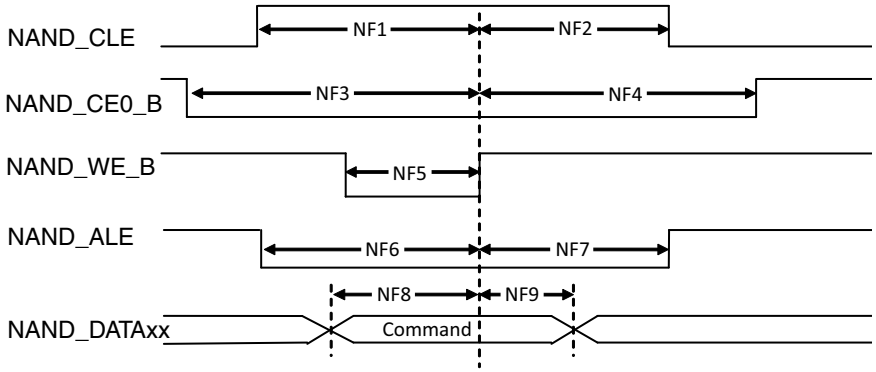


Figure 22. Command Latch Cycle Timing Diagram

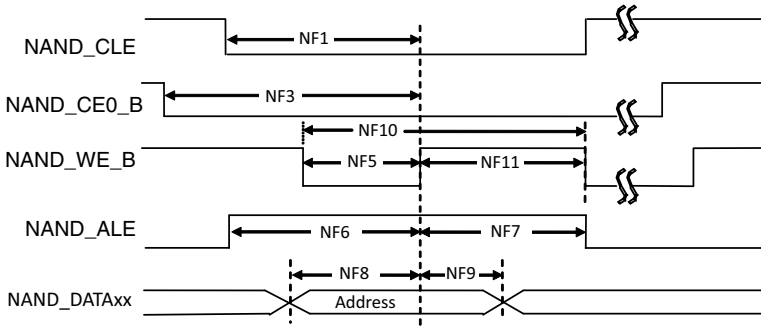


Figure 23. Address Latch Cycle Timing Diagram

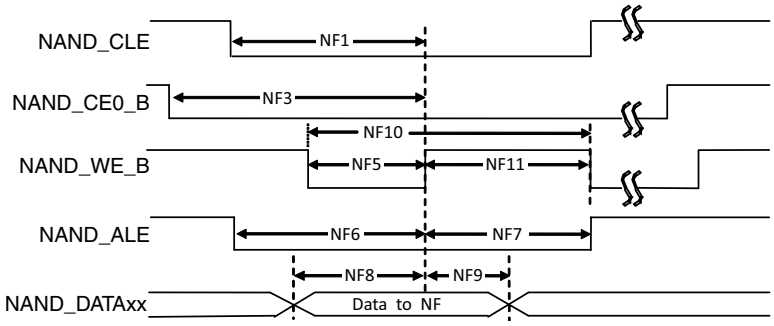


Figure 24. Write Data Latch Cycle Timing Diagram

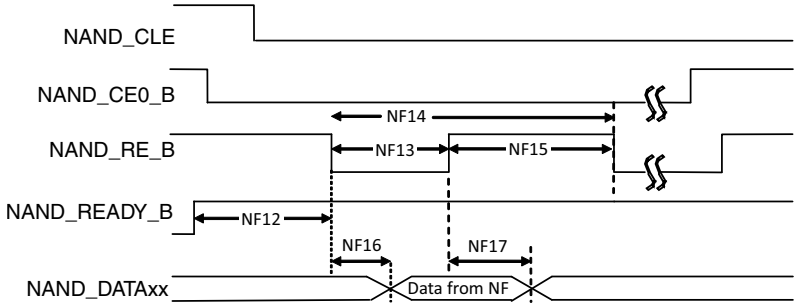


Figure 25. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

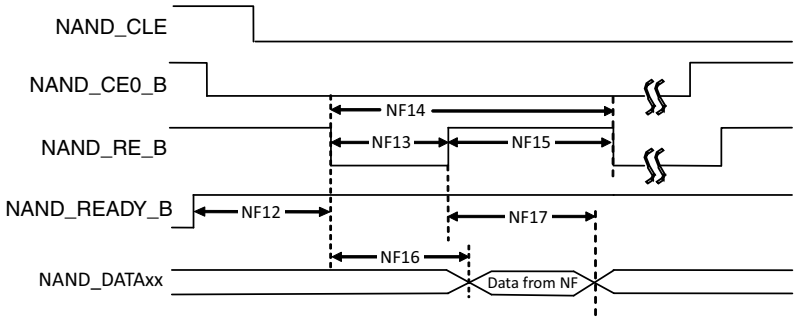


Figure 26. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 38. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		ns
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1) × T [see 3,2]		ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T - 1 [see 2]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see 2]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see 2]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see 2]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see 2]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see 2]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see 3,2]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see 2]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see 2]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see 2]		ns

Table 38. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see 5,6]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see 5,6]	—	ns

1 The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is met automatically by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 26), NF16/NF17 are different from the definition in non-EDO mode (Figure 25). They are called tREA/tRHOH (NAND_RE_B access time/NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 27 shows the write and read timing of Source Synchronous mode.

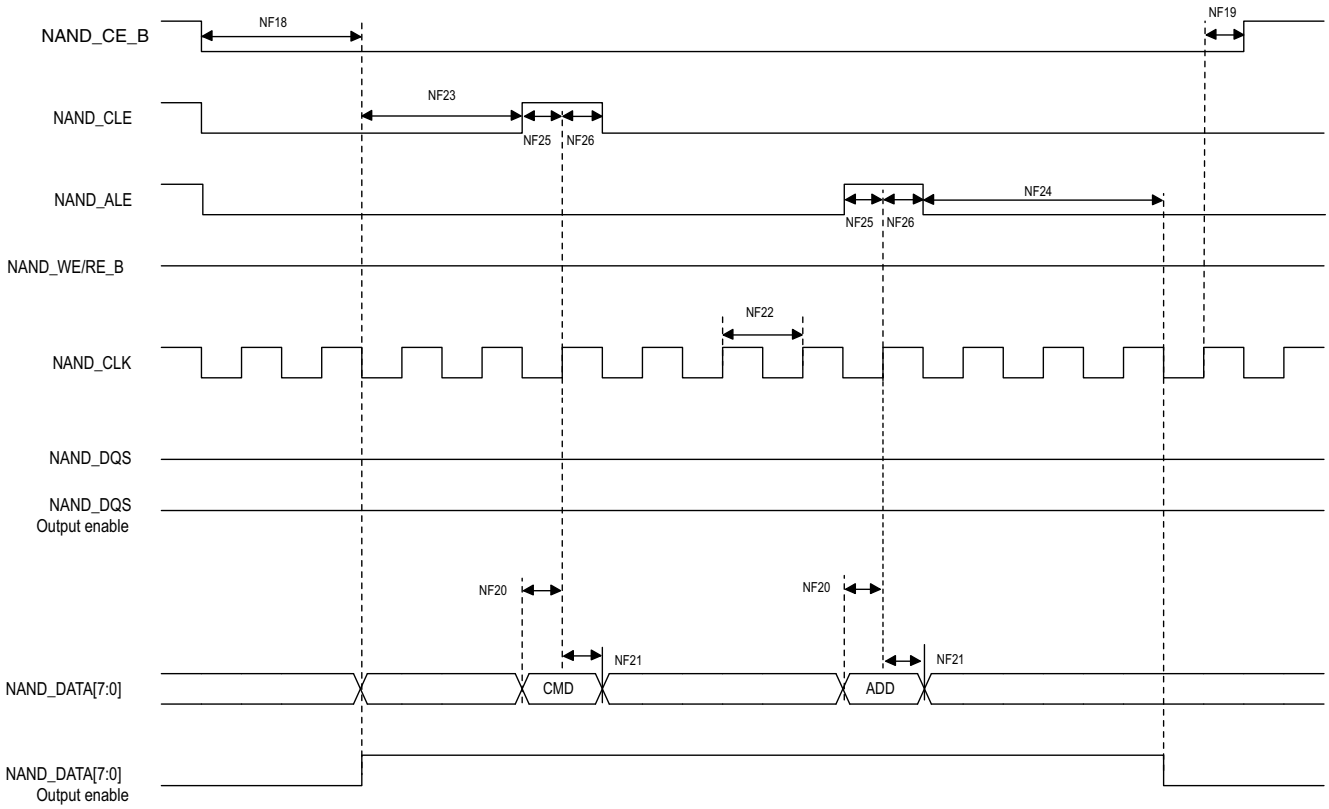


Figure 27. Source Synchronous Mode Command and Address Timing Diagram

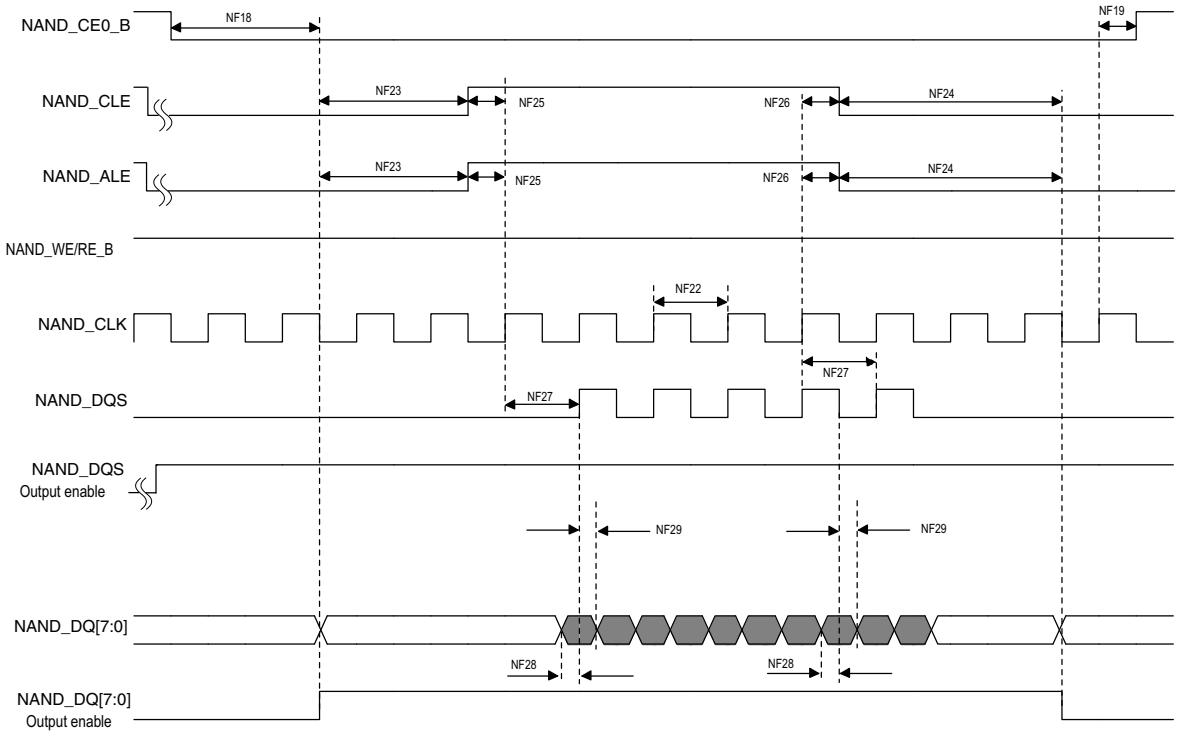


Figure 28. Source Synchronous Mode Data Write Timing Diagram

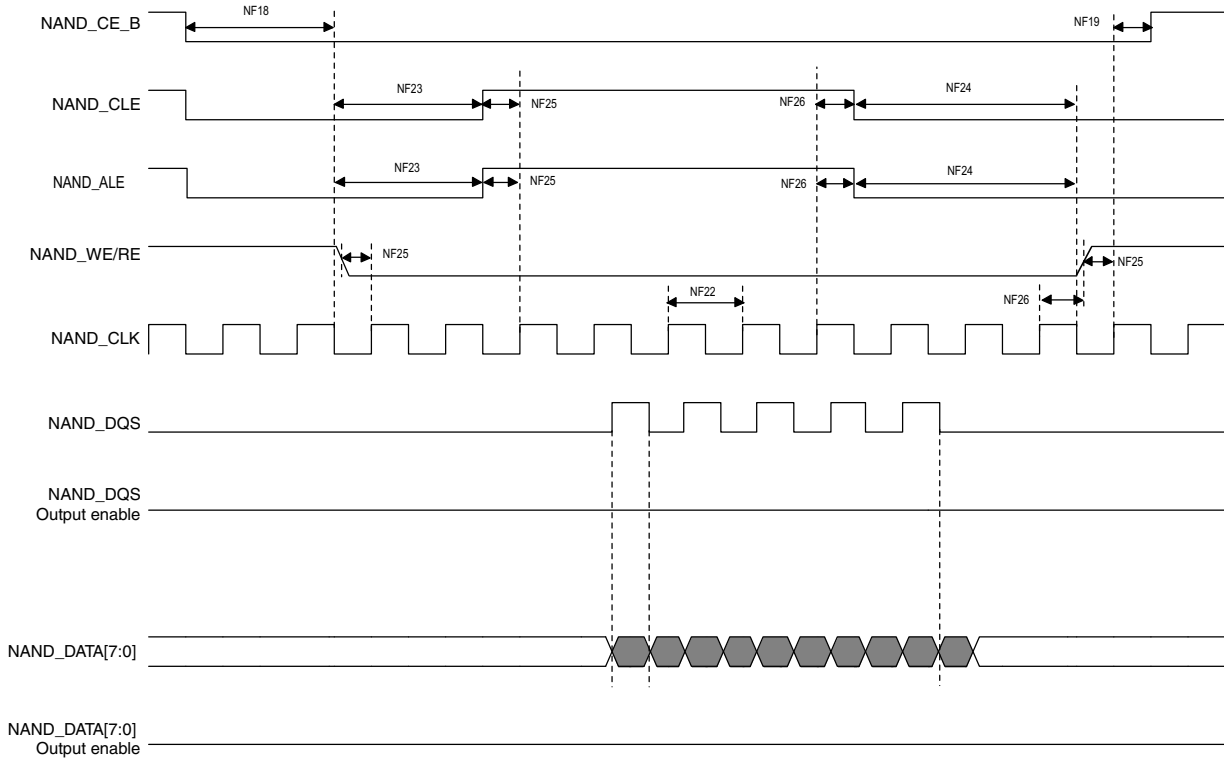


Figure 29. Source Synchronous Mode Data Read Timing Diagram

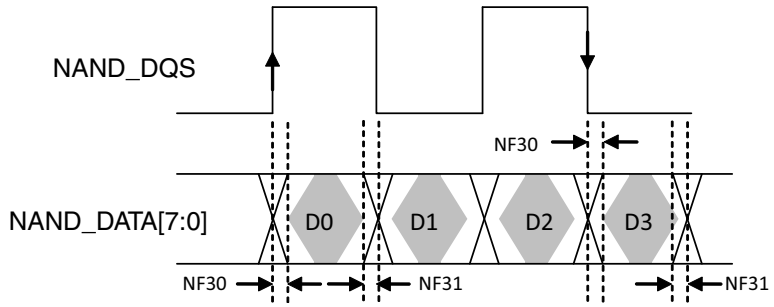


Figure 30. NAND_DQS/NAND_DQ Read Valid Window

Table 39. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CEx_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	tDS	0.25 × tCK - 0.35		—
NF29	Data write hold	tDH	0.25 × tCK - 0.85		—
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS	—	1.95	—

1 The GPMI source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

Figure 30 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.3 Samsung Toggle Mode AC Timing

4.11.3.1 Command and Address Timing

Samsung Toggle mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.11.1, “Asynchronous Mode AC Timing (ONFI 1.0 Compatible)” for details.

4.11.3.2 Read and Write Timing

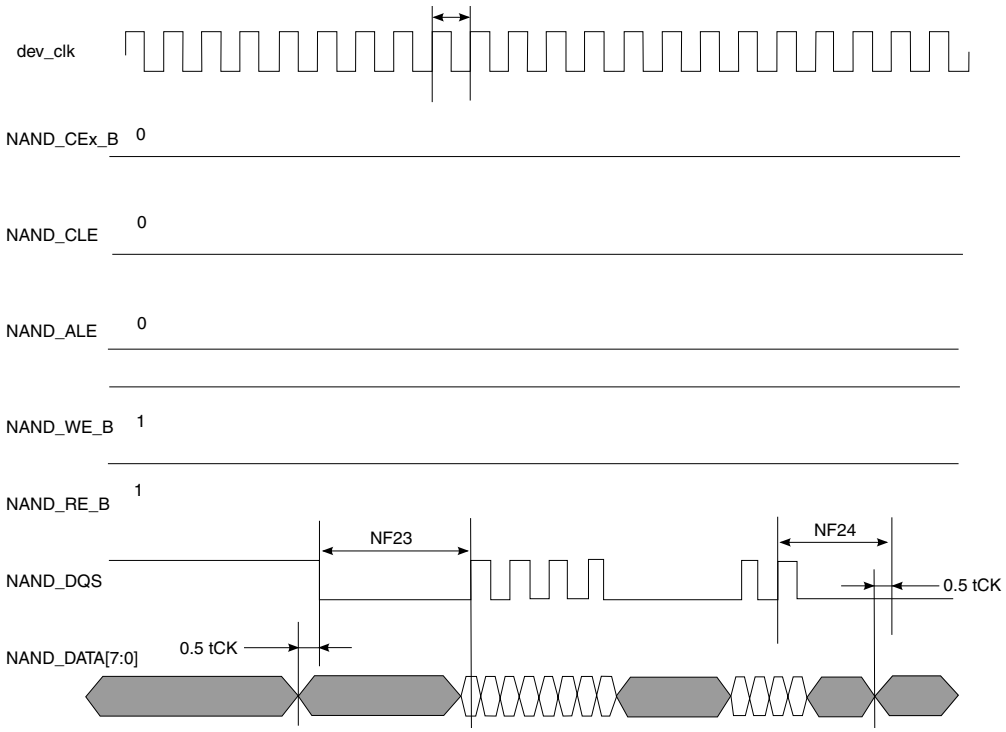


Figure 31. Samsung Toggle Mode Data Write Timing

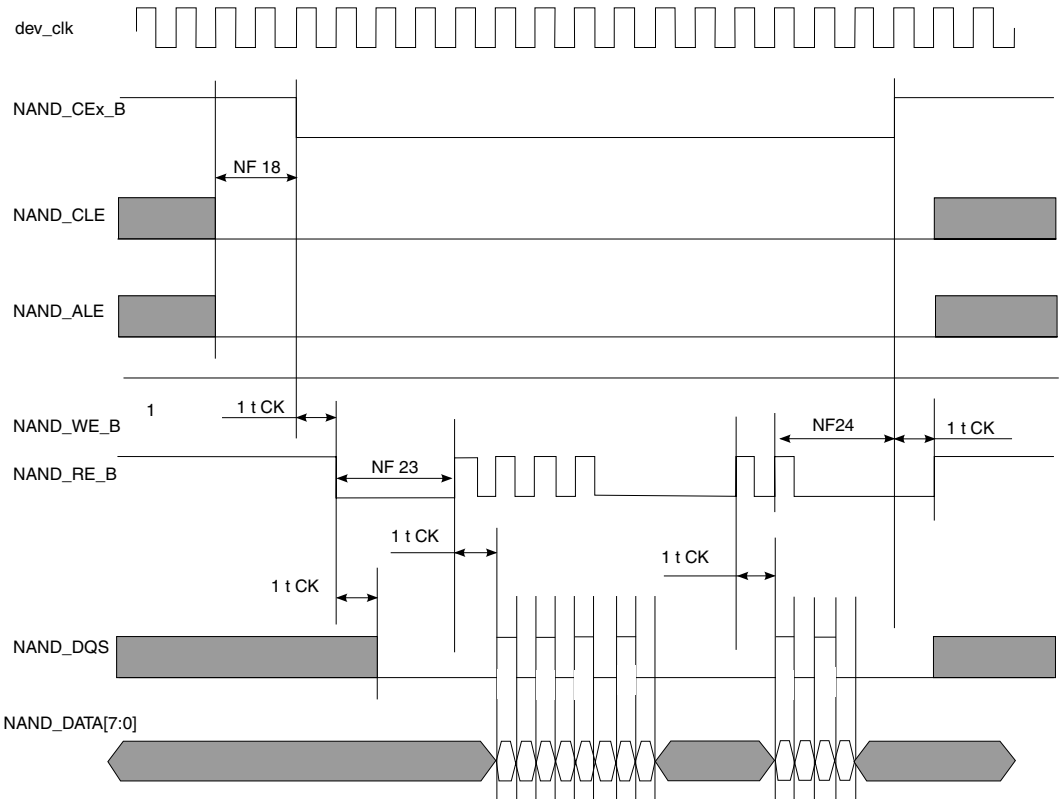


Figure 32. Samsung Toggle Mode Data Read Timing

Table 40. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		—
NF3	NAND_CEx_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		—
NF4	NAND_CEx_B hold time	tCH	DH × T - 1 [see 2]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

Table 40. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	—

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is met automatically by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS).

6 Shown in Figure 28.

7 Shown in Figure 29.

Figure 30 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For DDR Toggle mode, the typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM)). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 AUDMUX Timing Parameters

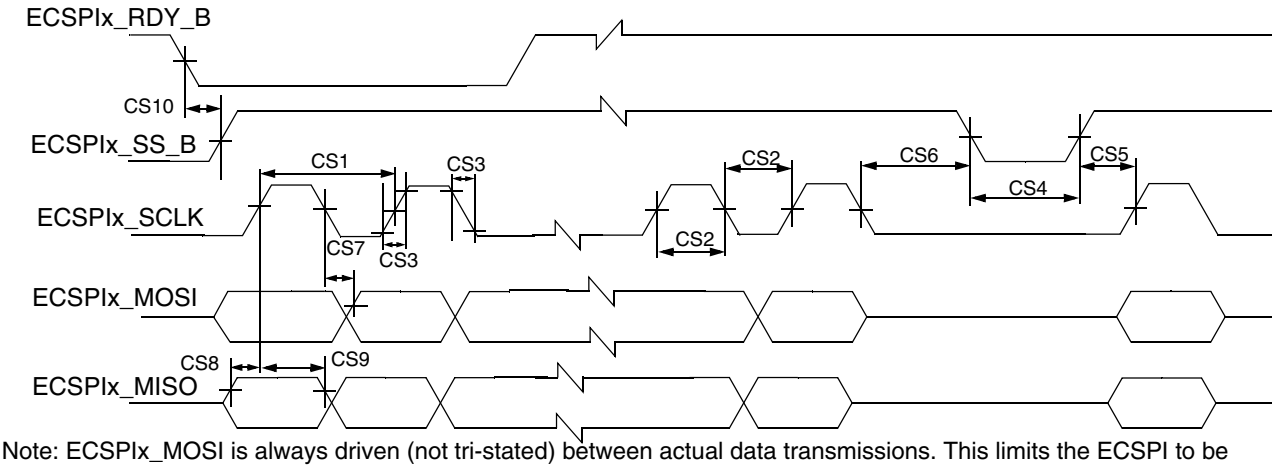
The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.12.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.12.2.1 ECSPI Master Mode Timing

Figure 33 depicts the timing of ECSPI in master mode and Table 41 lists the ECSPI master mode timing characteristics.



Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 33. ECSPI Master Mode Timing Diagram

Table 41. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	 21.5 16	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow includes:
ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/ ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

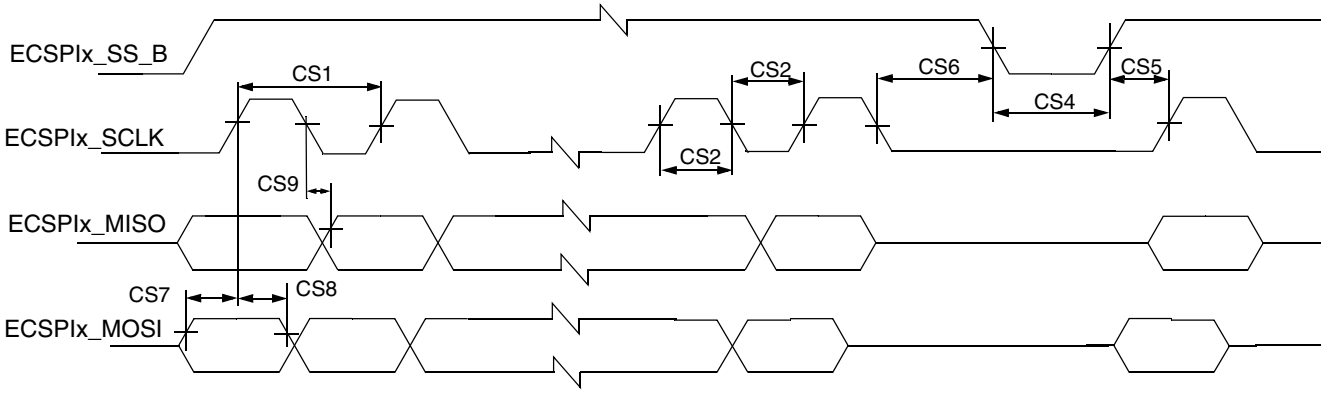
2 ECSPI fast includes:
ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

3 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

4 ECSPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.2.2 ECSPI Slave Mode Timing

Figure 34 depicts the timing of ECSPI in slave mode and Table 42 lists the ECSPI slave mode timing characteristics.



Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 34. ECSPI Slave Mode Timing Diagram

Table 42. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF) • Slow group[1] • Fast group[2]	t_{PDmiso}	4	 25 17	ns

[1] ECSPI slow includes:
ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/DISP0_DAT17, ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

[2] ECSPI fast includes:
ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

4.12.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 43 shows the interface timing values. The number field in the table refers to timing signals found in Figure 35 and Figure 36.

Table 43. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	19.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	19.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	19.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FSout (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (serial clock in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 19.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 19.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	19.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 43. Enhanced Serial Audio Interface (ESAI) Timing (continued)

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	19.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(ESAI_TX_CLK pin) = transmit clock
ESAI_RX_CLK(ESAI_RX_CLK pin) = receive clock
ESAI_TX_FS(ESAI_TX_FS pin) = transmit frame sync
ESAI_RX_FS(ESAI_RX_FS pin) = receive frame sync
ESAI_TX_HF_CLK(ESAI_TX_HF_CLK pin) = transmit high frequency clock
ESAI_RX_HF_CLK(ESAI_RX_HF_CLK pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

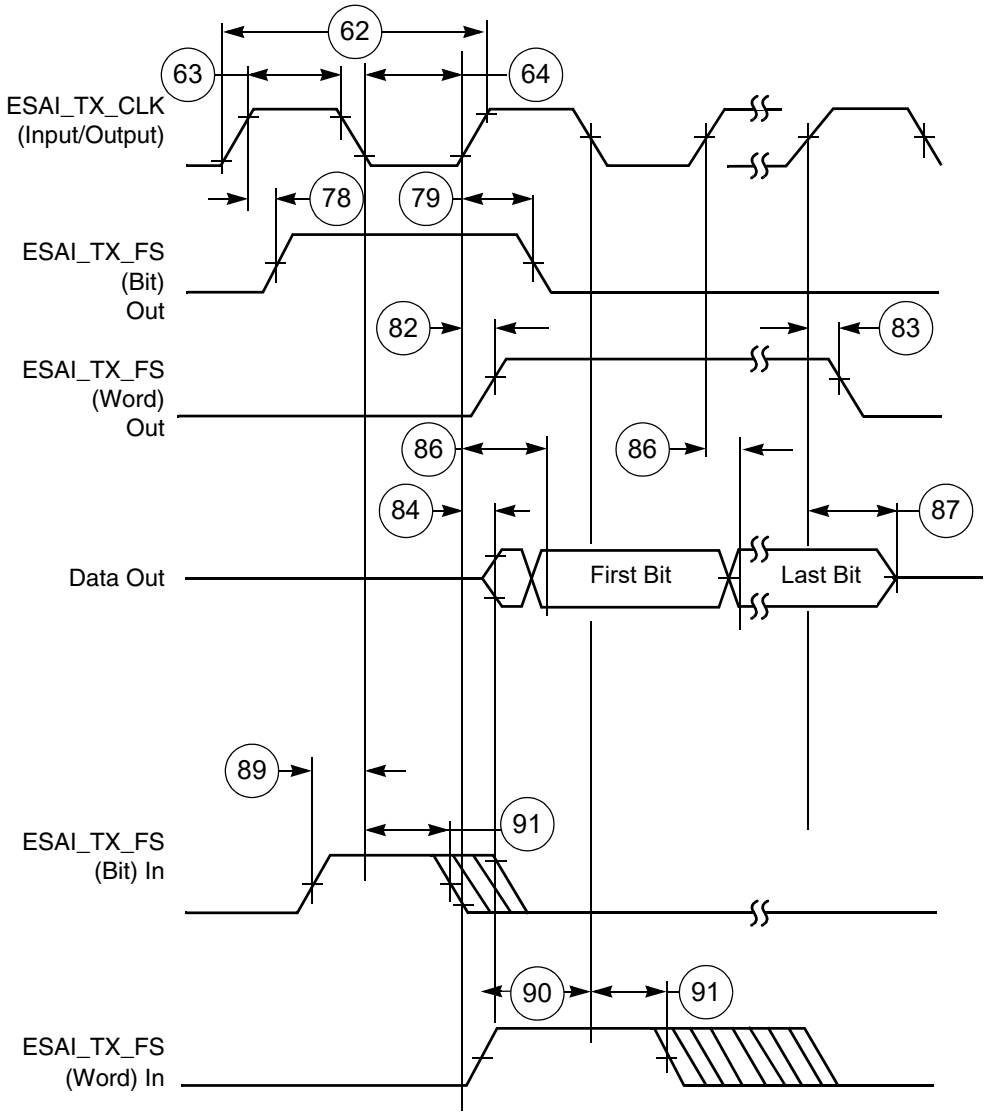


Figure 35. ESAI Transmitter Timing

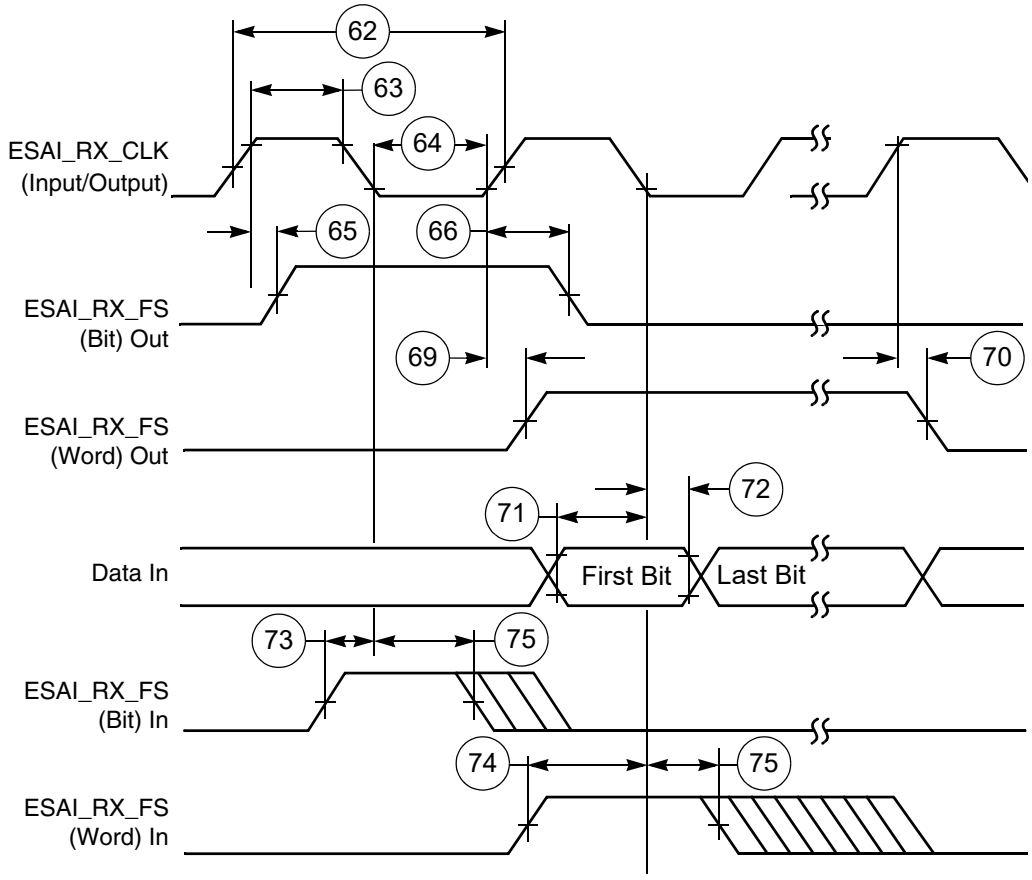


Figure 36. ESAI Receiver Timing

4.12.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.1 (Dual Date Rate) timing.

4.12.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 37 depicts the timing of SD/eMMC4.3, and Table 44 lists the SD/eMMC4.3 timing characteristics.

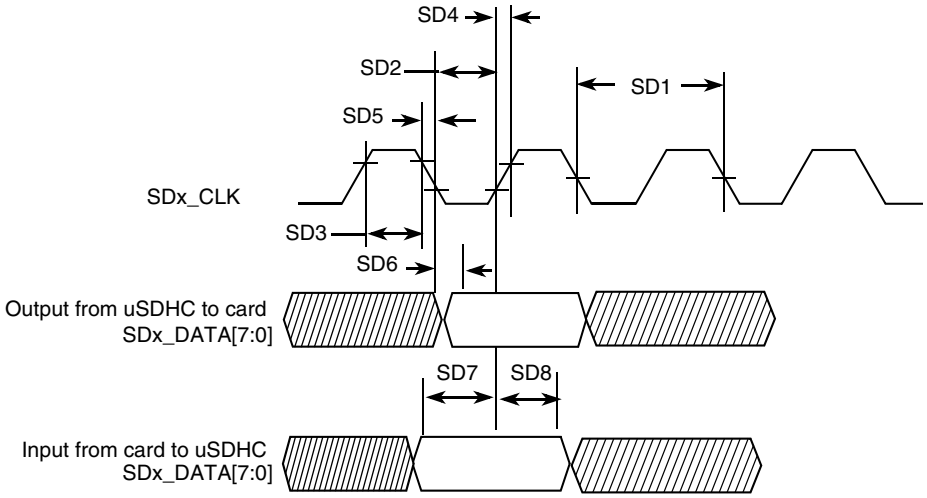


Figure 37. SD/eMMC4.3 Timing

Table 44. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

Table 44. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs SD_CMD, SD_DATAx (Reference to SDx_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 38 depicts the timing of eMMC4.4/4.41. Table 45 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SD_CMD).

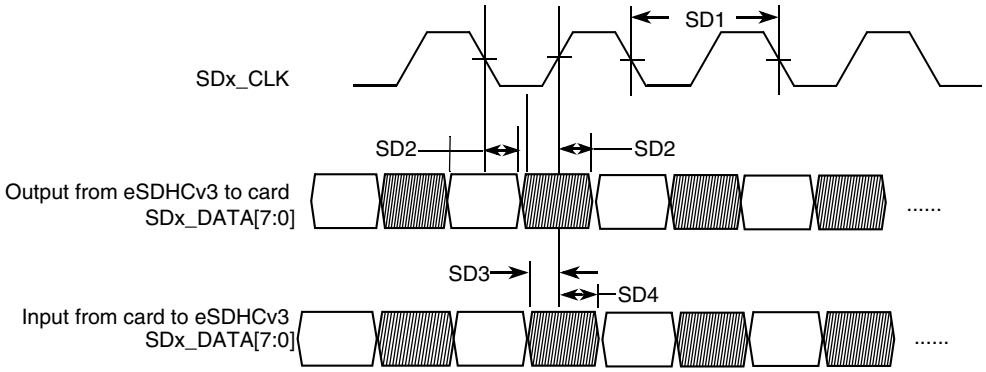


Figure 38. eMMC4.4/4.41 Timing

Table 45. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to SD_CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

4.12.4.3 SDR50/SDR104 AC Timing

Figure 39 depicts the timing of SDR50/SDR104, and Table 46 lists the SDR50/SDR104 timing characteristics.

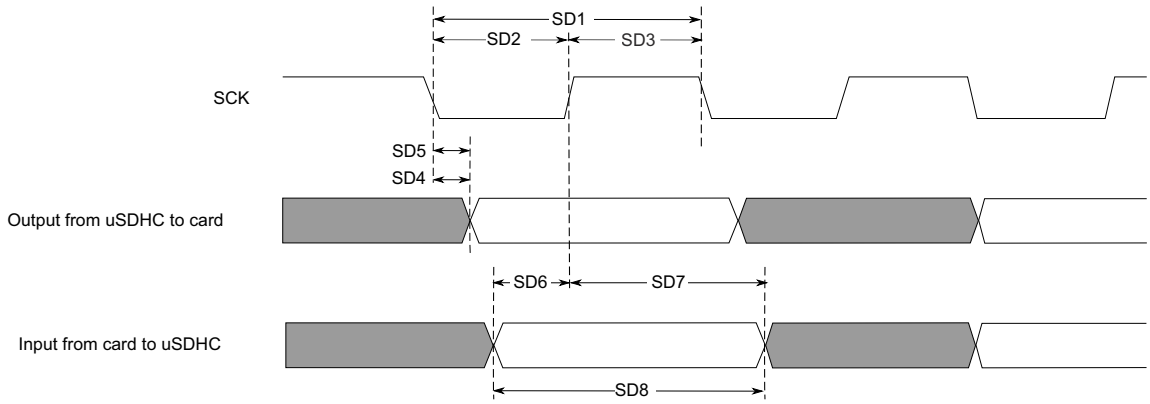


Figure 39. SDR50/SDR104 Timing

Table 46. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.12.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 21, “GPIO I/O DC Parameters,” on page 38.

4.12.5 Ethernet Controller (ENET) AC Electrical Specifications

4.12.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.12.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 40 shows MII receive signal timings. Table 47 describes the timing parameters (M1–M4) shown in the figure.

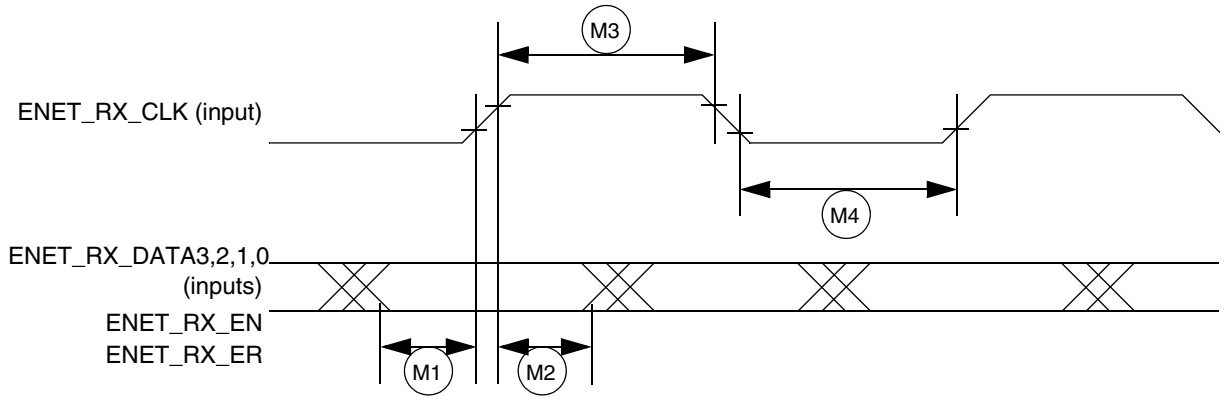


Figure 40. MII Receive Signal Timing Diagram

Table 47. MII Receive Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.12.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 41 shows MII transmit signal timings. Table 48 describes the timing parameters (M5–M8) shown in the figure.

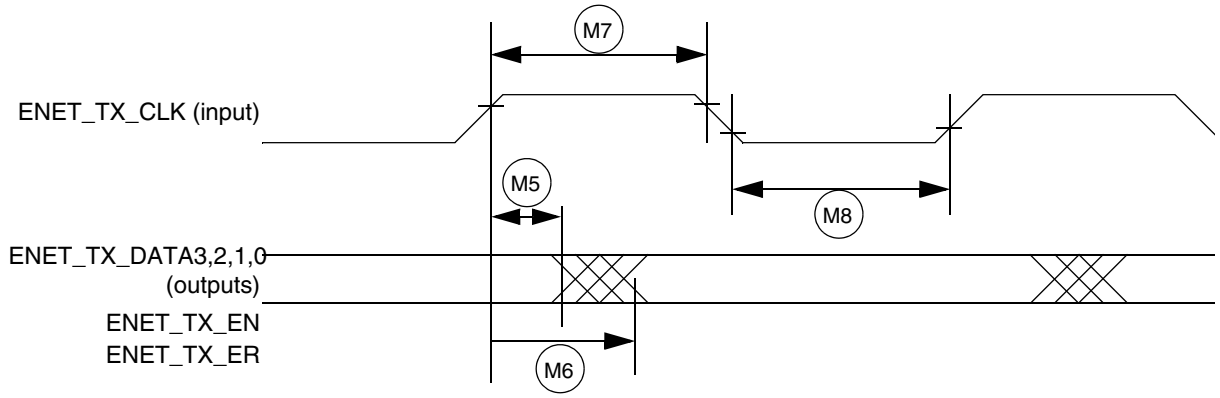


Figure 41. MII Transmit Signal Timing Diagram

Table 48. MII Transmit Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.12.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 42 shows MII asynchronous input timings. Table 49 describes the timing parameter (M9) shown in the figure.

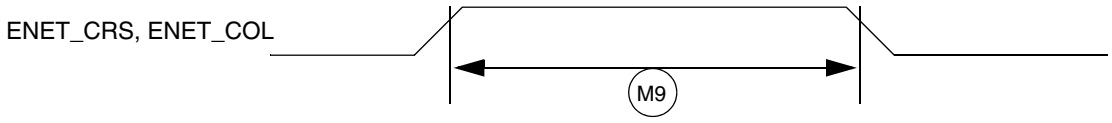


Figure 42. MII Async Inputs Timing Diagram

Table 49. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min	Max	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.12.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 43 shows MII asynchronous input timings. Table 50 describes the timing parameters (M10–M15) shown in the figure.

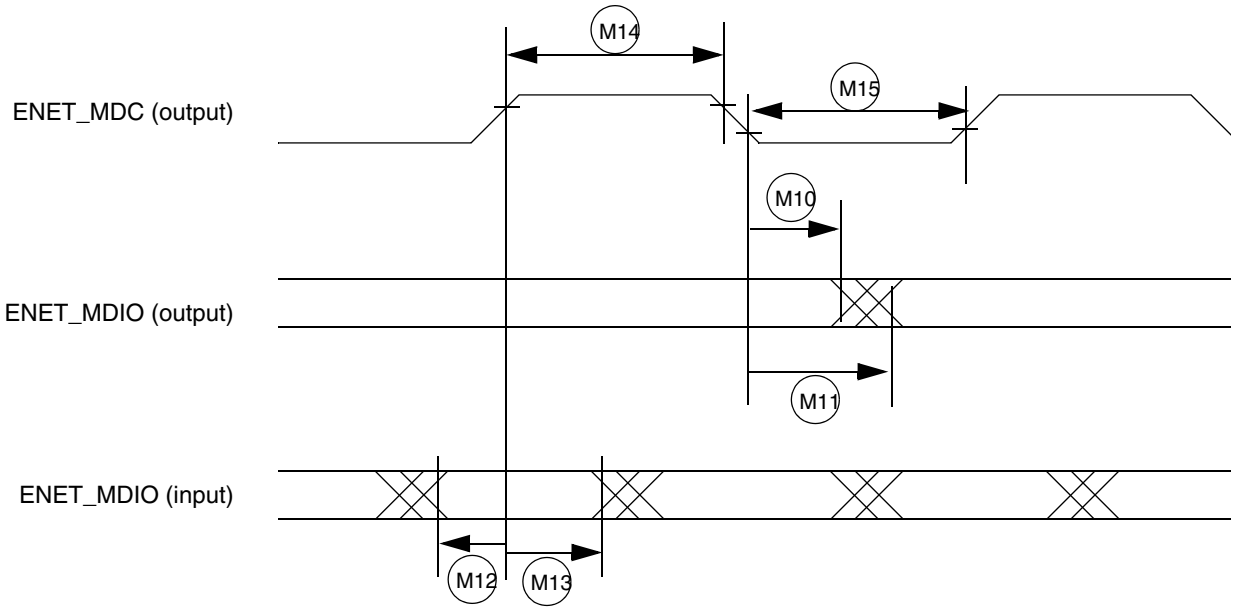


Figure 43. MII Serial Management Channel Timing Diagram

Table 50. MII Serial Management Channel Timing

ID	Characteristic	Min	Max	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (maximum propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.12.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET_RXD[1:0] and ENET_RX_ER.

Figure 44 shows RMII mode timings. Table 51 describes the timing parameters (M16–M21) shown in the figure.

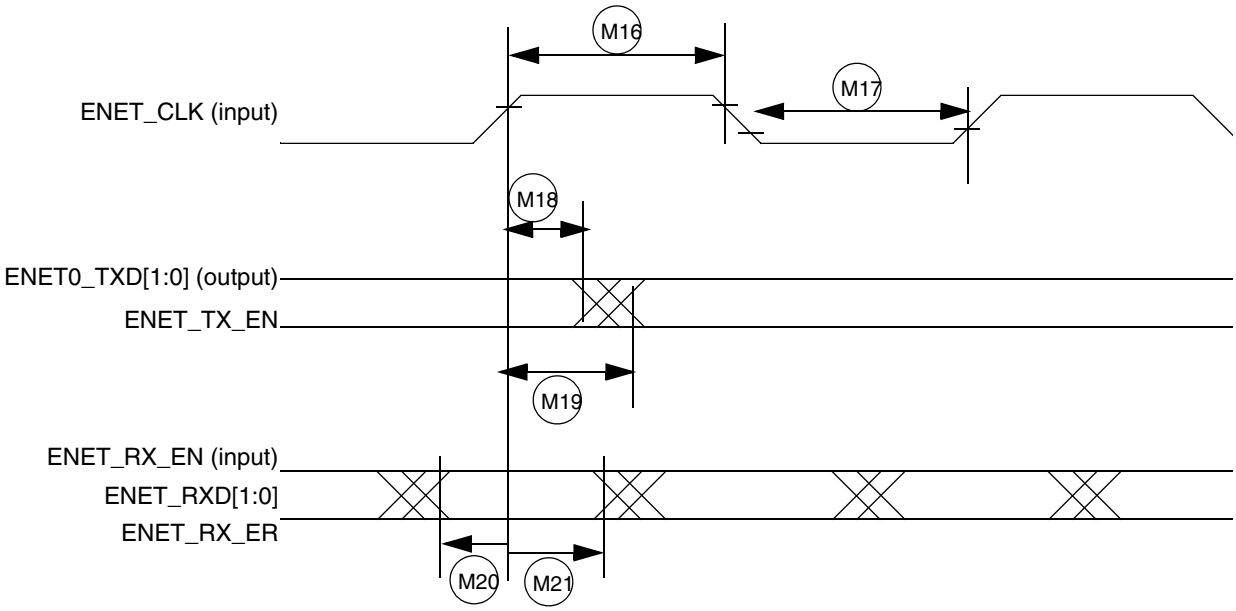


Figure 44. RMII Mode Signal Timing Diagram

Table 51. RMII Signal Timing

ID	Characteristic	Min	Max	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	13.5	ns
M20	ENET_RXD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.12.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 52. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

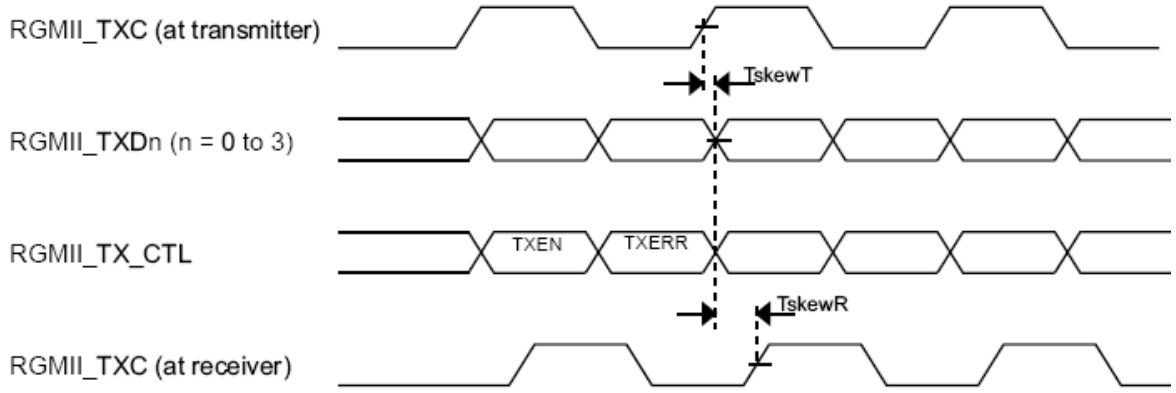


Figure 45. RGMII Transmit Signal Timing Diagram Original

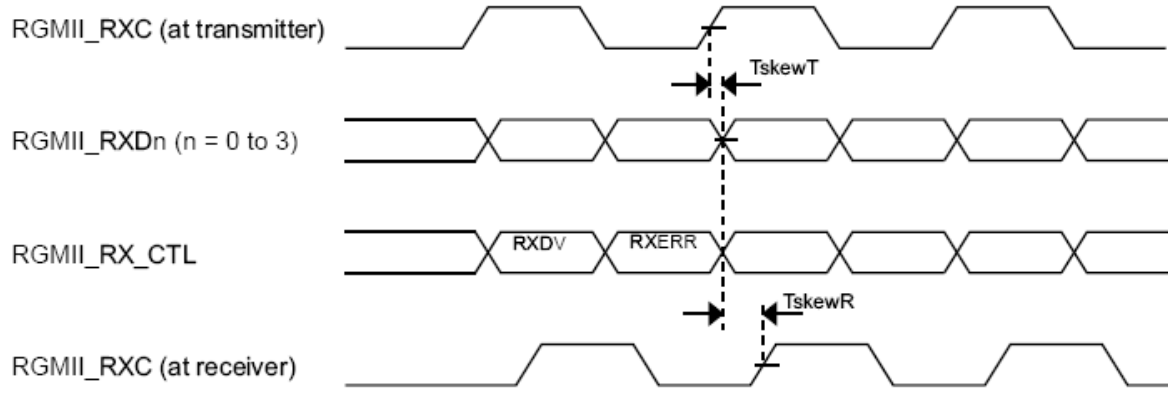


Figure 46. RGMII Receive Signal Timing Diagram Original

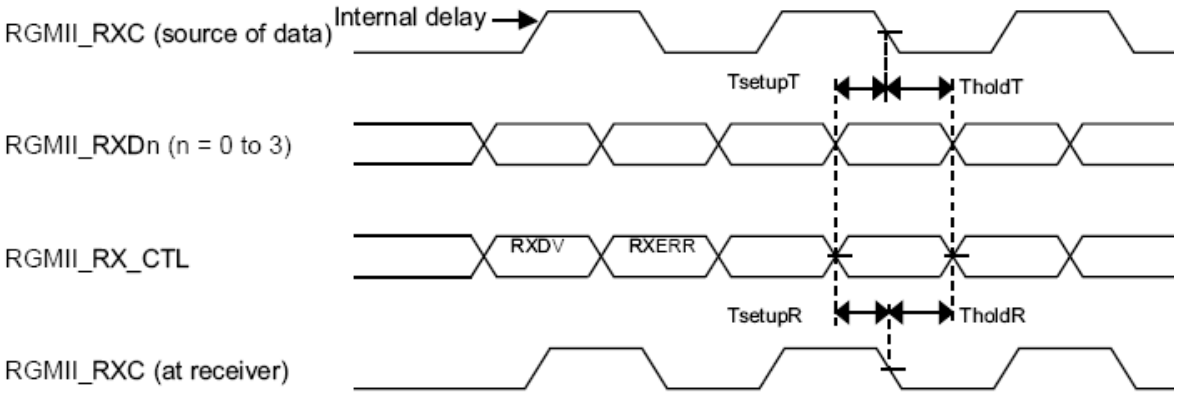


Figure 47. RGMII Receive Signal Timing Diagram with Internal Delay

4.12.6 Flexible Controller Area Network (FlexCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification.The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM) to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.12.7 HDMI Module Timing Parameters

4.12.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 µs.

4.12.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

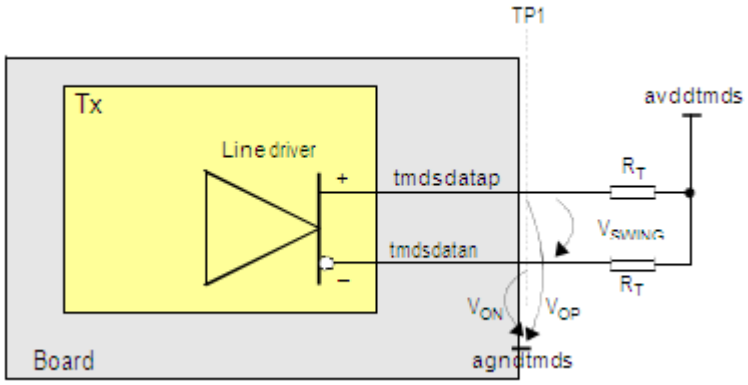


Figure 48. Driver Measuring Conditions

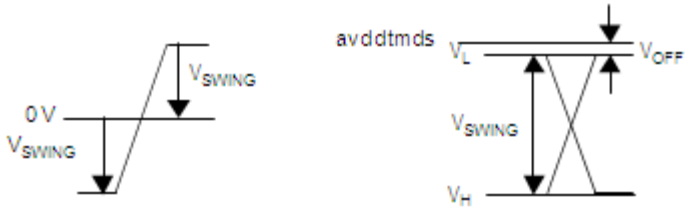


Figure 49. Driver Definitions

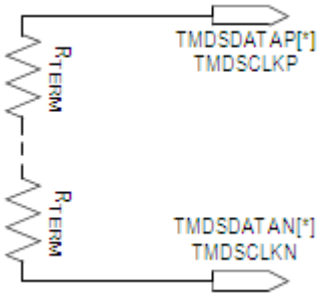


Figure 50. Source Termination

Table 53. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V

Table 53. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_T	Termination resistance	—	45	50	55	Ω
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	—	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above.	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds – 200 mV	—	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above.	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds – 600 mV	—	avddtmds – 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds – 700 mV	—	avddtmds – 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see the third figure above). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	—	50	—	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	—	2.0	—	5.3	V
$VHPD_{VL}$	Hot plug detect low range	—	0	—	0.8	V
HPD_Z	Hot plug detect input impedance	—	10	—	—	kΩ
HPD_t	Hot plug detect time delay	—	—	—	100	µs

4.12.8 Switching Characteristics

Table 54 describes switching characteristics for the HDMI 3D Tx PHY. Figure 51 to Figure 55 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

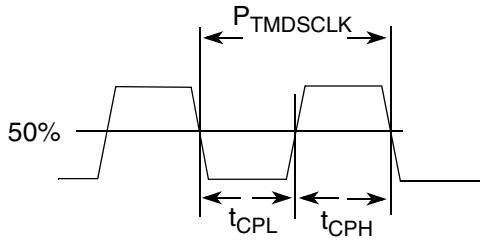


Figure 51. TMDS Clock Signal Definitions

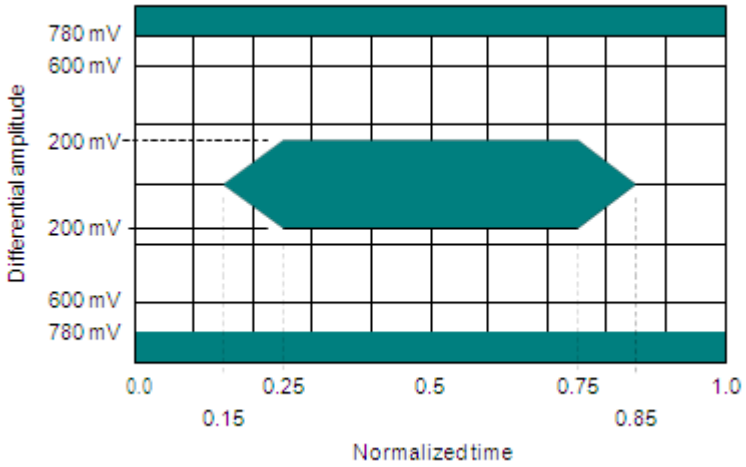


Figure 52. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

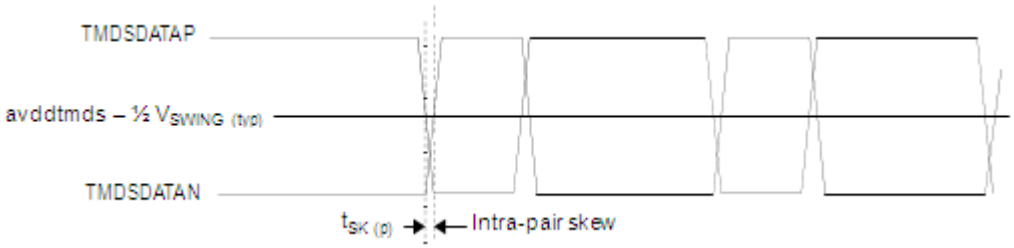


Figure 53. Intra-Pair Skew Definition

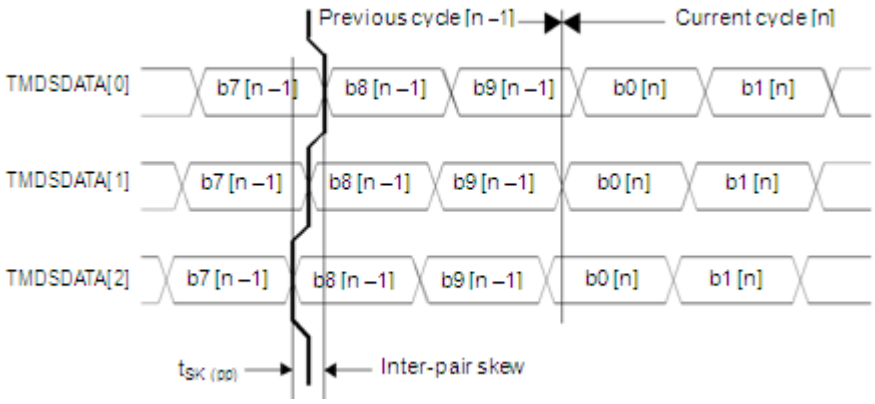


Figure 54. Inter-Pair Skew Definition

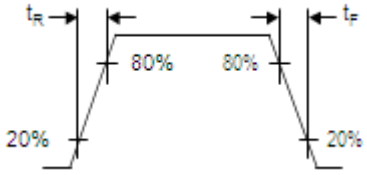


Figure 55. TMDS Output Signals Rise and Fall Time Definition

Table 54. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 51.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 51.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 51.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 51.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 53.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 54.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 55.	75	—	0.4 UI	ps

Table 54. Switching Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 55.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%
Data and Control Interface Specifications						
$t_{Power-up}$[2]	HDMI 3D Tx PHY power-up time	From power-down to HSI_TX_READY assertion	—	—	3.35	ms

1 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

2 For information about latencies and associated timings, see Section 4.12.7.1, "Latencies and Timing Information."

4.12.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 56 depicts the timing of I²C module, and Table 55 lists the I²C module timing characteristics.

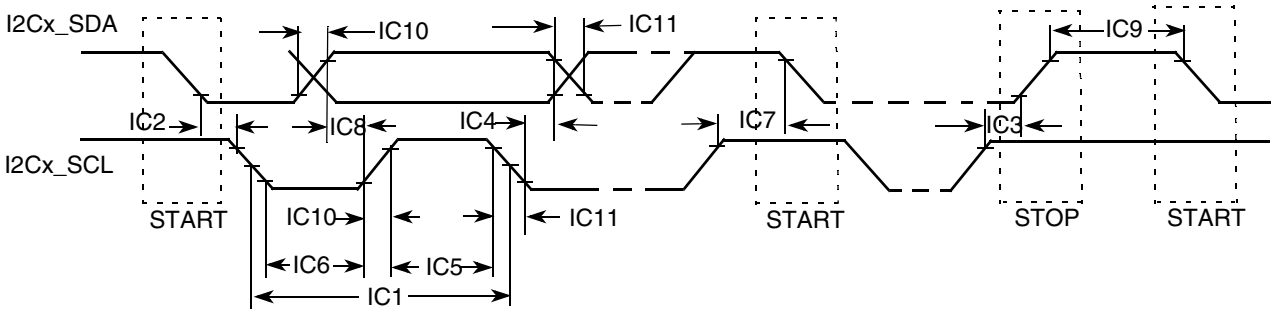


Figure 56. I²C Bus Timing

Table 55. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns

Table 55. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.12.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.12.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 56 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 56. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_ DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_ DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_ DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_ DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_ DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPU2_CSIx_ DATA_05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_ DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_ DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_ DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_ DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_ DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_ DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_ DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
IPUx_CSIx_ DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_ DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_ DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_ DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_ DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_ DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_ DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

[1] IPU2_CSIx stands for IPU2_CSI1 or IPU2_CSI2.

2 The MSB bits are duplicated on LSB bits implementing color extension.
3 The two MSB bits are duplicated on LSB bits implementing color extension.
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.
7 YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.12.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.12.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPU2_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPU2_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPU2_CSIx_DATA_EN bus.

4.12.10.2.2 Gated Clock Mode

The IPU2_CSIx_VSYNC, IPU2_CSIx_HSYNC, and IPU2_CSIx_PIX_CLK signals are used in this mode. See Figure 57.

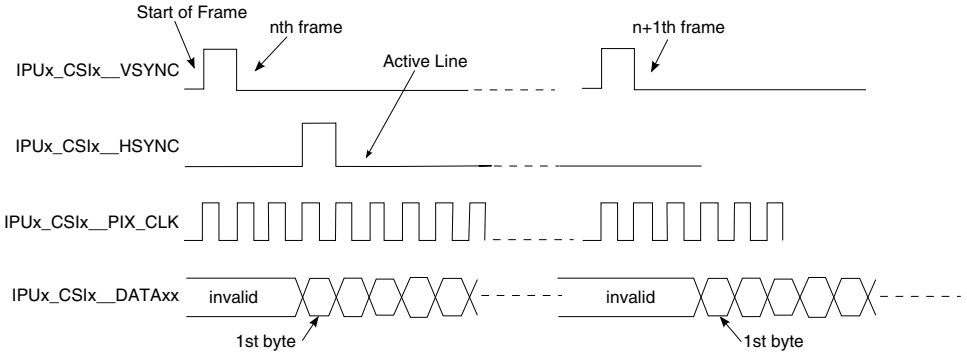


Figure 57. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPU2_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPU2_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPU2_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPU2_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI

stops receiving data from the stream. For the next line, the IPU2_CSIx_HSYNC timing repeats. For the next frame, the IPU2_CSIx_VSYNC timing repeats.

4.12.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.12.10.2.2, "Gated Clock Mode,") except for the IPU2_CSIx_HSYNC signal, which is not used (see Figure 58). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The IPU2_CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

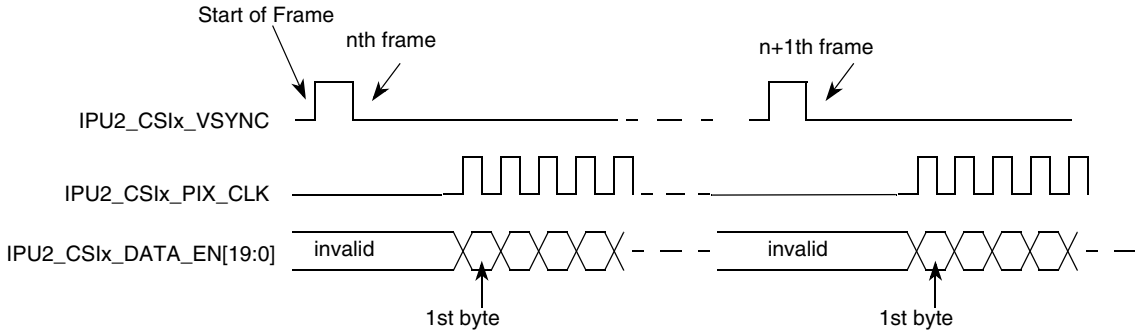


Figure 58. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 58 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered IPU2_CSIx_VSYNC; active-high/low IPU2_CSIx_HSYNC; and rising/falling-edge triggered IPU2_CSIx_PIX_CLK.

4.12.10.3 Electrical Characteristics

Figure 59 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 57 lists the sensor interface timing characteristics.

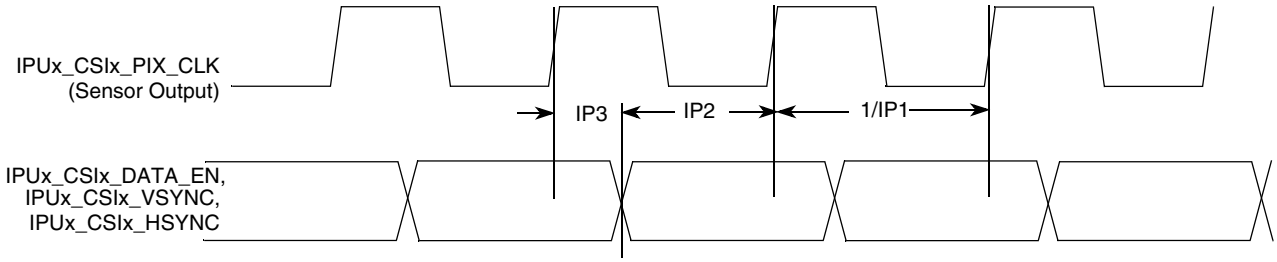


Figure 59. Sensor Interface Timing Diagram

Table 57. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns
—	Vsync to Hsync	Tv-h	1/Fpck	—	ns
—	Vsync and Hsync pulse width	Tpulse	1/Fpck	—	ns
—	Vsync to first data	Tv-d	1/Fpck	—	ns

4.12.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 58 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 58. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—

Table 58. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—
IPUx_DISPx_DAT07	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	—
IPUx_DISPx_DAT08	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	—
IPUx_DISPx_DAT09	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	—
IPUx_DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	—
IPUx_DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	—
IPUx_DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	—
IPUx_DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	—
IPUx_DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	—
IPUx_DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	—
IPUx_DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—
IPUx_DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—
IPUx_DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—
IPUx_DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—
IPUx_DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—
IPUx_DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—
IPUx_DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
IPUx_DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
IPUx_DIx_DISP_CLK	PixCLK							—
IPUx_DIx_PIN01	—							May be required for anti-tearing
IPUx_DIx_PIN02	HSYNC							—
IPUx_DIx_PIN03	VSYNC							VSYNC out

Table 58. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD						Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)					
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DIx_PIN04	—						Additional frame/row synchronous signals with programmable timing
IPUx_DIx_PIN05	—						
IPUx_DIx_PIN06	—						
IPUx_DIx_PIN07	—						
IPUx_DIx_PIN08	—						
IPUx_DIx_D0_CS	—						—
IPUx_DIx_D1_CS	—						Alternate mode of PWM output for contrast or brightness control
IPUx_DIx_PIN11	—						—
IPUx_DIx_PIN12	—						—
IPUx_DIx_PIN13	—						Register select signal
IPUx_DIx_PIN14	—						Optional RS2
IPUx_DIx_PIN15	DRDY/DV						Data validation/blank, data enable
IPUx_DIx_PIN16	—						Additional data synchronous signals with programmable features/timing
IPUx_DIx_PIN17	Q						

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 Restrictions for ports IPUx_DISPx_DAT00 through IPUx_DISPx_DAT23 are as follows:
- A maximum of three continuous groups of bits can be independently mapped to the external bus. Groups must not overlap.
- The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit.

3 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 58 provides information for both the DISP0 and DISP1 ports. However, DISP1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all configurations. See the IOMUXC table for details.

4.12.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls.

4.12.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent waveform.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.12.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.12.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.12.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.12.10.6.2 LCD Interface Functional Description

Figure 60 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPUx_DIx_PIN02 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPUx_DIx_PIN03 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

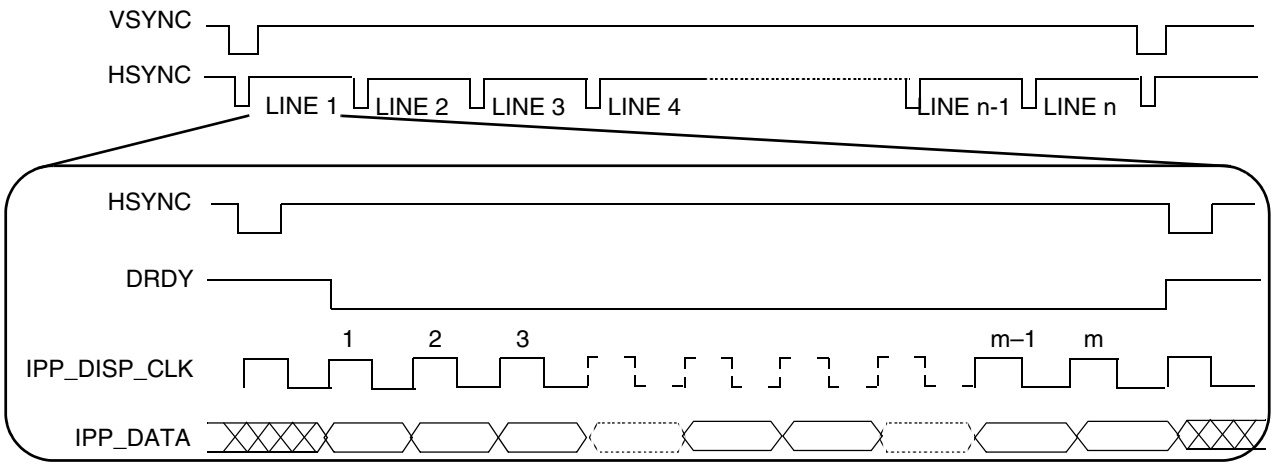


Figure 60. Interface Timing Diagram for TFT (Active Matrix) Panels

4.12.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 61 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

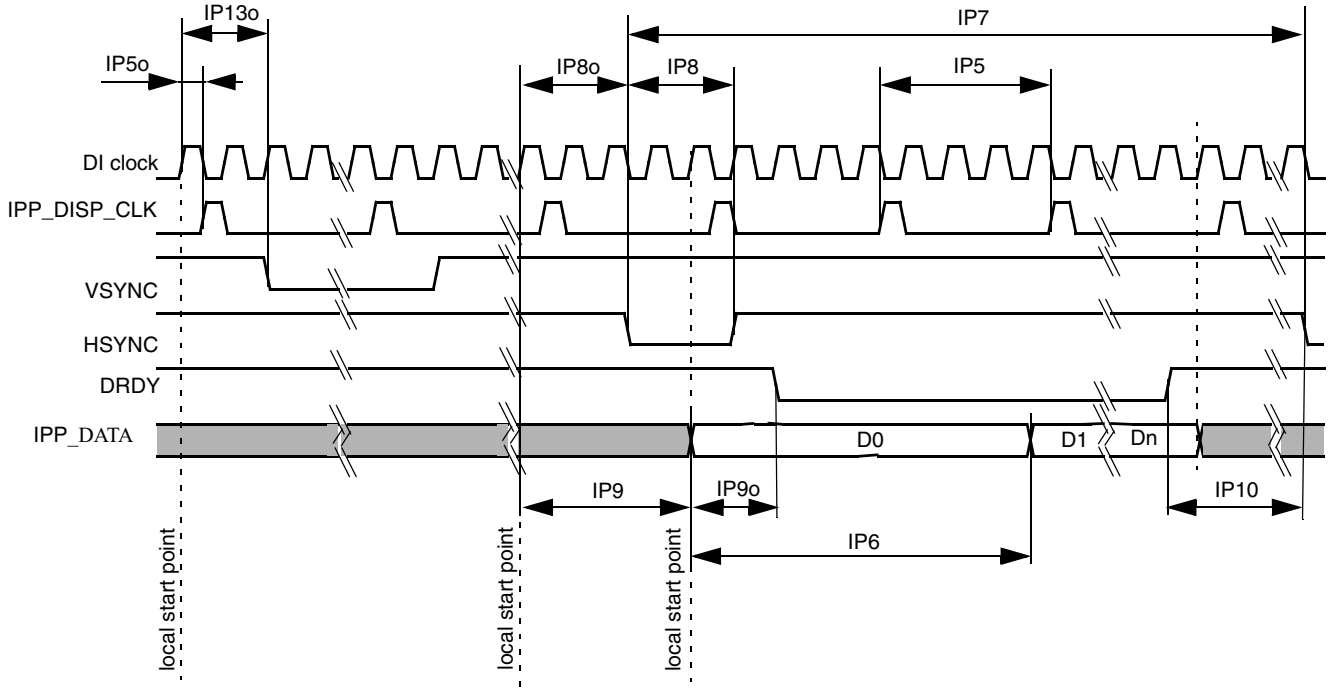


Figure 61. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 62 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

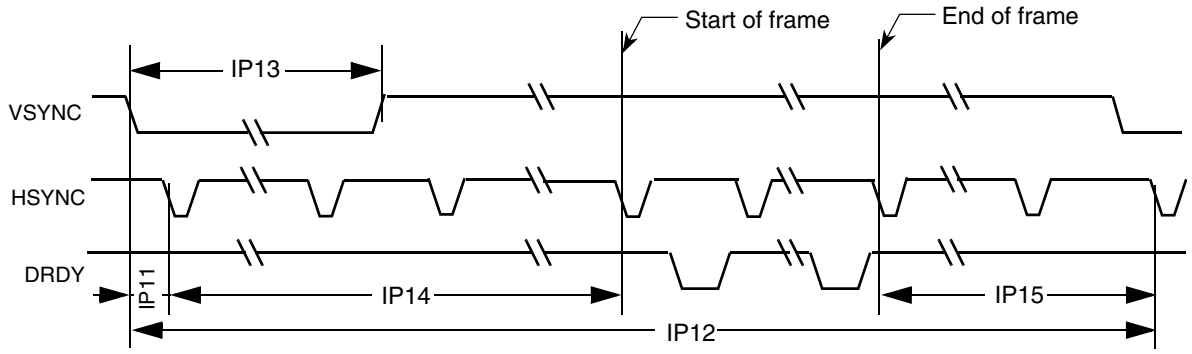


Figure 62. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 59 shows timing characteristics of signals presented in Figure 61 and Figure 62.

Table 59. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	(see[1])	Display interface clock IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.***n***). The DISP_CLK_PER_PIXEL is virtual parameter to define display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to ***n*** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	Width of second vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns

Table 59. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximum accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

The maximum accuracy of UP/DOWN edge of IPP_DISP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

Figure 63 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are register-controlled. Table 60 lists the synchronous display interface timing characteristics.

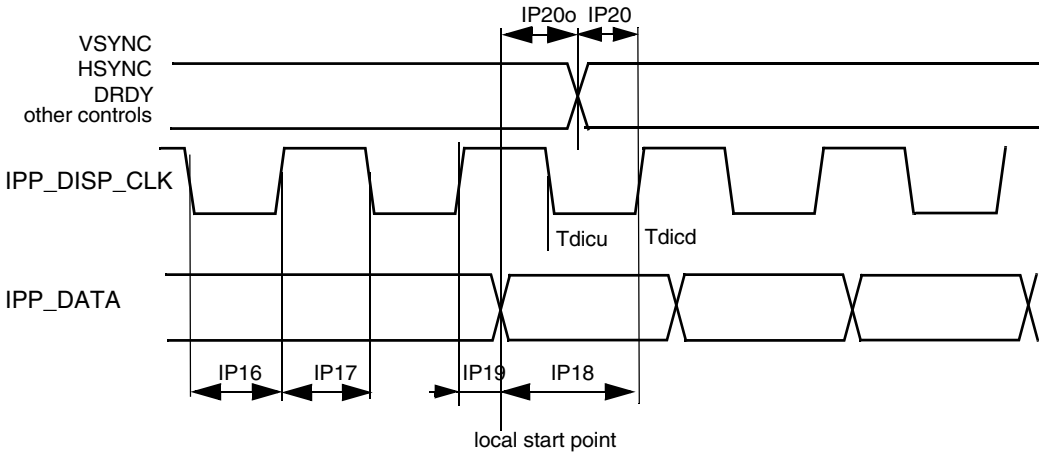


Figure 63. Synchronous Display Interface Timing Diagram—Access Level

Table 60. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defined for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defined for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_DOWN}{DI\_CLK\_PERIOD}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_UP}{DI\_CLK\_PERIOD}\right]\right)$$

4.12.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits."

Table 61. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short-circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and I/O supply voltage	247	454	mV

4.12.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.12.12.1 Electrical and Timing Information

Table 62. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications—Apply to DSI_CLK_P/_N and DSI_DATA_P/_N Inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level	—	—	—	1.45	V
$t_{voh(absmax)}$	Maximum transient time above VOH(absmax)	—	—	—	20	ns

Table 62. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
HS Line Drivers DC Specifications						
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω<= RL< = 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω<= RL< = 125 Ω	—	—	10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω<= RL< = 125 Ω	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	80 Ω<= RL< = 125 Ω	—	—	5	mV
V_{OHHS}	HS output high voltage	80 Ω<= RL< = 125 Ω	—	—	360	mV
Z_{OS}	Single-ended output impedance.	—	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.	—	—	—	10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage	—	-50		50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.	—	110	—	—	Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold	—	—	—	70	mV
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV
Z_{ID}	Differential input impedance	—	80	—	125	Ω

Table 62. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.12.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 64 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

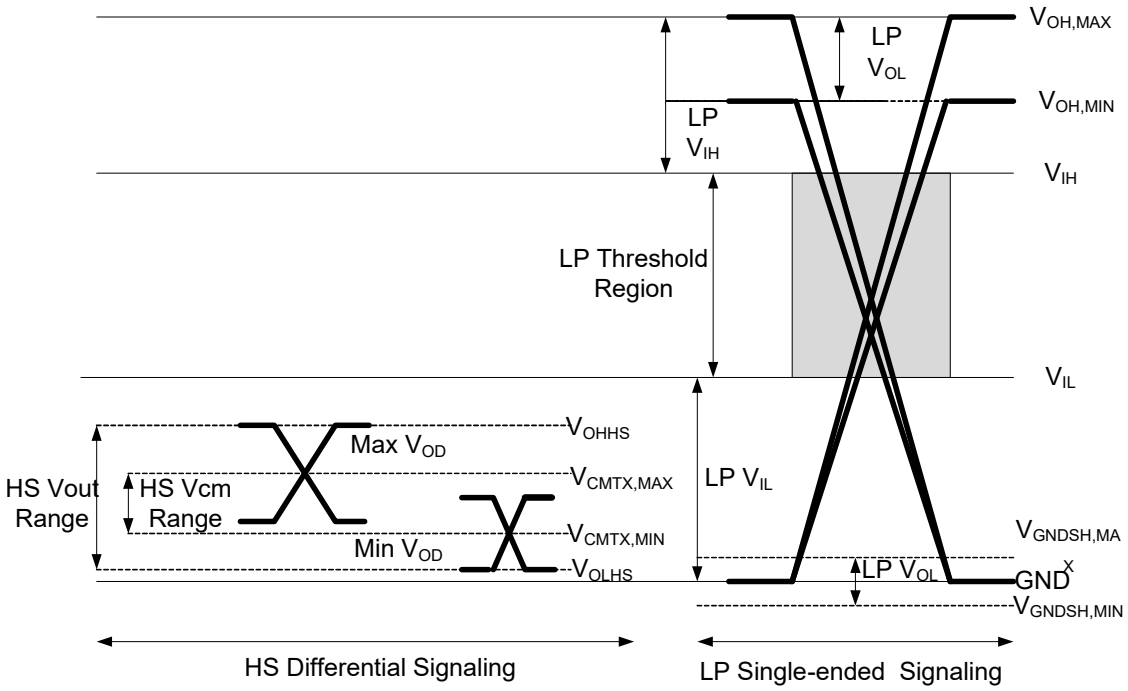


Figure 64. D-PHY Signaling Levels

4.12.12.3 HS Line Driver Characteristics

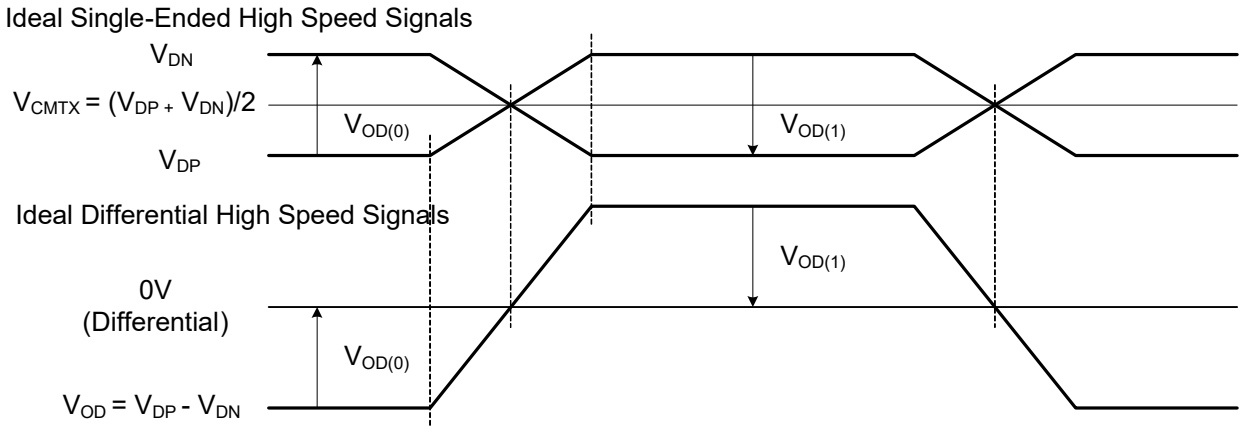


Figure 65. Ideal Single-ended and Resulting Differential HS Signals

4.12.12.4 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

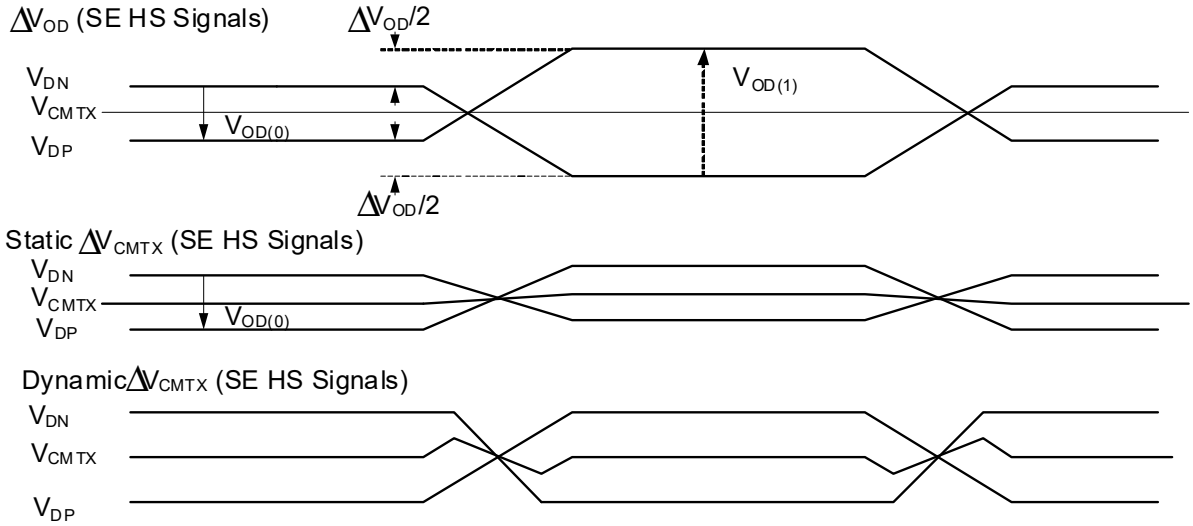


Figure 66. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.12.12.5 D-PHY Switching Characteristics

Table 63. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω <= RL< = 125 Ω	2	—	25	ns

Table 63. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time	—	—	1	—	UI
t_{CPL}	DDR CLK low time	—	—	1	—	UI
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew	—	—	0.075	—	UI
$t_{SKEW[TX]}$	Data to Clock Skew	—	0.350	—	0.650	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω	—	—	15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz	80 Ω<= RL< = 125 Ω	—	—	25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}	—	30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—	—	—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—	—	ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF

Table 63. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
L_S	Equivalent wire bond series inductance	—	—	—	1.5	nH
R_S	Equivalent wire bond series resistance	—	—	—	0.15	Ω
R_L	Load Resistance	—	80	100	125	Ω

4.12.12.6 High-Speed Clock Timing

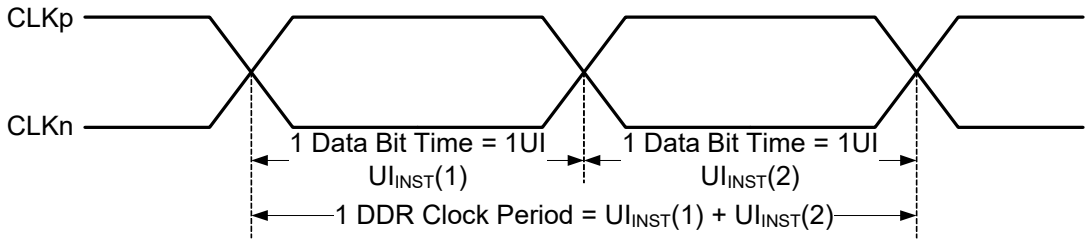


Figure 67. DDR Clock Definition

4.12.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 68:

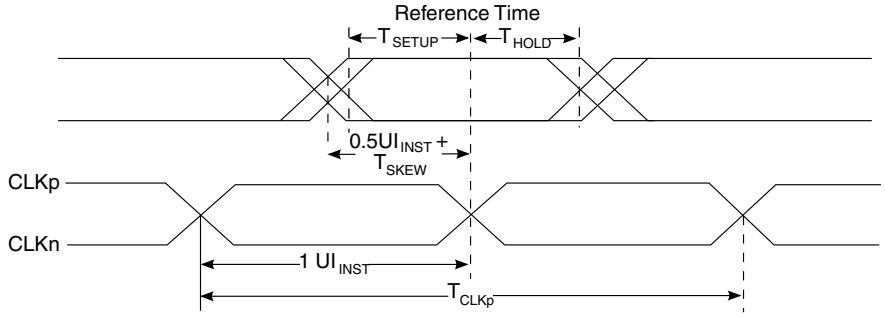


Figure 68. Data to Clock Timing Definitions

4.12.12.8 Reverse High-Speed Data Transmission Timing

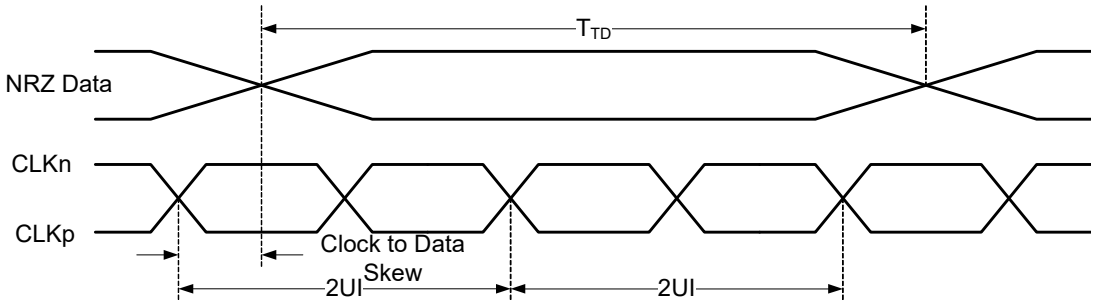


Figure 69. Reverse High-Speed Data Transmission Timing at Slave Side

4.12.12.9 Low-Power Receiver Timing

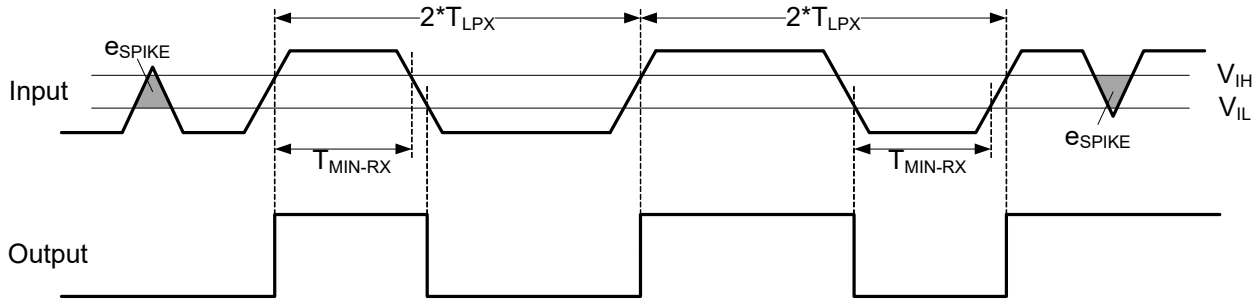


Figure 70. Input Glitch Rejection of Low-Power Receivers

4.12.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.12.13.1 Synchronous Data Flow

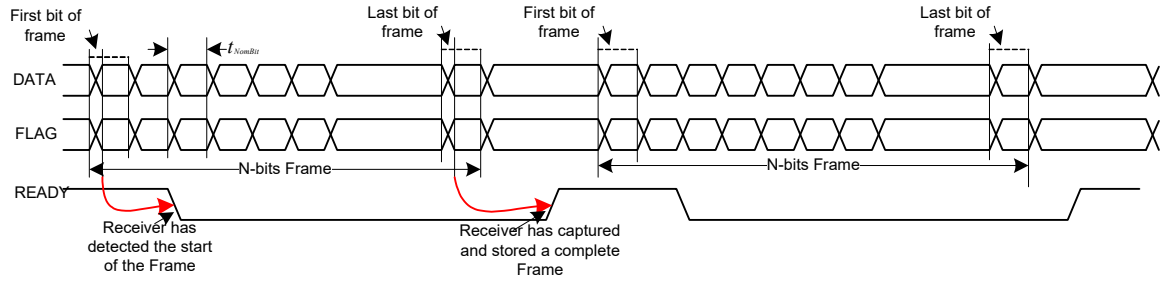


Figure 71. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.12.13.2 Pipelined Data Flow

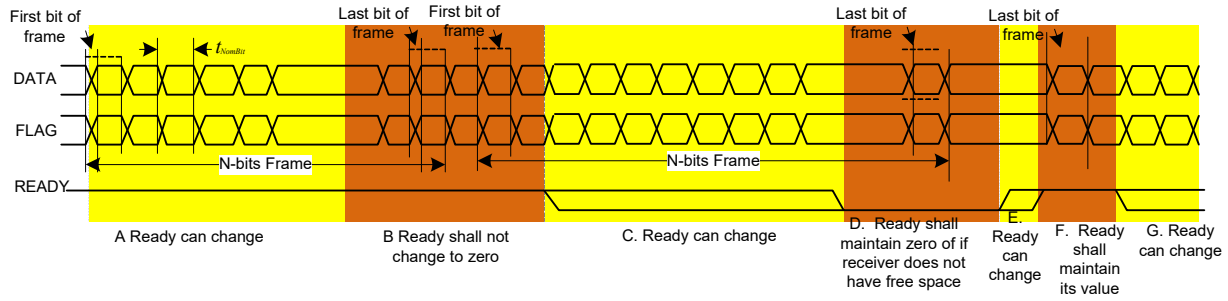


Figure 72. Pipelined Data Flow READY Signal Timing (Frame Transmission Mode)

4.12.13.3 Receiver Real-Time Data Flow

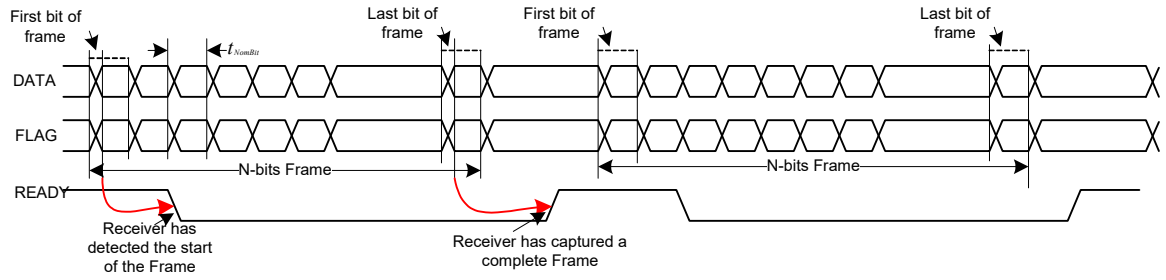


Figure 73. Receiver Real-Time Data Flow READY Signal Timing

4.12.13.4 Synchronized Data Flow Transmission with Wake

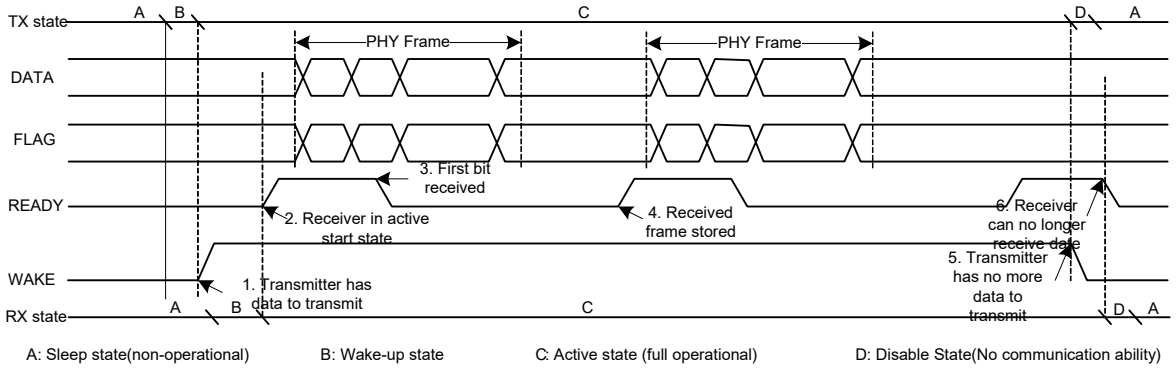


Figure 74. Synchronized Data Flow Transmission with WAKE

4.12.13.5 Stream Transmission Mode Frame Transfer

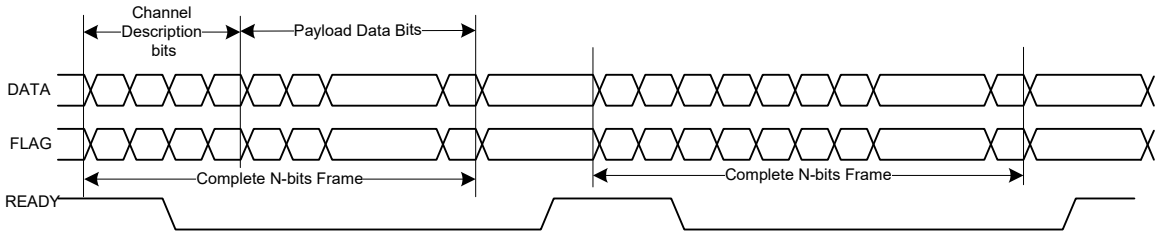


Figure 75. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.12.13.6 Frame Transmission Mode (Synchronized Data Flow)

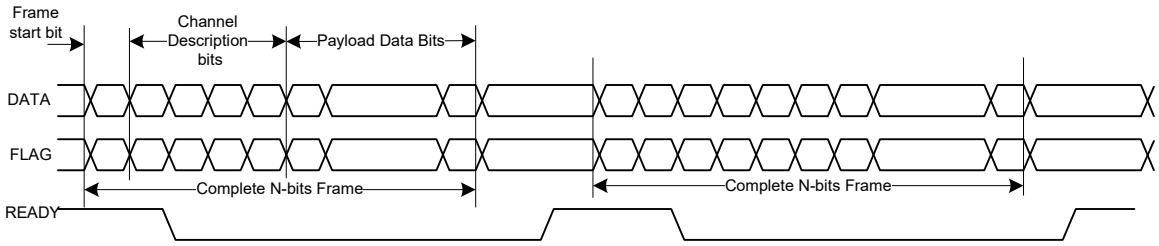


Figure 76. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.12.13.7 Frame Transmission Mode (Pipelined Data Flow)

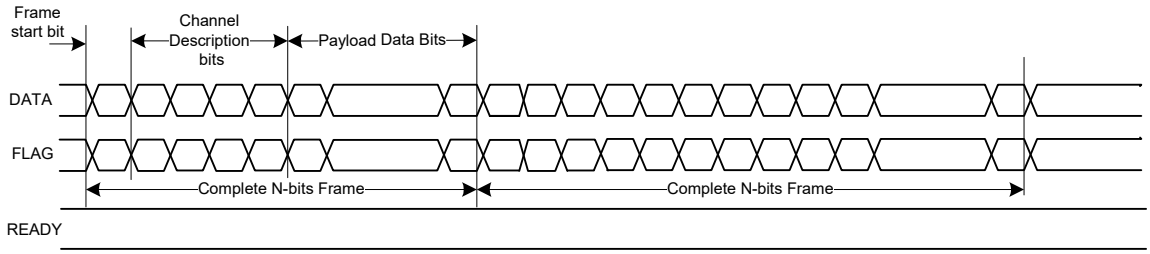


Figure 77. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.12.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 64. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2 ns	2 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50 ns	0.5 ns
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns

4.12.13.9 DATA and FLAG Signal Timing

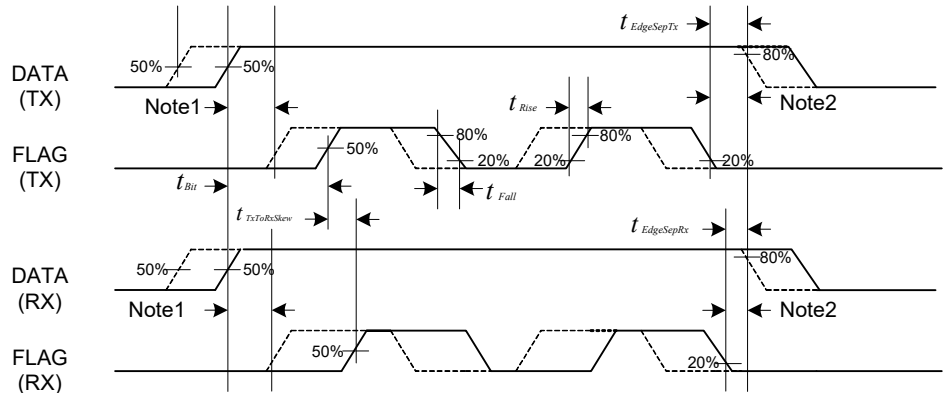


Figure 78. DATA and FLAG Signal Timing

4.12.14 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.12.14.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.12.15 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 79 depicts the timing of the PWM, and Table 65 lists the PWM timing parameters.

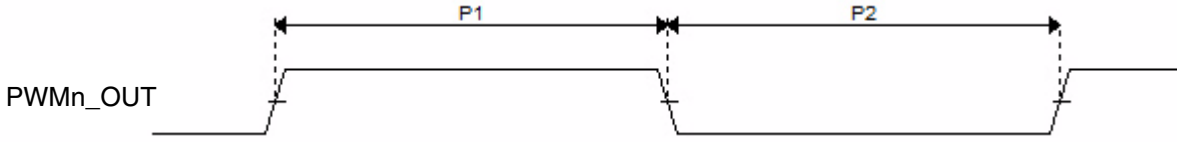


Figure 79. PWM Timing

Table 65. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
—	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.12.16 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.12.16.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

4.12.16.1.1 SATA PHY Transmitter Characteristics

Table 66 provides specifications for SATA PHY transmitter characteristics.

Table 66. SATA PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.12.16.1.2 SATA PHY Receiver Characteristics

Table 67 provides specifications for SATA PHY receiver characteristics.

Table 67. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	175	—	—	mV
Tolerance	PPM	–400	—	400	ppm

4.12.16.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω. 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.12.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 80 depicts the SJC test clock input timing. Figure 81 depicts the SJC boundary scan timing. Figure 82 depicts the SJC test access port. Figure 83 depicts the JTAG_TRST_B timing. Signal parameters are listed in Table 68.

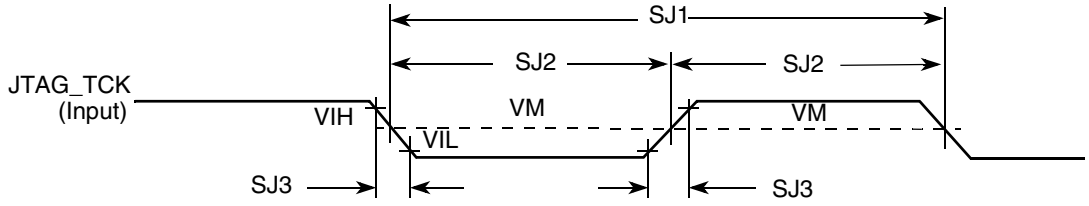


Figure 80. Test Clock Input Timing Diagram

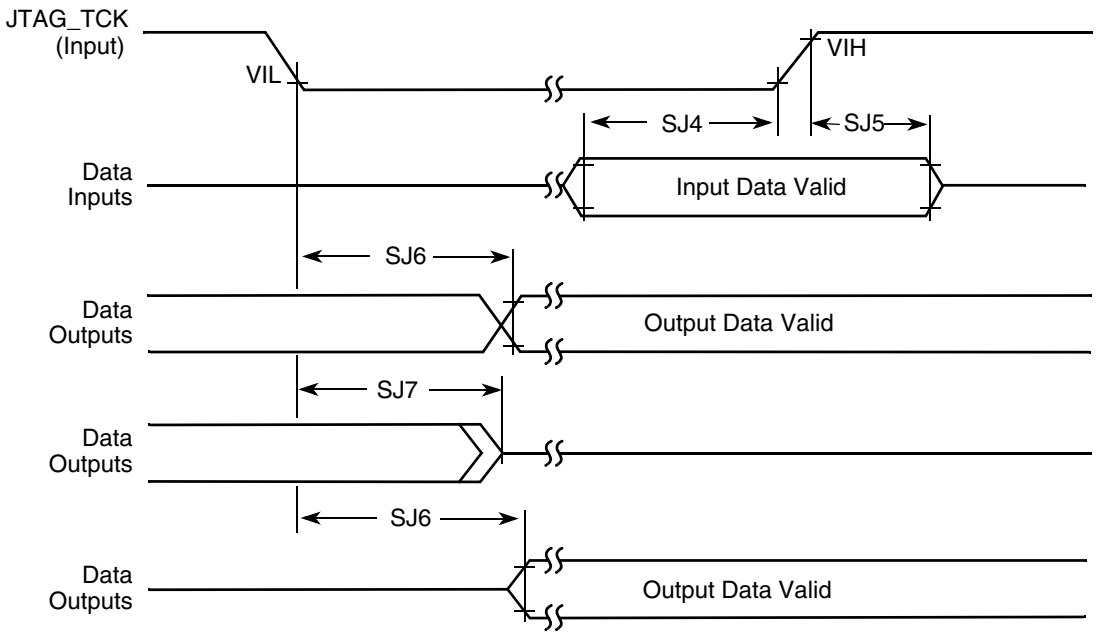


Figure 81. Boundary Scan (JTAG) Timing Diagram

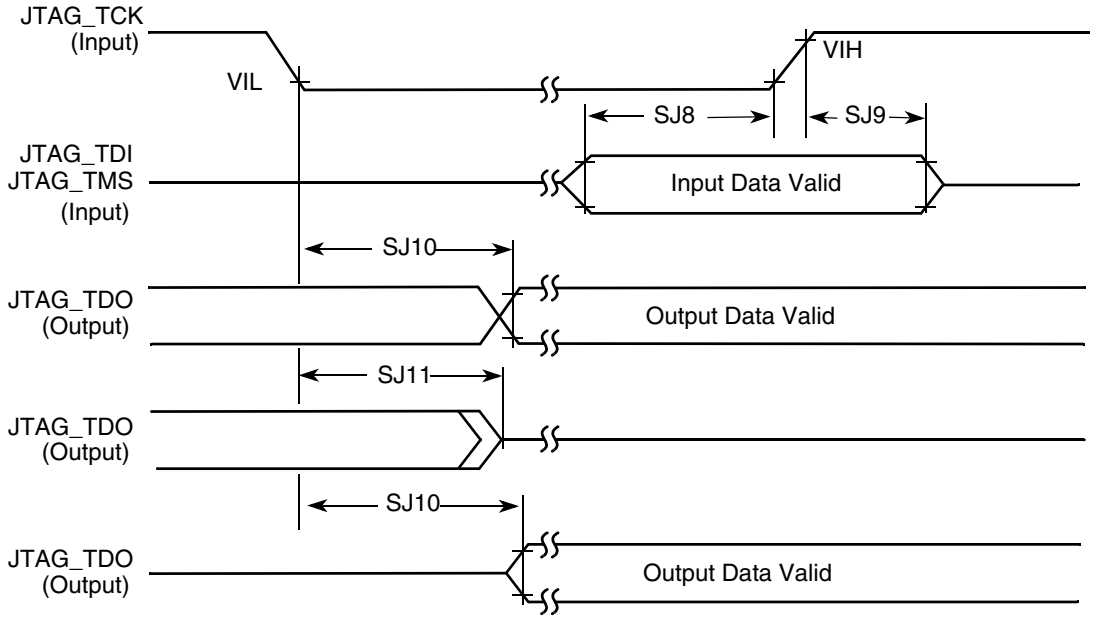


Figure 82. Test Access Port Timing Diagram

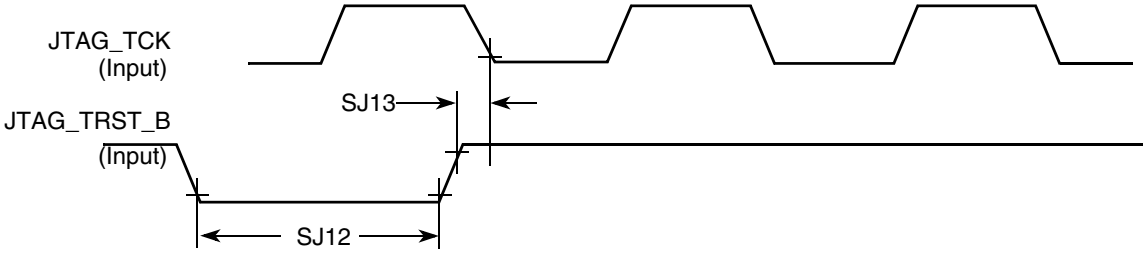


Figure 83. JTAG_TRST_B Timing Diagram

Table 68. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns

Table 68. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.12.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 69 and Figure 84 and Figure 85 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 69. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

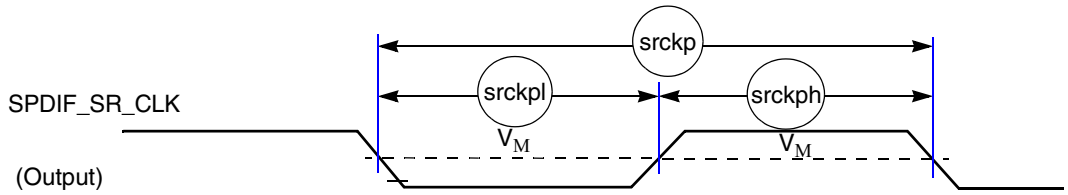


Figure 84. SPDIF_SR_CLK Timing Diagram

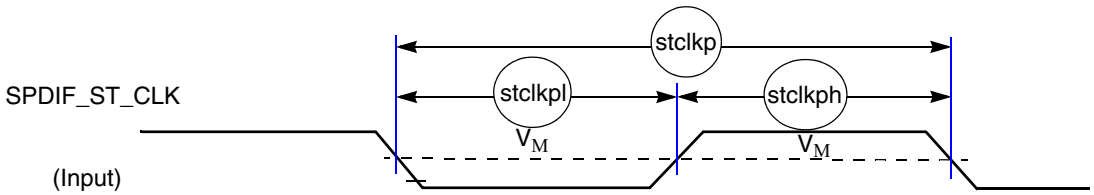


Figure 85. SPDIF_ST_CLK Timing Diagram

4.12.19 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 70.

Table 70. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.12.19.1 SSI Transmitter Timing with Internal Clock

Figure 86 depicts the SSI transmitter internal clock timing and Table 71 lists the timing parameters for the SSI transmitter internal clock.

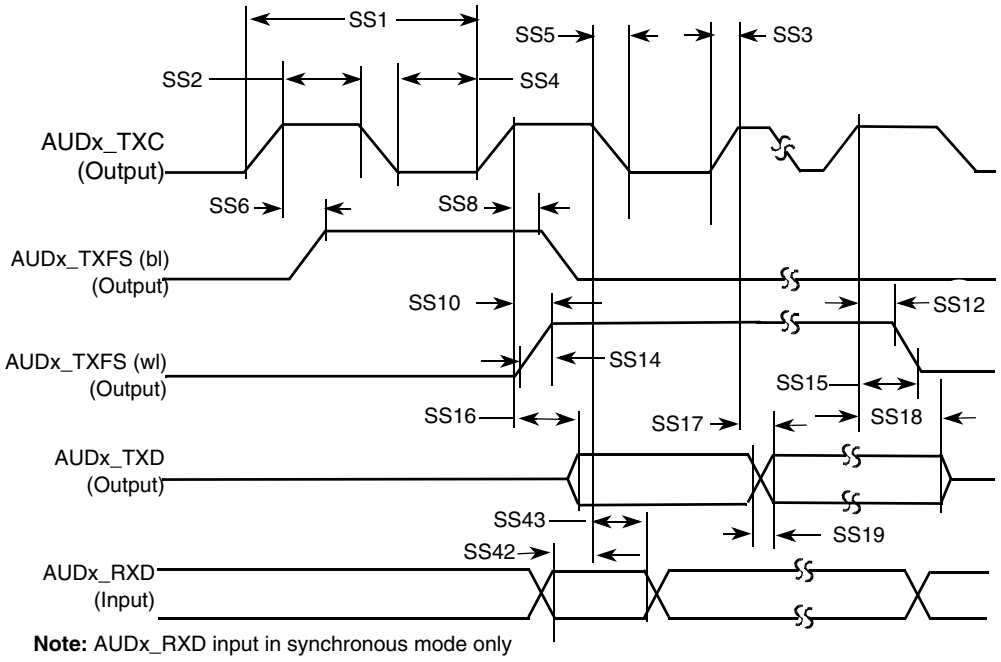


Figure 86. SSI Transmitter Internal Clock Timing Diagram

Table 71. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 71. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is the same as that of transmit data (for example, during AC97 mode of operation).

4.12.19.2 SSI Receiver Timing with Internal Clock

Figure 87 depicts the SSI receiver internal clock timing and Table 72 lists the timing parameters for the receiver timing with the internal clock.

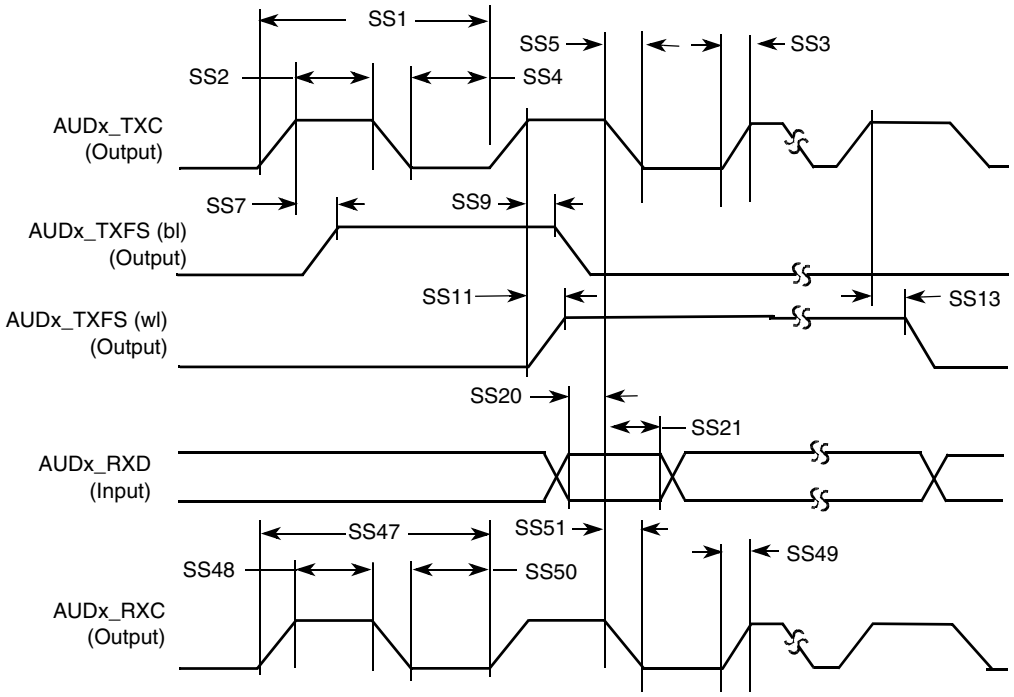


Figure 87. SSI Receiver Internal Clock Timing Diagram

Table 72. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

Table 72. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.19.3 SSI Transmitter Timing with External Clock

Figure 88 depicts the SSI transmitter external clock timing and Table 73 lists the timing parameters for the transmitter timing with the external clock.

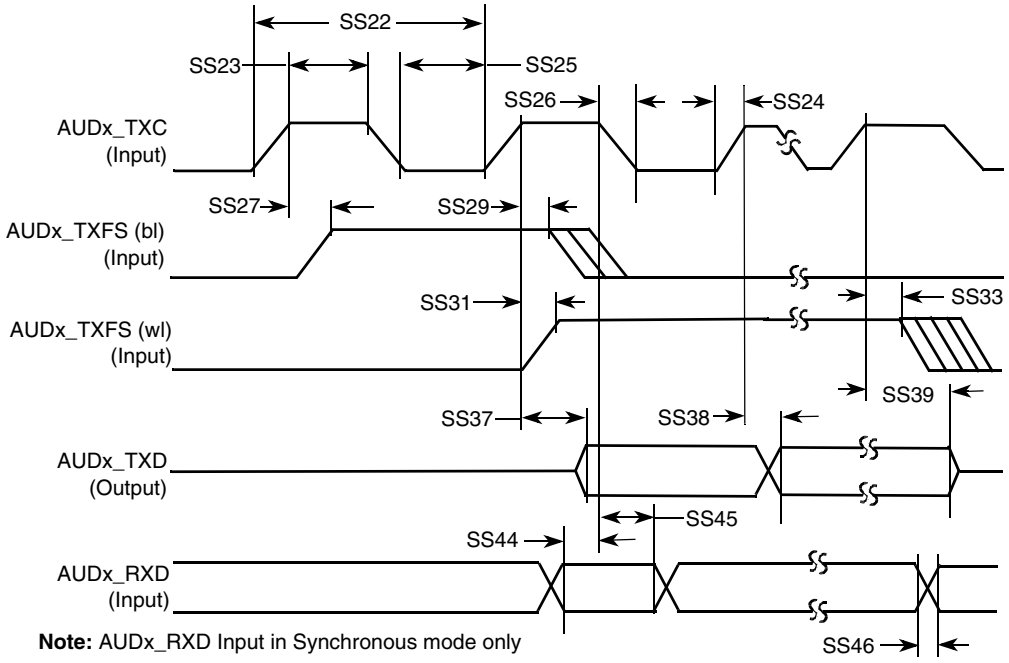


Figure 88. SSI Transmitter External Clock Timing Diagram

Table 73. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

Table 73. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.19.4 SSI Receiver Timing with External Clock

Figure 89 depicts the SSI receiver external clock timing and Table 74 lists the timing parameters for the receiver timing with the external clock.

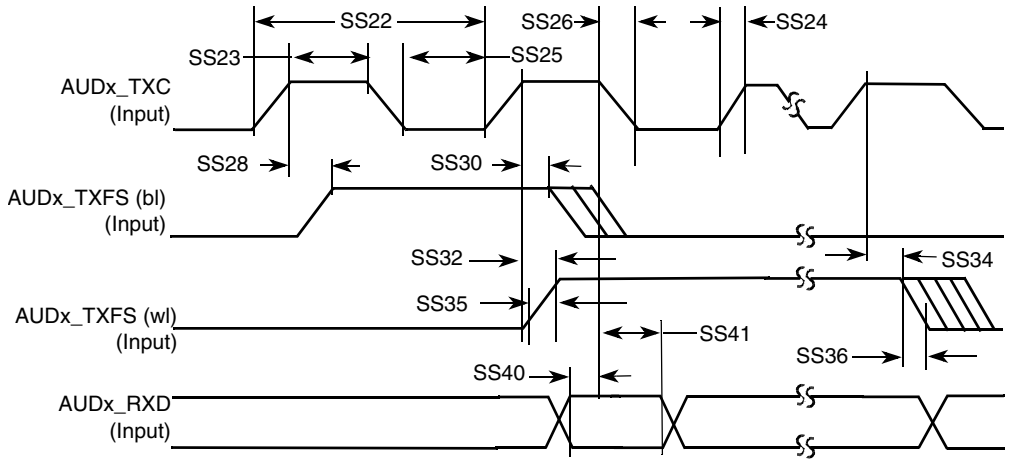


Figure 89. SSI Receiver External Clock Timing Diagram

Table 74. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	–10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	–10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.20 UART I/O Configuration and Timing Parameters

4.12.20.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Dual/6Quad UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 75 shows the UART I/O configuration based on the enabled mode.

Table 75. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.12.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.20.2.1 UART Transmitter

Figure 90 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 76 lists the UART RS-232 serial mode transmit timing characteristics.

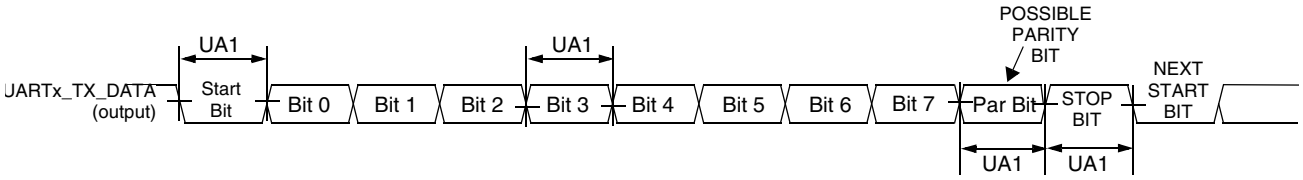


Figure 90. UART RS-232 Serial Mode Transmit Timing Diagram

Table 76. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.12.20.2.2 UART Receiver

Figure 91 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 77 lists serial mode receive timing characteristics.

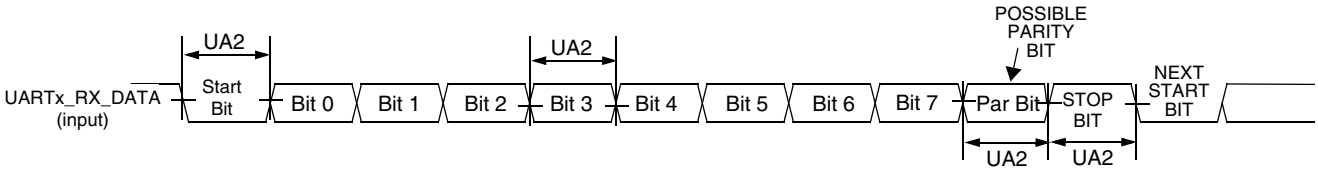


Figure 91. UART RS-232 Serial Mode Receive Timing Diagram

Table 77. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 92 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 78 lists the transmit timing characteristics.

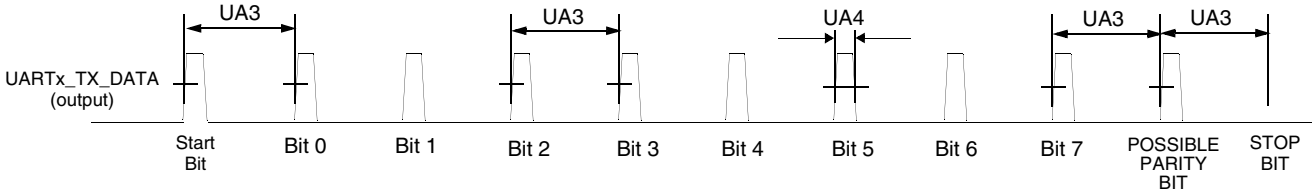


Figure 92. UART IrDA Mode Transmit Timing Diagram

Table 78. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 93 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 79 lists the receive timing characteristics.

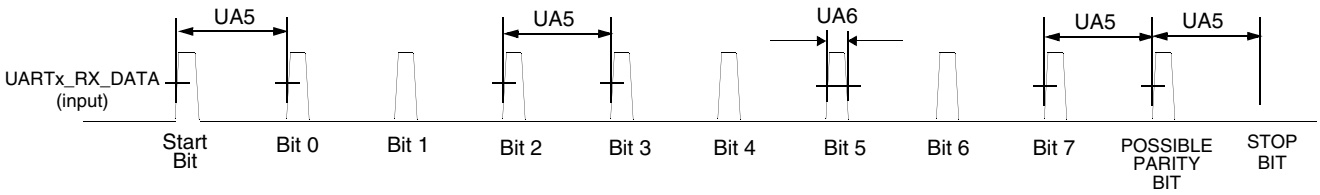


Figure 93. UART IrDA Mode Receive Timing Diagram

Table 79. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is a DDR signal. The following timing specification is for both rising and falling edges.

4.12.21.1 Transmit Timing

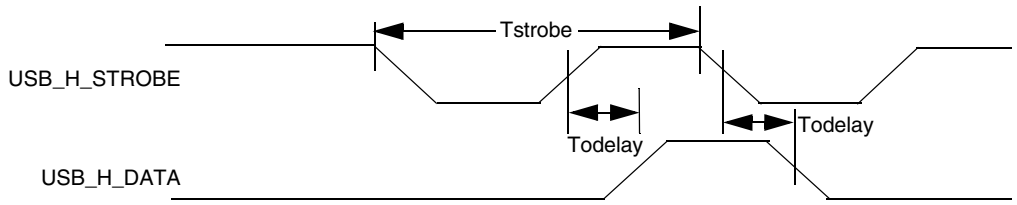


Figure 94. USB HSIC Transmit Waveform

Table 80. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.12.21.2 Receive Timing

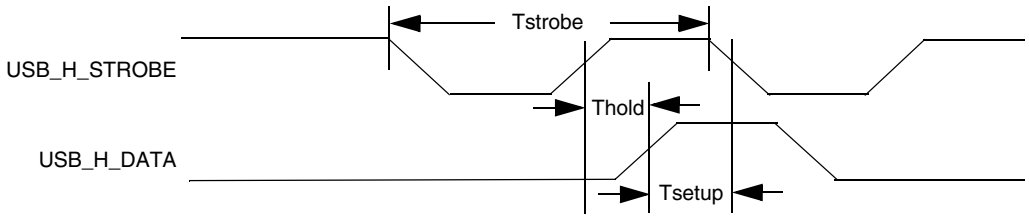


Figure 95. USB HSIC Receive Waveform

Table 81. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.12.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 82 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see i.MX 6Dual/6Quadthe System Boot chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

Table 82. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	Boot Mode Selection
BOOT_MODE0	Input	Boot Mode Selection
Boot Options[1]		
EIM_DA0	Input	BOOT_CFG1[0]
EIM_DA1	Input	BOOT_CFG1[1]
EIM_DA2	Input	BOOT_CFG1[2]
EIM_DA3	Input	BOOT_CFG1[3]
EIM_DA4	Input	BOOT_CFG1[4]
EIM_DA5	Input	BOOT_CFG1[5]
EIM_DA6	Input	BOOT_CFG1[6]
EIM_DA7	Input	BOOT_CFG1[7]
EIM_DA8	Input	BOOT_CFG2[0]
EIM_DA9	Input	BOOT_CFG2[1]
EIM_DA10	Input	BOOT_CFG2[2]
EIM_DA11	Input	BOOT_CFG2[3]
EIM_DA12	Input	BOOT_CFG2[4]
EIM_DA13	Input	BOOT_CFG2[5]
EIM_DA14	Input	BOOT_CFG2[6]
EIM_DA15	Input	BOOT_CFG2[7]
EIM_A16	Input	BOOT_CFG3[0]
EIM_A17	Input	BOOT_CFG3[1]
EIM_A18	Input	BOOT_CFG3[2]

Table 82. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 83 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 83. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3,DISP0_DAT4,DISP0_DAT5,DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

Table 83. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 Signal Naming Convention

The signal names of the i.MX6 series of products are standardized to align the signal names within the family and across the documentation. Benefits of this standardization are as follows:

- Signal names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- Signal names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This standardization applies only to signal names. The ball names are preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

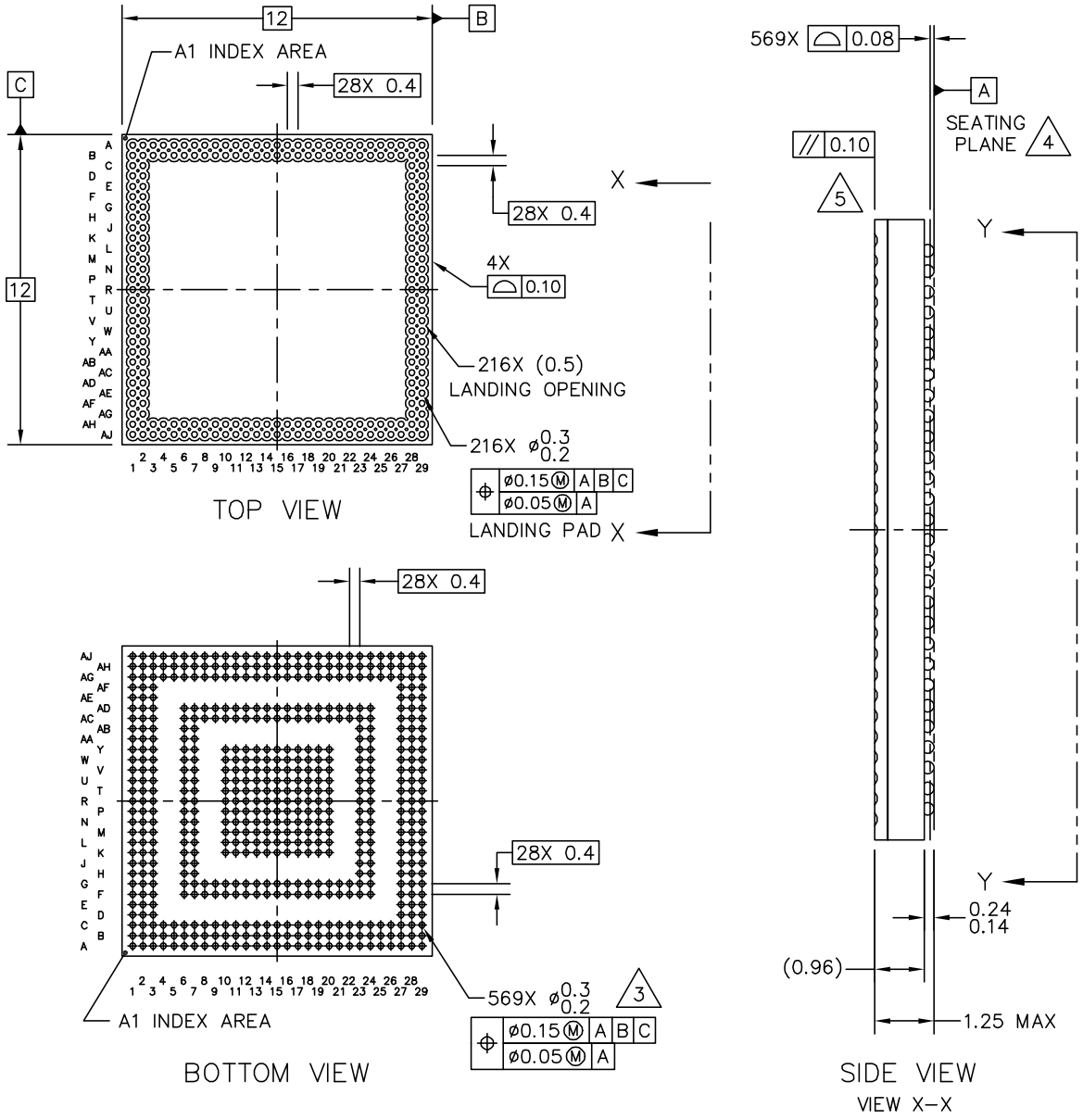
Throughout this document, the signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of signal names is in the document, *IMX 6 Series Standardized Signal Name Map* (EB792). This list can be used to map the signal names used in older documentation to the standardized naming conventions.

6.2 12 x 12 mm Package on Package (PoP) Information

This section contains the outline drawing, signal assignment map, ground/power reference ID (by ball grid location) for the 12 x 12 mm, 0.4 mm pitch PoP package.

6.2.1 Case PoP, 0.4 mm Pitch, 12 x 12 Ball Matrix

Figure 97 and Figure 97 show the top, bottom, and side views of the 12 x 12 mm PoP package.



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TITLE: FCMAPBGA STACKABLE, 12 X 12 X 1.15 PKG, 0.4 MM PITCH, 569 I/O	DOCUMENT NO: 98ASA00383D	REV: A
	STANDARD: NON–JEDEC	
	SOT1644–1	29 FEB 2016

Figure 96. 12 x 12 mm PoP Package Top, Bottom, and Side Views (Sheet 1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK AND LANDING PADS ON TOP SURFACE OF PACKAGE.

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TITLE: FCMAPBGA STACKABLE, 12 X 12 X 1.15 PKG, 0.4 MM PITCH, 569 I/O	DOCUMENT NO: 98ASA00383D	REV: A
	STANDARD: NON–JEDEC	
	SOT1644–1	29 FEB 2016

Figure 97. 12 x 12 mm PoP Package Top, Bottom, and Side Views (Sheet 2 of 2)

6.2.2 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments

Table 84 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 84. 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments

Ball Name	PoP Bottom Ball Position	PoP Top Ball Position	Remark
CSI_REXT	H6	—	—
DNU	—	A1, A29, AJ1, AJ29	—
DRAM_VREF	AG10	B15, R2, U28, AH16	—
DSI_REXT	K6	—	—
FA_ANA	J7	—	This signal should be tied to GND.
GND	A15, A29, B4, C6, D3, F6, F7, H3, K13, K14, K15, L3, L6, L13, L14, L15, M3, M6, M13, M14, M15, N3, N6, N13, N14, N15, P14, R14, R19, R20, T14, T19, T20, U10, U11, U12, U13, U14, U15, U16, U17, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, W13, W14, W17, W18, Y13, Y14, Y17, Y18, AG5, AG7, AG8, AG11, AG13, AH11, AH12, AH13, AH14, AH15, AH16, AH17, AH18, AH19, AJ1, AJ2, AJ11, AJ12, AJ13, AJ14, AJ15, AJ16, AJ17, AJ18, AJ20, AJ29	A2, A6, A9, A11, A14, A28, B1, B14, B21, B24, B29, E28, F1, H28, J1, L29, M2, P1, P2, R28, V2, V28, AA28, AB2, AE2, AF28, AH1, AH5, AH14, AH18, AH29, AJ2, AJ7, AJ11, AJ16, AJ22, AJ28	—
GPANAIO	C10	—	Analog output for NXP use only. This output must remain unconnected.
HDMI_DDCCEC	R2	—	Analog ground reference for the Hot Plug detect signal.
HDMI_REF	P6	—	—
HDMI_VP	M7	—	—
HDMI_VPH	N7	—	—
NC	A1	—	No connect
NVCC_CSI	T7	—	Supply of the camera sensor interface
NVCC_DRAM	Y23, AA23, AB23, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21	—	Supply of the DDR interface
NVCC_EIM0	K23	—	Supply of the EIM interface
NVCC_EIM1	M23	—	Supply of the EIM interface
NVCC_EIM2	P23	—	Supply of the EIM interface
NVCC_ENET	W23	—	Supply of the ENET interface
NVCC_GPIO	W7	—	Supply of the GPIO interface

Table 84. 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments (continued)

Ball Name	PoP Bottom Ball Position	PoP Top Ball Position	Remark
NVCC_JTAG	G6	—	Supply of the JTAG tap controller interface
NVCC_LCD	T23	—	Supply of the LCD interface
NVCC_LVDS2P5	AA7, AG14, AG18, AG20	—	Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered.
NVCC_MIPI	K7	—	Supply of the MIPI interface
NVCC_NANDF	G18	—	Supply of the RAW NAND Flash Memories interface
NVCC_PLL_OUT	C8	—	—
NVCC_RGMII	G23	—	Supply of the ENET interface
NVCC_SD1	G21	—	Supply of the SD card interface
NVCC_SD2	G22	—	Supply of the SD card interface
NVCC_SD3	G16	—	Supply of the SD card interface
PCIE_REXT	A4	—	—
PCIE_VP	H7	—	—
PCIE_VPH	G7	—	PCI PHY supply
PCIE_VPTX	G8	—	PCI PHY supply
POP_VDD1__1	C3	B2, C1	VDD1 supply to the LPDDR2 PoP memory. The bottom side signals are connected to the supply source on the board. The supplies are passed through the i.MX6 PoP package to the LPDDR2 memory VDD1 supplies on the top side.
POP_VDD1__2	C15	A15	
POP_VDD1__3	C27	B28, C28	
POP_VDD1__4	P3	N2, R1	
POP_VDD1__5	R27	P29	
POP_VDD1__6	AG3	AH2	
POP_VDD1__7	AG16	AJ15	
POP_VDD1__8	AG26	AH28	
POP_VDD2__1	C4	A3	VDD2 supply to the LPDDR2 PoP memory. The bottom side signals are connected to the supply source on the board. The supplies are passed through the i.MX6 PoP package to the LPDDR2 memory VDD2 supplies on the top side.
POP_VDD2__2	C16	A16, B16	
POP_VDD2__3	D27	C29	
POP_VDD2__4	P27	P28	
POP_VDD2__5	T3	T1, T2	
POP_VDD2__6	AG4	AH3	
POP_VDD2__7	AG15	AH15	
POP_VDD2__8	AG27	AG28	
POP_VDDCA	T27, AC27, AE27, AG19, AG22, AG25	T28, AC28, AE29, AH22, AJ19, AJ26	VDDCA supply to the LPDDR2 PoP memory. The bottom side signals are connected to the supply source on the board. The supplies are passed through the i.MX6 PoP package to the LPDDR2 memory VDDCA supplies on the top side.

Table 84. 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments (continued)

Ball Name	PoP Bottom Ball Position	PoP Top Ball Position	Remark
POP_VDDQ	C5, C7, C9, C13, C18, C22, C25, E3, E27, G3, J3, J27, M27, U3, Y3, AC3, AF3, AG6, AG9, AG12	A22, B4, B7, B9, B13, B18, B25, D2, D29, F29, G2, J2, J28, M28, U1, Y1, AC1, AF2, AH9, AH12, AJ4, AJ6	VDDQ supply to the LPDDR2 PoP memory. The bottom side signals are connected to the supply source on the board. The supplies are passed through the i.MX6 PoP package to the LPDDR2 memory VDDQ supplies on the top side.
POP_ZQP0	AF27	AG29	Bottom side signal should be connected to an external 240 ohm 1% resistor to ground. The bottom side signal is routed through the package to the top side signal to connect to the memory.
POP_ZQP1	AG17	AJ17	Bottom side signal should be connected to an external 240 ohm 1% resistor to ground. The bottom side signal is routed through the package to the top side signal to connect to the memory.
SATA_REXT	F15	—	—
SATA_VP	G15	—	—
SATA_VPH	G14	—	—
USB_H1_VBUS	C11	—	—
USB_OTG_VBUS	G11	—	—
VDD_CACHE_CAP	P7	—	Cache supply input. This input should be connected to (driven by) VDD_SOC_CAP. The external capacitor used for VDD_SOC_CAP is sufficient for this supply.
VDD_FA	J6	—	This signal must be tied to GND.
VDD_SNVS_CAP	G9	—	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G12	—	Primary supply for the SNVS regulator
VDDARM_CAP	P15, P16, P17, P18, R15, R16, R17, R18, T15, T16, T17, T18	—	Secondary supply for the ARM0 and ARM1 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	K16, K17, K18, L16, L17, L18, M16, M17, M18, N16, N17, N18	—	Primary supply for the ARM0 and ARM1 core regulator
VDDARM23_CAP	P10, P11, P12, P13, R10, R11, R12, R13, T10, T11, T12, T13	—	Secondary supply for the ARM2 and ARM3 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM23_IN	K10, K11, K12, L10, L11, L12, M10, M11, M12, N10, N11, N12	—	Primary supply for the ARM2 and ARM3 core regulator

Table 84. 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments (continued)

Ball Name	PoP Bottom Ball Position	PoP Top Ball Position	Remark
VDDHIGH_CAP	F10, F11	—	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	F8, F9	—	Primary supply for the 2.5 V regulator
VDDPU_CAP	N19, N20, P19, P20, U19, U20, V19, V20	—	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	K19, K20, R6, R7, W10, W11, W12, W15, W16, Y10, Y11, Y12, Y15, Y16	—	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	L19, L20, M19, M20, W19, W20, Y19, Y20	—	Primary supply for the SoC and PU regulators
VDDUSB_CAP	G10	—	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AJ19	—	Connect ZQPAD to an external 240Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.

6.2.3 12 x 12 mm Functional Contact Assignments

Table 85 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 85. 12 x 12 mm Functional Contact Assignments

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
BOOT_MODE0	C14	—	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100k)
BOOT_MODE1	G13	—	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100k)
CLK1_N	A7	—	VDD_HIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	B7	—	VDD_HIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	A6	—	VDD_HIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	B6	—	VDD_HIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	E2	—	NVCC_MIPI	—	—	CSI_CLK_N	—	—
CSI_CLK0P	E1	—	NVCC_MIPI	—	—	CSI_CLK_P	—	—
CSI_D0M	C2	—	NVCC_MIPI	—	—	CSI_DATA0_N	—	—
CSI_D0P	C1	—	NVCC_MIPI	—	—	CSI_DATA0_P	—	—
CSI_D1M	D1	—	NVCC_MIPI	—	—	CSI_DATA1_N	—	—
CSI_D1P	D2	—	NVCC_MIPI	—	—	CSI_DATA1_P	—	—
CSI_D2M	F1	—	NVCC_MIPI	—	—	CSI_DATA2_N	—	—
CSI_D2P	F2	—	NVCC_MIPI	—	—	CSI_DATA2_P	—	—

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
CSI_D3M	G2	—	NVCC_MIPI	—	—	CSI_DATA3_N	—	—
CSI_D3P	G1	—	NVCC_MIPI	—	—	CSI_DATA3_P	—	—
CSI0_DAT4	U6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO22	Input	PU (100k)
CSI0_DAT5	U7	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO23	Input	PU (100k)
CSI0_DAT6	Y1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO24	Input	PU (100k)
CSI0_DAT7	Y2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO25	Input	PU (100k)
CSI0_DAT8	W2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO26	Input	PU (100k)
CSI0_DAT9	W1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO27	Input	PU (100k)
CSI0_DAT10	W3	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	PU (100k)
CSI0_DAT11	V1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	PU (100k)
CSI0_DAT12	V3	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	PU (100k)
CSI0_DAT13	T6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	PU (100k)
CSI0_DAT14	U2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	PU (100k)
CSI0_DAT15	V2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	PU (100k)
CSI0_DAT16	T2	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	PU (100k)
CSI0_DAT17	U1	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO03	Input	PU (100k)
CSI0_DAT18	T1	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO04	Input	PU (100k)
CSI0_DAT19	R3	—	NVCC_CSI	GPIO	ALT5	GPIO6_IO05	Input	PU (100k)
CSI0_DATA_EN	V6	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO20	Input	PU (100k)
CSI0_MCLK	AA2	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO19	Input	PU (100k)
CSI0_PIXCLK	AD1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO18	Input	PU (100k)
CSI0_VSYNC	AA1	—	NVCC_CSI	GPIO	ALT5	GPIO5_IO21	Input	PU (100k)
DI0_DISP_CLK	AF29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO16	Input	PU (100k)
DI0_PIN2	AD29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO18	Input	PU (100k)
DI0_PIN3	W24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO19	Input	PU (100k)
DI0_PIN4	U24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO20	Input	PU (100k)
DI0_PIN15	AD28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO17	Input	PU (100k)
DISP0_DAT0	AH29	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO21	Input	PU (100k)
DISP0_DAT1	AD27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO22	Input	PU (100k)
DISP0_DAT2	AB27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO23	Input	PU (100k)
DISP0_DAT3	V23	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO24	Input	PU (100k)
DISP0_DAT4	V24	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	PU (100k)
DISP0_DAT5	AH27	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	PU (100k)
DISP0_DAT6	U23	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	PU (100k)
DISP0_DAT7	AE28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	PU (100k)
DISP0_DAT8	AJ26	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	PU (100k)
DISP0_DAT9	AG28	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	PU (100k)
DISP0_DAT10	AH26	—	NVCC_LCD	GPIO	ALT5	GPIO4_IO31	Input	PU (100k)
DISP0_DAT11	AJ27	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO05	Input	PU (100k)
DISP0_DAT12	AF28	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO06	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DISP0_DAT13	AJ25	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO07	Input	PU (100k)
DISP0_DAT14	AJ28	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO08	Input	PU (100k)
DISP0_DAT15	AH25	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO09	Input	PU (100k)
DISP0_DAT16	AB24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO10	Input	PU (100k)
DISP0_DAT17	AH28	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO11	Input	PU (100k)
DISP0_DAT18	AH24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO12	Input	PU (100k)
DISP0_DAT19	AA24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO13	Input	PU (100k)
DISP0_DAT20	AD24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO14	Input	PU (100k)
DISP0_DAT21	AC24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO15	Input	PU (100k)
DISP0_DAT22	Y24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO16	Input	PU (100k)
DISP0_DAT23	AJ24	—	NVCC_LCD	GPIO	ALT5	GPIO5_IO17	Input	PU (100k)
DRAM_CA0P0	—	R29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA0_P0	Output	0
DRAM_CA0P1	—	AJ27	NVCC_DRAM	DDR	ALT0	LPDDR2_CA0_P1	Output	0
DRAM_CA1P0	—	T29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA1_P0	Output	0
DRAM_CA1P1	—	AH27	NVCC_DRAM	DDR	ALT0	LPDDR2_CA1_P1	Output	0
DRAM_CA2P0	—	U29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA2_P0	Output	0
DRAM_CA2P1	—	AH26	NVCC_DRAM	DDR	ALT0	LPDDR2_CA2_P1	Output	0
DRAM_CA3P0	—	V29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA3_P0	Output	0
DRAM_CA3P1	—	AH25	NVCC_DRAM	DDR	ALT0	LPDDR2_CA3_P1	Output	0
DRAM_CA4P0	—	W28	NVCC_DRAM	DDR	ALT0	LPDDR2_CA4_P0	Output	0
DRAM_CA4P1	—	AJ25	NVCC_DRAM	DDR	ALT0	LPDDR2_CA4_P1	Output	0
DRAM_CA5P0	—	AC29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA5_P0	Output	0
DRAM_CA5P1	—	AJ20	NVCC_DRAM	DDR	ALT0	LPDDR2_CA5_P1	Output	0
DRAM_CA6P0	—	AD29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA6_P0	Output	0
DRAM_CA6P1	—	AH20	NVCC_DRAM	DDR	ALT0	LPDDR2_CA6_P1	Output	0
DRAM_CA7P0	—	AD28	NVCC_DRAM	DDR	ALT0	LPDDR2_CA7_P0	Output	0
DRAM_CA7P1	—	AH19	NVCC_DRAM	DDR	ALT0	LPDDR2_CA7_P1	Output	0
DRAM_CA8P0	—	AE28	NVCC_DRAM	DDR	ALT0	LPDDR2_CA8_P0	Output	0
DRAM_CA8P1	—	AJ18	NVCC_DRAM	DDR	ALT0	LPDDR2_CA8_P1	Output	0
DRAM_CA9P0	—	AF29	NVCC_DRAM	DDR	ALT0	LPDDR2_CA9_P0	Output	0
DRAM_CA9P1	—	AH17	NVCC_DRAM	DDR	ALT0	LPDDR2_CA9_P1	Output	0
DRAM_CKE0P0	AA29	AA29	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE0_P0	Output	Bottom side signals: DRAM_CKE0P0, DRAM_CKE0P1, DRAM_CKE1P0 & DRAM_1CKE1P0 must connect to ground through a 10 kohm resistor.
DRAM_CKE0P1	AH23	AH23	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE0_P1	Output	
DRAM_CKE1P0	Y29	Y29	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE1_P0	Output	
DRAM_CKE1P1	AJ23	AJ23	NVCC_DRAM	DDR	ALT0	LPDDR2_CKE1_P1	Output	
DRAM_CLKP0	—	AB28	NVCC_DRAM	DDRCLK	ALT0	LPDDR2_CK_P0	Input	Hi-Z
DRAM_CLKP0_B	—	AB29	NVCC_DRAM	—	—	LPDDR2_CK_P0_B	—	—
DRAM_CLKP1	—	AJ21	NVCC_DRAM	DDRCLK	ALT0	LPDDR2_CK_P1	Input	Hi-Z

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DRAM_CLKP1_B	—	AH21	NVCC_DRAM	—	—	LPDDR2_CK_P1_B	—	—
DRAM_CS0P0	—	Y28	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B0_P0	Output	0
DRAM_CS1P0	—	W29	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B1_P0	Output	0
DRAM_CS0P1	—	AH24	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B0_P1	Output	0
DRAM_CS1P1	—	AJ24	NVCC_DRAM	DDR	ALT0	LPDDR2_CS_B1_P1	Output	0
DRAM_D0P0	—	U2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	PU (100k)
DRAM_D1P0	—	N1	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	PU (100k)
DRAM_D2P0	—	M1	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100k)
DRAM_D3P0	—	Y2	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100k)
DRAM_D4P0	—	V1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100k)
DRAM_D5P0	—	W1	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	PU (100k)
DRAM_D6P0	—	W2	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	PU (100k)
DRAM_D7P0	—	L2	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	PU (100k)
DRAM_D8P0	—	AJ3	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	PU (100k)
DRAM_D9P0	—	AH4	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	PU (100k)
DRAM_D10P0	—	AG1	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	PU (100k)
DRAM_D11P0	—	AH6	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100k)
DRAM_D12P0	—	AE1	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100k)
DRAM_D13P0	—	AG2	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100k)
DRAM_D14P0	—	AF1	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100k)
DRAM_D15P0	—	AJ5	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100k)
DRAM_D16P0	—	H2	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100k)
DRAM_D17P0	—	F2	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100k)
DRAM_D18P0	—	C2	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100k)
DRAM_D19P0	—	E1	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100k)
DRAM_D20P0	—	H1	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100k)
DRAM_D21P0	—	G1	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100k)
DRAM_D22P0	—	E2	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100k)
DRAM_D23P0	—	D1	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100k)
DRAM_D24P0	—	AH11	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100k)
DRAM_D25P0	—	AJ9	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100k)
DRAM_D26P0	—	AJ14	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100k)
DRAM_D27P0	—	AJ12	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100k)
DRAM_D28P0	—	AH10	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100k)
DRAM_D29P0	—	AJ10	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100k)
DRAM_D30P0	—	AJ13	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100k)
DRAM_D31P0	—	AH13	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100k)
DRAM_D0P1	—	B3	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	PU (100k)
DRAM_D1P1	—	A7	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	PU (100k)
DRAM_D2P1	—	A4	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DRAM_D3P1	—	B5	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	PU (100k)
DRAM_D4P1	—	A5	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	PU (100k)
DRAM_D5P1	—	A8	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	PU (100k)
DRAM_D6P1	—	B8	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	PU (100k)
DRAM_D7P1	—	B6	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	PU (100k)
DRAM_D8P1	—	A18	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100k)
DRAM_D9P1	—	A13	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100k)
DRAM_D10P1	—	B19	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100k)
DRAM_D11P1	—	A12	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100k)
DRAM_D12P1	—	A19	NVCC_DRAM	DDR	ALT0	DRAM_DATA44	Input	PU (100k)
DRAM_D13P1	—	A17	NVCC_DRAM	DDR	ALT0	DRAM_DATA45	Input	PU (100k)
DRAM_D14P1	—	B12	NVCC_DRAM	DDR	ALT0	DRAM_DATA46	Input	PU (100k)
DRAM_D15P1	—	B17	NVCC_DRAM	DDR	ALT0	DRAM_DATA47	Input	PU (100k)
DRAM_D16P1	—	E29	NVCC_DRAM	DDR	ALT0	DRAM_DATA48	Input	PU (100k)
DRAM_D17P1	—	A24	NVCC_DRAM	DDR	ALT0	DRAM_DATA49	Input	PU (100k)
DRAM_D18P1	—	A27	NVCC_DRAM	DDR	ALT0	DRAM_DATA50	Input	PU (100k)
DRAM_D19P1	—	A26	NVCC_DRAM	DDR	ALT0	DRAM_DATA51	Input	PU (100k)
DRAM_D20P1	—	B27	NVCC_DRAM	DDR	ALT0	DRAM_DATA52	Input	PU (100k)
DRAM_D21P1	—	D28	NVCC_DRAM	DDR	ALT0	DRAM_DATA53	Input	PU (100k)
DRAM_D22P1	—	B26	NVCC_DRAM	DDR	ALT0	DRAM_DATA54	Input	PU (100k)
DRAM_D23P1	—	A25	NVCC_DRAM	DDR	ALT0	DRAM_DATA55	Input	PU (100k)
DRAM_D24P1	—	K28	NVCC_DRAM	DDR	ALT0	DRAM_DATA56	Input	PU (100k)
DRAM_D25P1	—	N29	NVCC_DRAM	DDR	ALT0	DRAM_DATA57	Input	PU (100k)
DRAM_D26P1	—	H29	NVCC_DRAM	DDR	ALT0	DRAM_DATA58	Input	PU (100k)
DRAM_D27P1	—	L28	NVCC_DRAM	DDR	ALT0	DRAM_DATA59	Input	PU (100k)
DRAM_D28P1	—	M29	NVCC_DRAM	DDR	ALT0	DRAM_DATA60	Input	PU (100k)
DRAM_D29P1	—	N28	NVCC_DRAM	DDR	ALT0	DRAM_DATA61	Input	PU (100k)
DRAM_D30P1	—	K29	NVCC_DRAM	DDR	ALT0	DRAM_DATA62	Input	PU (100k)
DRAM_D31P1	—	J29	NVCC_DRAM	DDR	ALT0	DRAM_DATA63	Input	PU (100k)
DRAM_DM0P0	—	AB1	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	0
DRAM_DM1P0	—	AC2	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	0
DRAM_DM2P0	—	L1	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	0
DRAM_DM3P0	—	AH7	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	0
DRAM_DM0P1	—	B11	NVCC_DRAM	DDR	ALT0	DRAM_DQM4	Output	0
DRAM_DM1P1	—	A21	NVCC_DRAM	DDR	ALT0	DRAM_DQM5	Output	0
DRAM_DM2P1	—	B22	NVCC_DRAM	DDR	ALT0	DRAM_DQM6	Output	0
DRAM_DM3P1	—	F28	NVCC_DRAM	DDR	ALT0	DRAM_DQM7	Output	0
DRAM_DQS0P0	—	AA1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z
DRAM_DQS0P0_B	—	AA2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS0_N	—	—
DRAM_DQS1P0	—	AD2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	Hi-Z

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
DRAM_DQS1P0_B	—	AD1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_N	—	—
DRAM_DQS2P0	—	K2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS2_P	Input	Hi-Z
DRAM_DQS2P0_B	—	K1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_N	—	—
DRAM_DQS3P0	—	AH8	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS3_P	Input	Hi-Z
DRAM_DQS3P0_B	—	AJ8	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_N	—	—
DRAM_DQS0P1	—	B10	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS4_P	Input	Hi-Z
DRAM_DQS0P1_B	—	A10	NVCC_DRAM	DDRCLK	—	DRAM_SDQS4_N	—	—
DRAM_DQS1P1	—	A20	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS5_P	Input	Hi-Z
DRAM_DQS1P1_B	—	B20	NVCC_DRAM	DDRCLK	—	DRAM_SDQS5_N	—	—
DRAM_DQS2P1	—	A23	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS6_P	Input	Hi-Z
DRAM_DQS2P1_B	—	B23	NVCC_DRAM	DDRCLK	—	DRAM_SDQS6_N	—	—
DRAM_DQS3P1	—	G28	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS7_P	Input	Hi-Z
DRAM_DQS3P1_B	—	G29	NVCC_DRAM	DDRCLK	—	DRAM_SDQS7_N	—	—
DSI_CLK0M	J1	—	NVCC_MIPI	—	—	DSI_CLK_N	—	—
DSI_CLK0P	J2	—	NVCC_MIPI	—	—	DSI_CLK_P	—	—
DSI_D0M	H2	—	NVCC_MIPI	—	—	DSI_DATA0_N	—	—
DSI_D0P	H1	—	NVCC_MIPI	—	—	DSI_DATA0_P	—	—
DSI_D1M	K2	—	NVCC_MIPI	—	—	DSI_DATA1_N	—	—
DSI_D1P	K1	—	NVCC_MIPI	—	—	DSI_DATA1_P	—	—
EIM_A16	T29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR16	Output	0
EIM_A17	N24	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR17	Output	0
EIM_A18	M24	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR18	Output	0
EIM_A19	R28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR19	Output	0
EIM_A20	R29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR20	Output	0
EIM_A21	P29	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR21	Output	0
EIM_A22	P28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR22	Output	0
EIM_A23	N28	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR23	Output	0
EIM_A24	N27	—	NVCC_EIM1	GPIO	ALT0	EIM_ADDR24	Output	0
EIM_A25	H28	—	NVCC_EIM0	GPIO	ALT0	EIM_ADDR25	Output	0
EIM_BCLK	AA27	—	NVCC_EIM2	GPIO	ALT0	EIM_BCLK	Output	0
EIM_CS0	U29	—	NVCC_EIM1	GPIO	ALT0	EIM_CS0_B	Output	1
EIM_CS1	U28	—	NVCC_EIM1	GPIO	ALT0	EIM_CS1_B	Output	1
EIM_D16	J24	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO16	Input	PU (100k)
EIM_D17	H29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO17	Input	PU (100k)
EIM_D18	J28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO18	Input	PU (100k)
EIM_D19	J29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO19	Input	PU (100k)
EIM_D20	J23	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO20	Input	PU (100k)
EIM_D21	K29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO21	Input	PU (100k)
EIM_D22	K28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO22	Input	PU (100k)
EIM_D23	K24	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO23	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
EIM_D24	L29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO24	Input	PU (100k)
EIM_D25	L28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO25	Input	PU (100k)
EIM_D26	L27	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO26	Input	PU (100k)
EIM_D27	M28	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO27	Input	PU (100k)
EIM_D28	M29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO28	Input	PU (100k)
EIM_D29	L24	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO29	Input	PU (100k)
EIM_D30	N29	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO30	Input	PU (100k)
EIM_D31	L23	—	NVCC_EIM0	GPIO	ALT5	GPIO3_IO31	Input	PD (100k)
EIM_DA0	V28	—	NVCC_EIM2	GPIO	ALT0	EIM_AD00	Input	PU (100k)
EIM_DA1	V27	—	NVCC_EIM2	GPIO	ALT0	EIM_AD01	Input	PU (100k)
EIM_DA2	W29	—	NVCC_EIM2	GPIO	ALT0	EIM_AD02	Input	PU (100k)
EIM_DA3	AB29	—	NVCC_EIM2	GPIO	ALT0	EIM_AD03	Input	PU (100k)
EIM_DA4	W27	—	NVCC_EIM2	GPIO	ALT0	EIM_AD04	Input	PU (100k)
EIM_DA5	W28	—	NVCC_EIM2	GPIO	ALT0	EIM_AD05	Input	PU (100k)
EIM_DA6	T24	—	NVCC_EIM2	GPIO	ALT0	EIM_AD06	Input	PU (100k)
EIM_DA7	R24	—	NVCC_EIM2	GPIO	ALT0	EIM_AD07	Input	PU (100k)
EIM_DA8	AB28	—	NVCC_EIM2	GPIO	ALT0	EIM_AD08	Input	PU (100k)
EIM_DA9	AC29	—	NVCC_EIM2	GPIO	ALT0	EIM_AD09	Input	PU (100k)
EIM_DA10	Y28	—	NVCC_EIM2	GPIO	ALT0	EIM_AD10	Input	PU (100k)
EIM_DA11	AE29	—	NVCC_EIM2	GPIO	ALT0	EIM_AD11	Input	PU (100k)
EIM_DA12	Y27	—	NVCC_EIM2	GPIO	ALT0	EIM_AD12	Input	PU (100k)
EIM_DA13	R23	—	NVCC_EIM2	GPIO	ALT0	EIM_AD13	Input	PU (100k)
EIM_DA14	AC28	—	NVCC_EIM2	GPIO	ALT0	EIM_AD14	Input	PU (100k)
EIM_DA15	AA28	—	NVCC_EIM2	GPIO	ALT0	EIM_AD15	Input	PU (100k)
EIM_EB0	N23	—	NVCC_EIM2	GPIO	ALT0	EIM_EB0_B	Output	1
EIM_EB1	P24	—	NVCC_EIM2	GPIO	ALT0	EIM_EB1_B	Output	1
EIM_EB2	H27	—	NVCC_EIM0	GPIO	ALT5	GPIO2_IO30	Input	PU (100k)
EIM_EB3	K27	—	NVCC_EIM0	GPIO	ALT5	GPIO2_IO31	Input	PU (100k)
EIM_LBA	V29	—	NVCC_EIM1	GPIO	ALT0	EIM_LBA_B	Output	1
EIM_OE	T28	—	NVCC_EIM1	GPIO	ALT0	EIM_OE	Output	1
EIM_RW	U27	—	NVCC_EIM1	GPIO	ALT0	EIM_RW	Output	1
EIM_WAIT	AG29	—	NVCC_EIM2	GPIO	ALT0	EIM_WAIT	Input	PU (100k)
ENET_CRS_DV	AG23	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	PU (100k)
ENET_MDC	AJ21	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	PU (100k)
ENET_MDIO	AJ22	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	PU (100k)
ENET_REF_CLK[3]	AH21	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	PU (100k)
ENET_RX_ER	AD22	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	PU (100k)
ENET_RXD0	AH22	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	PU (100k)
ENET_RXD1	AH20	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	PU (100k)
ENET_TX_EN	AG24	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
ENET_TXD0	AD23	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	PU (100k)
ENET_TXD1	AG21	—	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	PU (100k)
GPIO_0	AE2	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	PD (100k)
GPIO_1	AA6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	PU (100k)
GPIO_2	W6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	PU (100k)
GPIO_3	AE1	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	PU (100k)
GPIO_4	Y6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	PU (100k)
GPIO_5	AB3	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	PU (100k)
GPIO_6	AC6	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	PU (100k)
GPIO_7	AC1	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	PU (100k)
GPIO_8	V7	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	PU (100k)
GPIO_9	AD2	—	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	PU (100k)
GPIO_16	AB2	—	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	PU (100k)
GPIO_17	AC2	—	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	PU (100k)
GPIO_18	AA3	—	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	PU (100k)
GPIO_19	AB1	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	PU (100k)
HDMI_CLKM	L1	—	HDMI_VPH	—	—	HDMI_TX_CLK_N	—	—
HDMI_CLKP	L2	—	HDMI_VPH	—	—	HDMI_TX_CLK_P	—	—
HDMI_D0M	M1	—	HDMI_VPH	—	—	HDMI_TX_DATA0_N	—	—
HDMI_D0P	M2	—	HDMI_VPH	—	—	HDMI_TX_DATA0_P	—	—
HDMI_D1M	N1	—	HDMI_VPH	—	—	HDMI_TX_DATA1_N	—	—
HDMI_D1P	N2	—	HDMI_VPH	—	—	HDMI_TX_DATA1_P	—	—
HDMI_D2M	P1	—	HDMI_VPH	—	—	HDMI_TX_DATA2_N	—	—
HDMI_D2P	P2	—	HDMI_VPH	—	—	HDMI_TX_DATA2_P	—	—
HDMI_HPD	R1	—	HDMI_VPH	—	—	HDMI_TX_HPD	—	—
JTAG_MOD	F3	—	NVCC_JTAG	GPIO	ALT0	JTAG_MODE	Input	PU (100k)
JTAG_TCK	B1	—	NVCC_JTAG	GPIO	ALT0	JTAG_TCK	Input	PU (47k)
JTAG_TDI	L7	—	NVCC_JTAG	GPIO	ALT0	JTAG_TDI	Input	PU (47k)
JTAG_TDO	B2	—	NVCC_JTAG	GPIO	ALT0	JTAG_TDO	Output	Keeper
JTAG_TMS	A2	—	NVCC_JTAG	GPIO	ALT0	JTAG_TMS	Input	PU (47k)
JTAG_TRSTB	K3	—	NVCC_JTAG	GPIO	ALT0	JTAG_TRST_B	Input	PU (47k)
KEY_COL0	AB6	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO06	Input	PU (100k)
KEY_COL1	Y7	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO08	Input	PU (100k)
KEY_COL2	AD7	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO10	Input	PU (100k)
KEY_COL3	AD6	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO12	Input	PU (100k)
KEY_COL4	AF1	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO14	Input	PU (100k)
KEY_ROW0	AB7	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO07	Input	PU (100k)
KEY_ROW1	AD3	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO09	Input	PU (100k)
KEY_ROW2	AF2	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO11	Input	PU (100k)
KEY_ROW3	AE3	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO13	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
KEY_ROW4	AC7	—	NVCC_GPIO	GPIO	ALT5	GPIO4_IO15	Input	PU (100k)
LVDS0_CLK_N	AH4	—	NVCC_LVDS_2P5	LVDS	—	LVDS0_CLK_N	—	—
LVDS0_CLK_P	AJ4	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_CLK_P	Input	Keeper
LVDS0_TX0_N	AG2	—	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX0_N	—	—
LVDS0_TX0_P	AG1	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX0_P	Input	Keeper
LVDS0_TX1_N	AH2	—	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX1_N	—	—
LVDS0_TX1_P	AH1	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX1_P	Input	Keeper
LVDS0_TX2_N	AH3	—	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX2_N	—	—
LVDS0_TX2_P	AJ3	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX2_P	Input	Keeper
LVDS0_TX3_N	AH5	—	NVCC_LVDS_2P5	LVDS	—	LVDS0_TX3_N	—	—
LVDS0_TX3_P	AJ5	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX3_P	Input	Keeper
LVDS1_CLK_N	AJ8	—	NVCC_LVDS_2P5	LVDS	—	LVDS1_CLK_N	—	—
LVDS1_CLK_P	AH8	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_CLK_P	Input	Keeper
LVDS1_TX0_N	AJ6	—	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX0_N	—	—
LVDS1_TX0_P	AH6	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX0_P	Input	Keeper
LVDS1_TX1_N	AH7	—	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX1_N	—	—
LVDS1_TX1_P	AJ7	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX1_P	Input	Keeper
LVDS1_TX2_N	AJ9	—	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AH9	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AJ10	—	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AH10	—	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX3_P	Input	Keeper
NANDF_ALE	A20	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	PU (100k)
NANDF_CLE	G17	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO07	Input	PU (100k)
NANDF_CS0	A21	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	PU (100k)
NANDF_CS1	F18	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	PU (100k)
NANDF_CS2	C20	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	PU (100k)
NANDF_CS3	B21	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	PU (100k)
NANDF_D0	F19	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	PU (100k)
NANDF_D1	B22	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	PU (100k)
NANDF_D2	B23	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	PU (100k)
NANDF_D3	A23	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	PU (100k)
NANDF_D4	G19	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	PU (100k)
NANDF_D5	A24	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	PU (100k)
NANDF_D6	C23	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	PU (100k)
NANDF_D7	F20	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO07	Input	PU (100k)
NANDF_RB0	B20	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	PU (100k)
NANDF_WP_B	C19	—	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	PU (100k)
ONOFF	A13	—	VDD_SNVS_IN	GPIO	—	SRC_ONOFF	Input	PU (100k)
PCIE_RXM	B3	—	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RXP	A3	—	PCIE_VPH	—	—	PCIE_RX_P	—	—

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
PCIE_TXM	A5	—	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B5	—	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	A12	—	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU(100k)
PMIC_STBY_REQ	C12	—	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	F13	—	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100k)
RGMII_RD0	G27	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	PU (100k)
RGMII_RD1	F29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	PU (100k)
RGMII_RD2	H23	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	PU (100k)
RGMII_RD3	G29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	PU (100k)
RGMII_RX_CTL	F28	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	PD (100k)
RGMII_RXC	H24	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	PD (100k)
RGMII_TD0	C28	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	PU (100k)
RGMII_TD1	E29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	PU (100k)
RGMII_TD2	G24	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	PU (100k)
RGMII_TD3	F27	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	PU (100k)
RGMII_TX_CTL	G28	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	PD (100k)
RGMII_TXC	C29	—	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	PD (100k)
RTC_XTALI	B10	—	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	A10	—	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SATA_RXM	A16	—	SATA_VPH	—	—	SATA_PHY_RX_N	—	—
SATA_RXP	B16	—	SATA_VPH	—	—	SATA_PHY_RX_P	—	—
SATA_TXM	A14	—	SATA_VPH	—	—	SATA_PHY_TX_N	—	—
SATA_TXP	B14	—	SATA_VPH	—	—	SATA_PHY_TX_P	—	—
SD1_CLK	C26	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	PU (100k)
SD1_CMD	D28	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	PU (100k)
SD1_DAT0	A27	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	PU (100k)
SD1_DAT1	B27	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	PU (100k)
SD1_DAT2	F22	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	PU (100k)
SD1_DAT3	A28	—	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	PU (100k)
SD2_CLK	E28	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	PU (100k)
SD2_CMD	D29	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	PU (100k)
SD2_DAT0	B29	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	PU (100k)
SD2_DAT1	F24	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	PU (100k)
SD2_DAT2	B28	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	PU (100k)
SD2_DAT3	F23	—	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	PU (100k)
SD3_CLK	C17	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	PU (100k)
SD3_CMD	F16	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	PU (100k)
SD3_DAT0	A18	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	PU (100k)
SD3_DAT1	B18	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	PU (100k)
SD3_DAT2	A19	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	PU (100k)

Table 85. 12 x 12 mm Functional Contact Assignments (continued)

Ball Name	PoP Bottom Ball	PoP Top Ball	Power Group	Ball Type	Out of Reset Condition[1]			
					Default Mode	Default Function	Input/ Output	Value[2]
SD3_DAT3	F17	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	PU (100k)
SD3_DAT4	F14	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	PU (100k)
SD3_DAT5	B17	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	PU (100k)
SD3_DAT6	B15	—	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	PU (100k)
SD3_DAT7	A17	—	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	PU (100k)
SD3_RST	B19	—	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	PU (100k)
SD4_CLK	A22	—	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	PU (100k)
SD4_CMD	C21	—	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	PU (100k)
SD4_DAT0	B24	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	PU (100k)
SD4_DAT1	A25	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	PU (100k)
SD4_DAT2	G20	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	PU (100k)
SD4_DAT3	A26	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	PU (100k)
SD4_DAT4	F21	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO12	Input	PU (100k)
SD4_DAT5	C24	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO13	Input	PU (100k)
SD4_DAT6	B26	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO14	Input	PU (100k)
SD4_DAT7	B25	—	NVCC_NANDF	GPIO	ALT5	GPIO2_IO15	Input	PU (100k)
TAMPER	B12	—	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	PD (100k)
TEST_MODE	B13	—	VDD_SNVS_IN	—	—	TCU_TEST_MODE	Input	PD (100k)
USB_H1_DN	B11	—	VDD_USB_CAP	—	—	USB_H1_DN	—	—
USB_H1_DP	A11	—	VDD_USB_CAP	—	—	USB_H1_DP	—	—
USB_OTG_CHD_B	F12	—	VDD_USB_CAP	—	—	USB_OTG_CHD_B	—	—
USB_OTG_DN	B9	—	VDD_USB_CAP	—	—	USB_OTG_DN	—	—
USB_OTG_DP	A9	—	VDD_USB_CAP	—	—	USB_OTG_DP	—	—
XTALI	A8	—	NVCC_PLL	—	—	XTALI	—	—
XTALO	B8	—	NVCC_PLL	—	—	XTALO	—	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 Variance of the pull-up and pull-down strengths are shown in the tables as follows:

- Table 21, “GPIO I/O DC Parameters,” on page 38.
- Table 24, “LVDS I/O DC Parameters,” on page 41.

3 ENET_REF_CLK is used as a clock source for MII and RGMII modes only. RMII mode uses either GPIO_16 or RGMII_TX_CTL as a clock source. For more information on these clocks, see the device Reference Manual and the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

6.2.4 Signals with Different Reset States

For most of the signals, the state during reset is same as the state after reset, given in Out of Reset Condition column of Table 85, “12 x 12 mm Functional Contact Assignments”. However, there are few signals for which the state during reset is different from the state after reset. These signals along with their state during reset are given in Table 86.

Table 86. Signals with Differing Before Reset and After Reset States

Ball Name	Before Reset State	
	Input/Output	Value
EIM_A16	Input	PD (100K)
EIM_A17	Input	PD (100K)
EIM_A18	Input	PD (100K)
EIM_A19	Input	PD (100K)
EIM_A20	Input	PD (100K)
EIM_A21	Input	PD (100K)
EIM_A22	Input	PD (100K)
EIM_A23	Input	PD (100K)
EIM_A24	Input	PD (100K)
EIM_A25	Input	PD (100K)
EIM_DA0	Input	PD (100K)
EIM_DA1	Input	PD (100K)
EIM_DA2	Input	PD (100K)
EIM_DA3	Input	PD (100K)
EIM_DA4	Input	PD (100K)
EIM_DA5	Input	PD (100K)
EIM_DA6	Input	PD (100K)
EIM_DA7	Input	PD (100K)
EIM_DA8	Input	PD (100K)
EIM_DA9	Input	PD (100K)
EIM_DA10	Input	PD (100K)
EIM_DA11	Input	PD (100K)
EIM_DA12	Input	PD (100K)
EIM_DA13	Input	PD (100K)
EIM_DA14	Input	PD (100K)
EIM_DA15	Input	PD (100K)
EIM_EB0	Input	PD (100K)
EIM_EB1	Input	PD (100K)
EIM_EB2	Input	PD (100K)
EIM_EB3	Input	PD (100K)
EIM_LBA	Input	PD (100K)
EIM_RW	Input	PD (100K)
EIM_WAIT	Input	PD (100K)
GPIO_17	Output	Drive state unknown (x)

Table 86. Signals with Differing Before Reset and After Reset States (continued)

Ball Name	Before Reset State	
	Input/Output	Value
GPIO_19	Output	Drive state unknown (x)
KEY_COL0	Output	Drive state unknown (x)

6.2.5 12 x 12 mm PoP, 0.4 mm Pitch Ball Maps

Table 87 shows the 12 x 12 mm, 0.4 mm pitch top ball map. Table 88 shows the 12 x 12 mm, 0.4 mm pitch bottom ball map.

NOTE

On the top of the package, the data and control signals associated with each byte have been swizzled relative to the ball map of the associated LPDDR2 memory. This does not affect the operation of the i.MX 6Dual/6Quad SoC with the LPDDR2 memory.

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	GND	POP_VDD2__1	DRAM_D2P1	DRAM_D4P1	GND	DRAM_D1P1	DRAM_D5P1	GND	DRAM_DQS0P1_B	GND	DRAM_D11P1	DRAM_D9P1	GND	POP_VDD1__2	POP_VDD2__2	DRAM_D13P1	DRAM_D8P1	DRAM_D12P1	DRAM_DQS1P1	DRAM_DM1P1	POP_VDDQ	DRAM_DQS2P1	DRAM_D17P1	DRAM_D23P1	DRAM_D19P1	DRAM_D18P1	GND	DNU
B	GND	POP_VDD1__1	DRAM_D0P1	POP_VDDQ	DRAM_D3P1	DRAM_D7P1	POP_VDDQ	DRAM_D6P1	POP_VDDQ	DRAM_DQS0P1	DRAM_DM0P1	DRAM_D14P1	POP_VDDQ	GND	DRAM_VREF	POP_VDD2__2	DRAM_D15P1	POP_VDDQ	DRAM_D10P1	DRAM_DQS1P1_B	GND	DRAM_DM2P1	DRAM_DQS2P1_B	GND	POP_VDDQ	DRAM_D22P1	DRAM_D20P1	POP_VDD1__3	GND
C	POP_VDD1__1	DRAM_D18P0																										POP_VDD1__3	POP_VDD2__3
D	DRAM_D23P0	POP_VDDQ																										DRAM_D21P1	POP_VDDQ

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

M	L	K	J	H	G	F	E
DRAM_D2P0	DRAM_DM2P0	DRAM_DQS2P0_B	GND	DRAM_D20P0	DRAM_D21P0	GND	DRAM_D19P0
GND	DRAM_D7P0	DRAM_DQS2P0	POP_VDDQ	DRAM_D16P0	POP_VDDQ	DRAM_D17P0	DRAM_D22P0
POP_VDDQ	DRAM_D27P1	DRAM_D24P1	POP_VDDQ	GND	DRAM_DQS3P1	DRAM_DM3P1	GND
DRAM_D28P1	GND	DRAM_D30P1	DRAM_D31P1	DRAM_D26P1	DRAM_DQS3P1_B	POP_VDDQ	DRAM_D16P1

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

Y	W	V	U	T	R	P	N
POP_VDDQ	DRAM_D5P0	DRAM_D4P0	POP_VDDQ	POP_VDD2__5	POP_VDD1__4	GND	DRAM_D1P0
DRAM_D3P0	DRAM_D6P0	GND	DRAM_D0P0	POP_VDD2__5	DRAM_VREF	GND	POP_VDD1__4
DRAM_CS0P0	DRAM_CA4P0	GND	DRAM_VREF	POP_VDDCA	GND	POP_VDD2__4	DRAM_D29P1
DRAM_CKE1P0	DRAM_CS1P0	DRAM_CA3P0	DRAM_CA2P0	DRAM_CA1P0	DRAM_CA0P0	POP_VDD1__5	DRAM_D25P1

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

AG	AF	AE	AD	AC	AB	AA
DRAM_D10P0	DRAM_D14P0	DRAM_D12P0	DRAM_DQS1P0_B	POP_VDDQ	DRAM_DM0P0	DRAM_DQS0P0
DRAM_D13P0	POP_VDDQ	GND	DRAM_DQS1P0	DRAM_DM1P0	GND	DRAM_DQS0P0_B
POP_VDD2__8	GND	DRAM_CA8P0	DRAM_CA7P0	POP_VDDCA	DRAM_CLKP0	GND
POP_ZQP0	DRAM_CA9P0	POP_VDDCA	DRAM_CA6P0	DRAM_CA5P0	DRAM_CLKP0_B	DRAM_CKE0P0

Table 87. PoP 12 x 12 mm, 0.4 mm Pitch Top Ball Map (continued)

AJ	AH
DNU	GND
GND	POP_VDD1__6
DRAM_D8P0	POP_VDD2__6
POP_VDDQ	DRAM_D9P0
DRAM_D15P0	GND
POP_VDDQ	DRAM_D11P0
GND	DRAM_DM3P0
DRAM_DQS3P0_B	DRAM_DQS3P0
DRAM_D25P0	POP_VDDQ
DRAM_D29P0	DRAM_D28P0
GND	DRAM_D24P0
DRAM_D27P0	POP_VDDQ
DRAM_D30P0	DRAM_D31P0
DRAM_D26P0	GND
POP_VDD1__7	POP_VDD2__7
GND	DRAM_VREF
POP_ZQP1	DRAM_CA9P1
DRAM_CA8P1	GND
POP_VDDCA	DRAM_CA7P1
DRAM_CA5P1	DRAM_CA6P1
DRAM_CLKP1	DRAM_CLKP1_B
GND	POP_VDDCA
DRAM_CKE1P1	DRAM_CKE0P1
DRAM_CS1P1	DRAM_CS0P1
DRAM_CA4P1	DRAM_CA3P1
POP_VDDCA	DRAM_CA2P1
DRAM_CA0P1	DRAM_CA1P1
GND	POP_VDD1__8
DNU	GND

Table 88. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map

E	D	C	B	A	
CSI_CLK0P	CSI_D1M	CSI_D0P	JTAG_TCK	NC	1
CSI_CLK0M	CSI_D1P	CSI_D0M	JTAG_TDO	JTAG_TMS	2
POP_VDDQ	GND	POP_VDD1__1	PCIE_RXM	PCIE_RXP	3
		POP_VDD2__1	GND	PCIE_REXT	4
		POP_VDDQ	PCIE_TXP	PCIE_TXM	5
		GND	CLK2_P	CLK2_N	6
		POP_VDDQ	CLK1_P	CLK1_N	7
		NVCC_PLL_OUT	XTALO	XTALI	8
		POP_VDDQ	USB_OTG_DN	USB_OTG_DP	9
		GPANAIO	RTC_XTALI	RTC_XTALO	10
		USB_H1_VBUS	USB_H1_DN	USB_H1_DP	11
		PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ	12
		POP_VDDQ	TEST_MODE	ONOFF	13
		BOOT_MODE0	SATA_TXP	SATA_TXM	14
		POP_VDD1__2	SD3_DAT6	GND	15
		POP_VDD2__2	SATA_RXP	SATA_RXM	16
		SD3_CLK	SD3_DAT5	SD3_DAT7	17
		POP_VDDQ	SD3_DAT1	SD3_DAT0	18
		NANDF_WP_B	SD3_RST	SD3_DAT2	19
		NANDF_CS2	NANDF_RB0	NANDF_ALE	20
		SD4_CMD	NANDF_CS3	NANDF_CS0	21
		POP_VDDQ	NANDF_D1	SD4_CLK	22
		NANDF_D6	NANDF_D2	NANDF_D3	23
		SD4_DAT5	SD4_DAT0	NANDF_D5	24
		POP_VDDQ	SD4_DAT7	SD4_DAT1	25
		SD1_CLK	SD4_DAT6	SD4_DAT3	26
POP_VDDQ	POP_VDD2__3	POP_VDD1__3	SD1_DAT1	SD1_DAT0	27
SD2_CLK	SD1_CMD	RGMII_TD0	SD2_DAT2	SD1_DAT3	28
RGMII_TD1	SD2_CMD	RGMII_TXC	SD2_DAT0	GND	29

Table 88. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

N	M	L	K	J	H	G	F
HDMI_D1M	HDMI_D0M	HDMI_CLKM	DSI_D1P	DSI_CLK0M	DSI_D0P	CSI_D3P	CSI_D2M
HDMI_D1P	HDMI_D0P	HDMI_CLKP	DSI_D1M	DSI_CLK0P	DSI_D0M	CSI_D3M	CSI_D2P
GND	GND	GND	JTAG_TRSTB	POP_VDDQ	GND	POP_VDDQ	JTAG_MOD
GND	GND	GND	DSI_REXT	VDD_FA	CSI_REXT	NVCC_JTAG	GND
HDMI_VPH	HDMI_VP	JTAG_TDI	NVCC_MIPI	FA_ANA	PCIE_VP	PCIE_VPH	GND
						PCIE_VPTX	VDDHIGH_IN
						VDD_SNVS_CAP	VDDHIGH_IN
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDDUSB_CAP	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			USB_OTG_VBUS	VDDHIGH_CAP
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN			VDD_SNVS_IN	USB_OTG_CHD_B
GND	GND	GND	GND			BOOT_MODE1	POR_B
GND	GND	GND	GND			SATA_VPH	SD3_DAT4
GND	GND	GND	GND			SATA_VP	SATA_REXT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_SD3	SD3_CMD
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NANDF_CLE	SD3_DAT3
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN			NVCC_NANDF	NANDF_CS1
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			NANDF_D4	NANDF_D0
VDDPU_CAP	VDDSOC_IN	VDDSOC_IN	VDDSOC_CAP			SD4_DAT2	NANDF_D7
						NVCC_SD1	SD4_DAT4
						NVCC_SD2	SD1_DAT2
EIM_EB0	NVCC_EIM1	EIM_D31	NVCC_EIM0	EIM_D20	RGMII_RD2	NVCC_RGMII	SD2_DAT3
EIM_A17	EIM_A18	EIM_D29	EIM_D23	EIM_D16	RGMII_RXC	RGMII_TD2	SD2_DAT1
EIM_A24	POP_VDDQ	EIM_D26	EIM_EB3	POP_VDDQ	EIM_EB2	RGMII_RD0	RGMII_TD3
EIM_A23	EIM_D27	EIM_D25	EIM_D22	EIM_D18	EIM_A25	RGMII_TX_CTL	RGMII_RX_CTL
EIM_D30	EIM_D28	EIM_D24	EIM_D21	EIM_D19	EIM_D17	RGMII_RD3	RGMII_RD1

Table 88. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

AA	Y	W	V	U	T	R	P
CSI0_VSYNC	CSI0_DAT6	CSI0_DAT9	CSI0_DAT11	CSI0_DAT17	CSI0_DAT18	HDMI_HPD	HDMI_D2M
CSI0_MCLK	CSI0_DAT7	CSI0_DAT8	CSI0_DAT15	CSI0_DAT14	CSI0_DAT16	HDMI_DDCCEC	HDMI_D2P
GPIO_18	POP_VDDQ	CSI0_DAT10	CSI0_DAT12	POP_VDDQ	POP_VDD2__5	CSI0_DAT19	POP_VDD1__4
GPIO_1	GPIO_4	GPIO_2	CSI0_DATA_EN	CSI0_DAT4	CSI0_DAT13	VDDSOC_CAP	HDMI_REF
NVCC_LVDS2P5	KEY_COL1	NVCC_GPIO	GPIO_8	CSI0_DAT5	NVCC_CSI	VDDSOC_CAP	VDD_CACHE_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	GND	GND	GND	GND	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
	GND	GND	GND	GND	GND	GND	GND
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	VDDSOC_CAP	VDDSOC_CAP	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	GND	GND	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	GND	GND	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
	VDDSOC_IN	VDDSOC_IN	VDDPU_CAP	VDDPU_CAP	GND	GND	VDDPU_CAP
	VDDSOC_IN	VDDSOC_IN	VDDPU_CAP	VDDPU_CAP	GND	GND	VDDPU_CAP
NVCC_DRAM	NVCC_DRAM	NVCC_ENET	DISP0_DAT3	DISP0_DAT6	NVCC_LCD	EIM_DA13	NVCC_EIM2
DISP0_DAT19	DISP0_DAT22	DI0_PIN3	DISP0_DAT4	DI0_PIN4	EIM_DA6	EIM_DA7	EIM_EB1
EIM_BCLK	EIM_DA12	EIM_DA4	EIM_DA1	EIM_RW	POP_VDDCA	POP_VDD1__5	POP_VDD2__4
EIM_DA15	EIM_DA10	EIM_DA5	EIM_DA0	EIM_CS1	EIM_OE	EIM_A19	EIM_A22
DRAM_CKE0P0	DRAM_CKE1P0	EIM_DA2	EIM_LBA	EIM_CS0	EIM_A16	EIM_A20	EIM_A21

Table 88. PoP 12 x 12 mm, 0.4 mm Pitch Bottom Ball Map (continued)

AJ	AH	AG	AF	AE	AD	AC	AB
GND	LVDS0_TX1_P	LVDS0_TX0_P	KEY_COL4	GPIO_3	CSI0_PIXCLK	GPIO_7	GPIO_19
GND	LVDS0_TX1_N	LVDS0_TX0_N	KEY_ROW2	GPIO_0	GPIO_9	GPIO_17	GPIO_16
LVDS0_TX2_P	LVDS0_TX2_N	POP_VDD1__6	POP_VDDQ	KEY_ROW3	KEY_ROW1	POP_VDDQ	GPIO_5
LVDS0_CLK_P	LVDS0_CLK_N	POP_VDD2__6					
LVDS0_TX3_P	LVDS0_TX3_N	GND					
LVDS1_TX0_N	LVDS1_TX0_P	POP_VDDQ			KEY_COL3	GPIO_6	KEY_COL0
LVDS1_TX1_P	LVDS1_TX1_N	GND			KEY_COL2	KEY_ROW4	KEY_ROW0
LVDS1_CLK_N	LVDS1_CLK_P	GND			NVCC_DRAM	NVCC_DRAM	
LVDS1_TX2_N	LVDS1_TX2_P	POP_VDDQ			NVCC_DRAM	NVCC_DRAM	
LVDS1_TX3_N	LVDS1_TX3_P	DRAM_VREF			NVCC_DRAM	NVCC_DRAM	
GND	GND	GND			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDDQ			NVCC_DRAM	NVCC_DRAM	
GND	GND	GND			NVCC_DRAM	NVCC_DRAM	
GND	GND	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDD2__7			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_VDD1__7			NVCC_DRAM	NVCC_DRAM	
GND	GND	POP_ZQP1			NVCC_DRAM	NVCC_DRAM	
GND	GND	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
ZQPAD	GND	POP_VDDCA			NVCC_DRAM	NVCC_DRAM	
GND	ENET_RXD1	NVCC_LVDS2P5			NVCC_DRAM	NVCC_DRAM	
ENET_MDC	ENET_REF_CLK	ENET_TXD1			NVCC_DRAM	NVCC_DRAM	
ENET_MDIO	ENET_RXD0	POP_VDDCA			ENET_RX_ER	NVCC_DRAM	
DRAM_CKE1P1	DRAM_CKE0P1	ENET_CRS_DV			ENET_TXD0	NVCC_DRAM	NVCC_DRAM
DISP0_DAT23	DISP0_DAT18	ENET_TX_EN			DISP0_DAT20	DISP0_DAT21	DISP0_DAT16
DISP0_DAT13	DISP0_DAT15	POP_VDDCA					
DISP0_DAT8	DISP0_DAT10	POP_VDD1__8					
DISP0_DAT11	DISP0_DAT5	POP_VDD2__8	POP_ZQP0	POP_VDDCA	DISP0_DAT1	POP_VDDCA	DISP0_DAT2
DISP0_DAT14	DISP0_DAT17	DISP0_DAT9	DISP0_DAT12	DISP0_DAT7	DI0_PIN15	EIM_DA14	EIM_DA8
GND	DISP0_DAT0	EIM_WAIT	DI0_DISP_CLK	EIM_DA11	DI0_PIN2	EIM_DA9	EIM_DA3

7 Revision History

Table 89 provides a revision history for the i.MX 6Dual Pop and i.MX 6Quad Pop data sheet.

Table 89. Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 2	10/2018	Rev. 2 changes include the following: • Table 20, “XTALI and RTC_XTALI DC Parameters,” on page 38, – Row: XTALI input leakage current at startup, $I_{XTALI\_STARTUP}$: Changed from “... driven 32KHz RTC clock @ 1.1V” to “...driven 24 MHz clock at 1.1V.” • Table 45, “eMMC4.4/4.41 Interface Timing Specification,” on page 77, – Row: SD2, uSDHC Output Delay: Changed t_{OD} *from* 2.5 ns minimum *to* 2.8 ns and 7.1 ns maximum *to* 6.8 ns.
1	09/2017	Rev. 1 changes include the following: • Changed throughout: – Changed terminology from “floating” to “not connected”. • Section 1, “Introduction” on page 1: Changed ARM Cortex-A9 operating speed from “up to 1 GHz” to “up to 800 MHz.” • Figure 1, "Part Number Nomenclature—i.MX 6Dual PoP and 6Quad PoP," on page 4: – Removed from Temperature block: Automotive temperature row. • Table 2, “i.MX 6Dual/6Quad Modules List,” on page 10: – Added bullet to uSDHC row: “Conforms to the SD Host Controller Standard Specification v3.0” • Table 4, “Absolute Maximum Ratings,” on page 20: Extensive changes: – Separated rows Core supply voltage by LDO enable/bypass — Maximum LDO enabled value change from 1.5 to 1.6 V — Maximum LDO bypass value added, 1.4 V – Renamed Internal supply voltages to Core supply output voltage (LDO enabled) and changed maximum value from 1.3 to 1.4V. Added symbol NVCC_PLL_OUT. – Reordered VDD_HIGH_IN row and changed maximum value from 3.6 to 3.7V. – DDR I/O supply voltage row changes: — Changed Symbols from “Supplies denoted as I/O supply” to: “NVCC_DRAM” — Added footnote to maximum value regarding “The absolute maximum voltage includes an allowance for 400 mV …”. – Change row GPIO I/O supply voltage: — Changed Symbols from “Supplies denoted as I/O supply” to: multiple values — Maximum value change from 3.6 to 3.7 V – Added rows: HDMI, PCIe, and SATA PHY high (VPH) and low (VP) supply voltage and values – Change row “LVDS I/O supply voltage” to “LVDS and MIPI I/O supply voltage (2.5V supply)” — Changed Symbols from “Supplies denoted as I/O supply” to: multiple values — Maximum value change from 2.8 to 2.85 V – Added row: PCI PHY supply voltage and values – Added row: RGMII I/O supply voltage and values – Added row: SNVS IN supply voltage and values – Added row: USB_OTG_CHD_B and values – Changed row: “Input voltage on USB_OTG_DP…” to “USB I/O supply voltage” — Changed Symbols from “USB_DP/USB_DN” to: multiple values — Maximum value change from 3.63 to 3.73 V – Separated row: “Input/output voltage range” by non-DDR/DDR pins, and added Vin/Vout to row name — Maximum value added for Vin/Vout DDR pins: OVDD + 0.4 V and added footnote – Separated and renamed row: “ESD damage immunity” by HBM/CDM and changed Symbol names — Maximum value added for Vin/Vout DDR pins: OVDD + 0.4 V and added footnote *(Revision History table continues on next page.)*

Table 89. Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1 (*Cont.*)	09/2017	• Section 4.1.2, “Thermal Resistance” on page 21: Added NOTE: “Per JEDEC JESD51-2, the intent of thermal resistance measurements…”. • Table 6, “Operating Ranges,” on page 22: – Changed row: “Junction Temperature Standard Commercial” to “Junction Temperature Industrial” – Changed row: Junction Temperature Industrial, maximum value from 95°C to 105°C • Section 4.1.5, “Maximum Measured Supply Currents” on page 25: Added section. • Section 4.2.1, “Power-Up Sequence” on page 32: – Removed content about calculating the proper current limiting resistor for a coin cell. – Removed inference to internal POR. • Section 4.5.2, “OSC32K” on page 36: Removed content about calculating the proper current limiting resistor for a coin cell. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” on page 38: Added “NOTE: The Vil and Vih specifications only apply when an external clock source is used…”. • Table 20, “XTALI and RTC_XTALI DC Parameters,” on page 38: – Added footnote to RTC_XTALI high level DC input voltage row: “This voltage specification must not be exceeded and …”. • Section 4.6.4, “RGMII I/O 2.5V I/O DC Electrical Parameters” on page 39: Added section and table. • Section 4.10, “Multi-Mode DDR Controller (MMDC)” on page 60: Replaced section with new content. Was 4.9.4 *DDR SDRAM Specific Parameters (LPDDR2)*” with timing diagrams and parameter tables for LPDDR2. • Section 4.12.4.3, “SDR50/SDR104 AC Timing” on page 78: Adjusted dimension SD5 in Figure 39. • Table 46, “SDR50/SDR104 Interface Timing Specification,” on page 78: Changes to Min/Max values: – SD2 min from: 0.3 x tCLK; to: 0.46 x tCLK – SD2 max from: 0.7 x tCLK to: 0.54 x tCLK – SD3 min from: 0.3 x tCLK; to: 0.46 x tCLK. Also corrected ID from duplicate SD2 to SD3. – SD3 max from: 0.7 x tCLK; to: 0.54 x tCLK – SD5 max from: 1 ns; to: 0.74 ns • Table 56, “Camera Input Signal Cross Reference, Format, and Bits Per Cycle,” on page 91: Changed RGB565, 16 bits column heading from 2 cycles to 1 cycle. • Table 84, “12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments,” on page 136: – Added description to ZQPAD. – Added description to GPANAIO row: “…output for NXP use only…”
0	3/2015	• Initial Release

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