2.25MHz 1A Synchronous Step-Down Converter

General Description

The RT8057 is a high efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter, capable of delivering 1A output current over a wide input voltage range from 2.7V to 5.5V. The RT8057 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as cellular phones, PDAs, hand-held devices, game console and related accessories.

The internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical applications. The RT8057 enters Low Dropout Mode when normal Pulse -Width Mode cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8057 enters shut-down mode and consumes less than 1μA when the EN pin is pulled low. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operating frequency of 2.25MHz.

The RT8057 is available in a small WDFN-6SL 2x2 package.

Ordering Information

RT8057□□(2)

- Taping Type (Pin1 at Q2)
- Package Type
  QW : WDFN-6SL 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

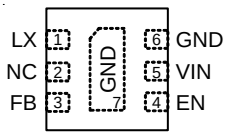
- **2.7V to 5.5V Wide Input Operation Range**
- **2.25MHz Fixed-Frequency PWM Operation**
- **Up to 1A Output Current**
- **Up to 90% Efficiency**
- **0.6V Reference Allows Low Output Voltage**
- **Internal Soft-Start**
- **No Schottky Diode Required**
- **Internal Compensation to Reduce External Components**
- **Low Dropout Operation : 100% Duty Cycle**
- **RoHS Compliant and Halogen Free**

Applications

- Portable Instruments
- Game Console and Accessories
- Microprocessors and DSP Core Supplies
- Cellular Phones
- Wireless and DSL Modems
- PC Cards

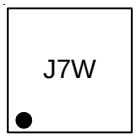
Pin Configurations

(TOP VIEW)



WDFN-6SL 2x2

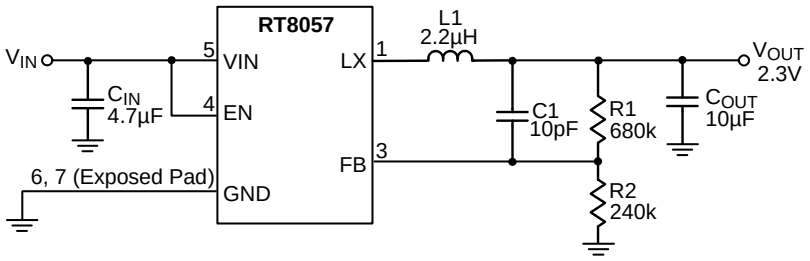
Marking Information



J7 : Product Code

W : Date Code

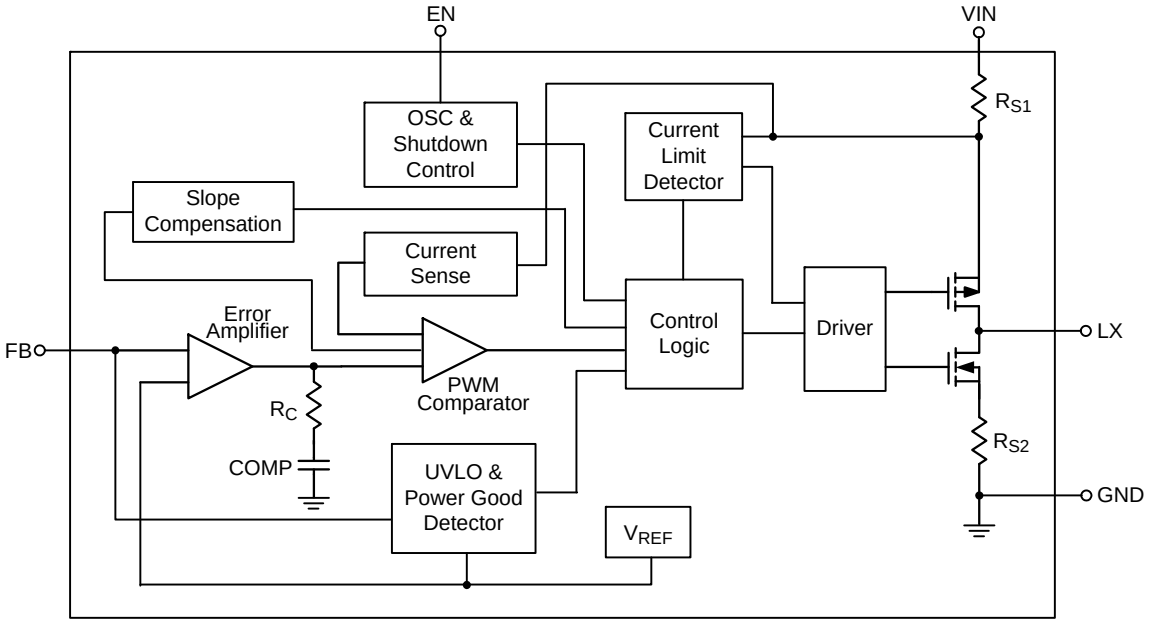
Typical Application Circuit



Function Pin Description

Pin No.	Pin Name	Pin Function
1	LX	Switch Node. Connect to the external inductor.
2	NC	No Internal Connection. Connect to GND.
3	FB	Feedback Pin. Connect to the external resistor divider.
4	EN	Chip Enable (Active High).
5	VIN	Power Input. Connect to the input capacitor.
6, 7 (Exposed Pad)	GND	Power GND. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6SL 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  WDFN-6SL 2x2, θ_{JA} ---------- 165°C/W
  WDFN-6SL 2x2, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM ---------- 2kV
  MM ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Current		I_{OUT}	V_{IN} = 2.7V to 5.5V	--	--	1	A
Quiescent Current		I_Q	I_{OUT} = 0mA	--	81	--	μA
Reference Voltage (0.6V)		V_{REF}		–2	--	2	%
			Note 5	–2.5	--	2.5	
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	2	2.2	2.4	V
			Hysteresis	--	0.2	--	V
Shutdown Current		I_{SHDN}		--	0.1	1	μA
Switching Frequency				--	2.25	--	MHz
EN Threshold Voltage	Logic-High	V_{IH}		1	--	V_{IN}	V
	Logic-Low	V_{IL}		--	--	0.4	V
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C
Switch On Resistance	High Side	$R_{DS(ON)\_H}$	I_{SW} = 0.2A	--	250	--	mΩ
	Low Side	$R_{DS(ON)\_L}$	I_{SW} = 0.2A	--	200	--	mΩ
Peak Current Limit		I_{LIM}		1.1	1.5	2	A
Output Voltage Line Regulation			V_{IN} = 2.7V to 5.5V	--	--	1	%/V
Output Voltage Load Regulation			0mA < I_{OUT} < 0.6A	--	--	1	%
Start-Up Time		t_{SS}	Guaranteed by Design	200	300	400	μs

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a low-effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

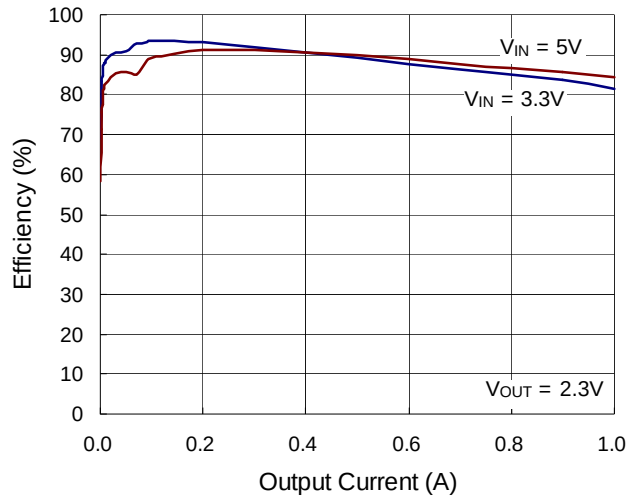
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

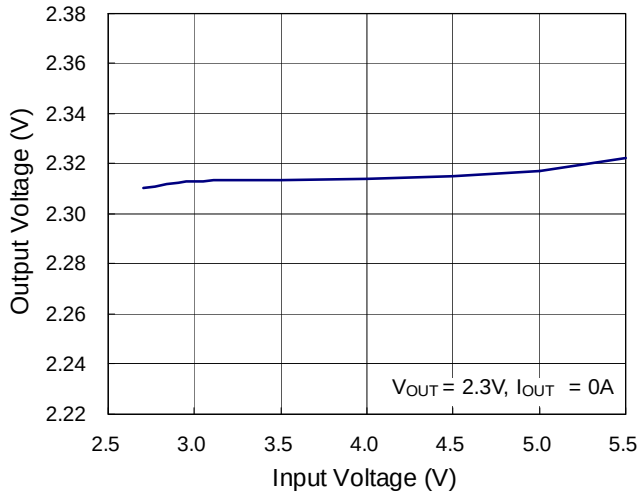
Note 5. The reference voltage accuracy is ±2.5% at recommended ambient temperature range, guaranteed by design.

Typical Operating Characteristics

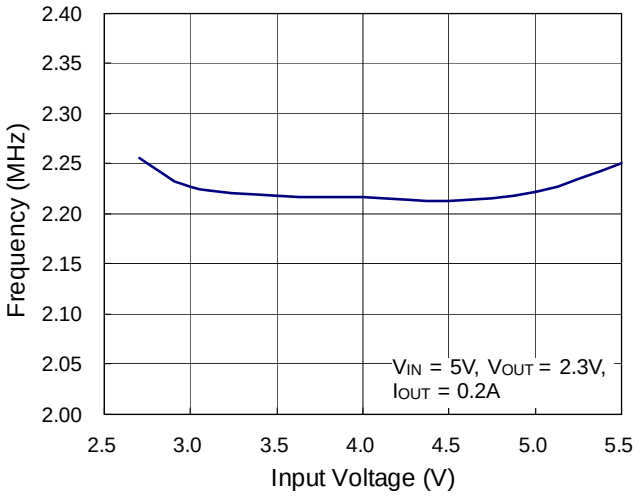
Efficiency vs. Output Current



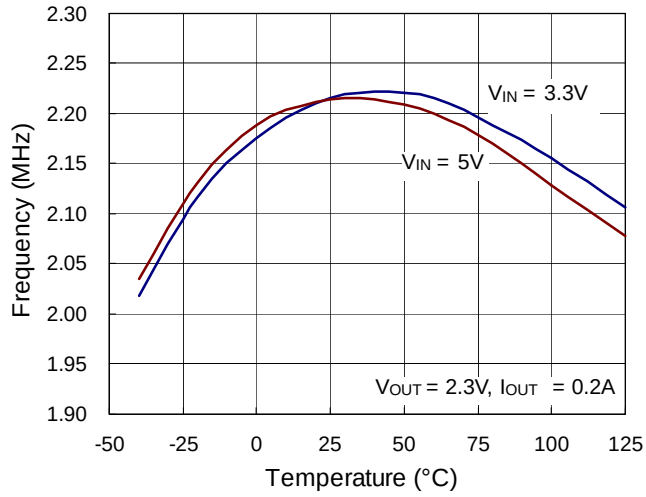
Output Voltage vs. Input Voltage



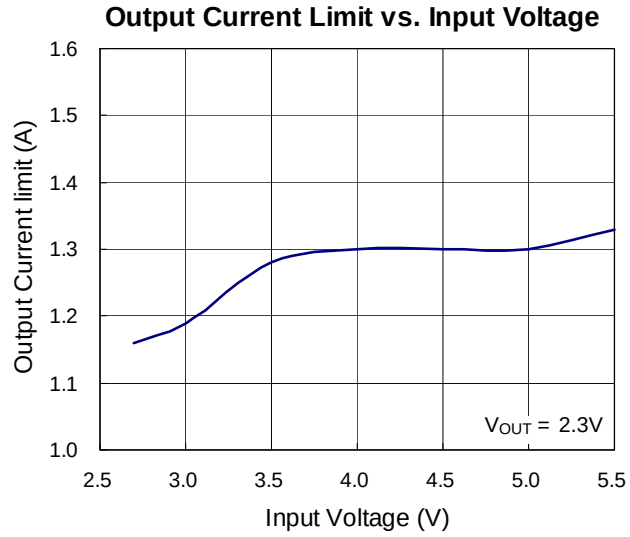
Frequency vs. Input Voltage



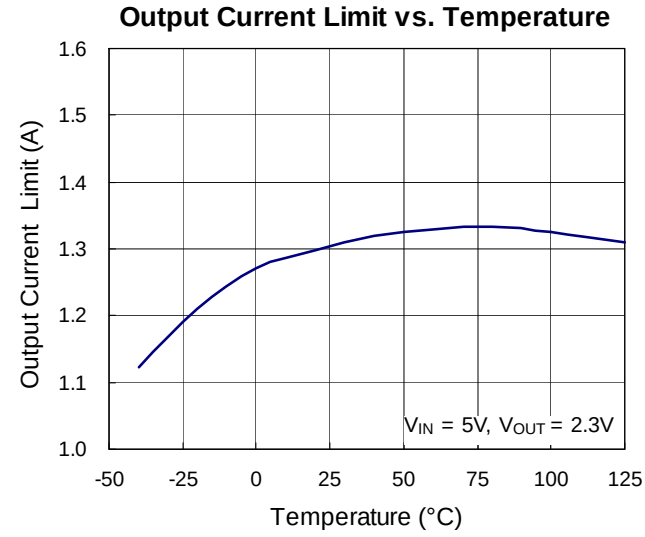
Frequency vs. Temperature



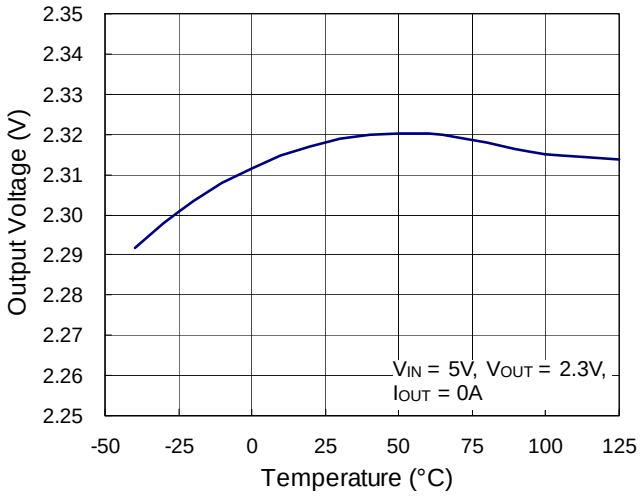
Output Current Limit vs. Input Voltage



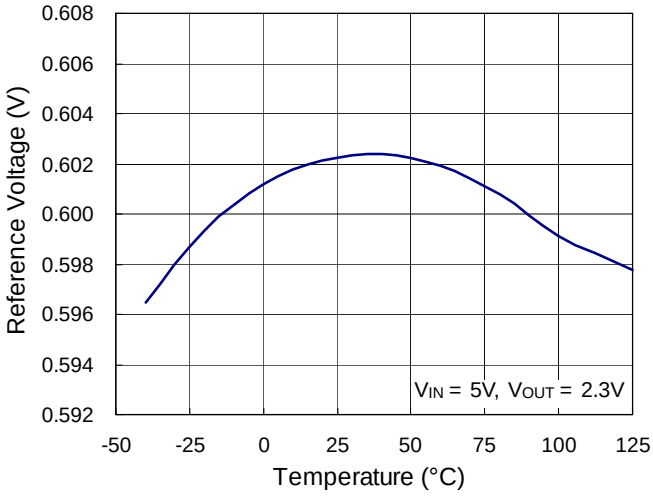
Output Current Limit vs. Temperature



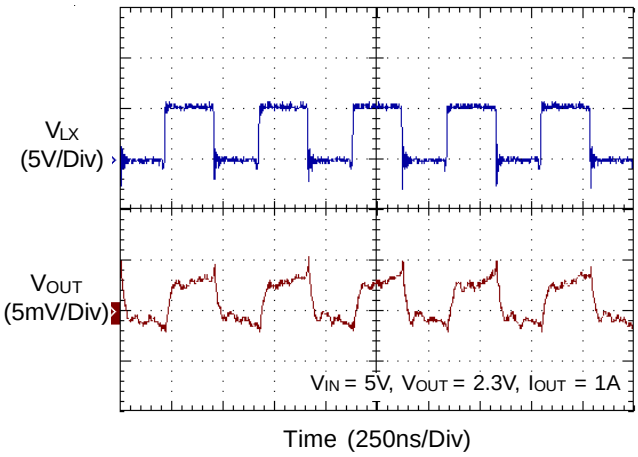
Output Voltage vs. Temperature



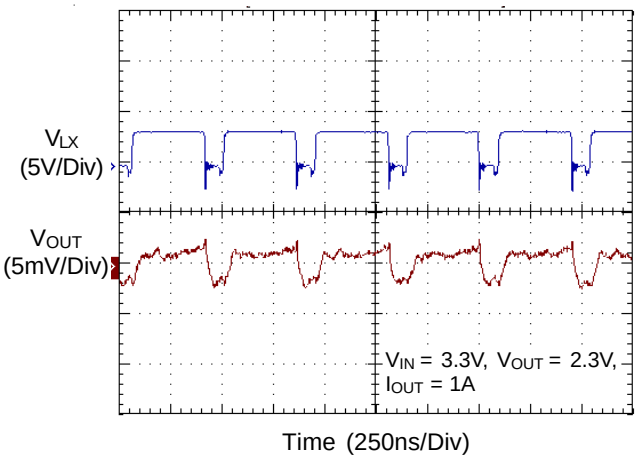
Reference Voltage vs. Temperature



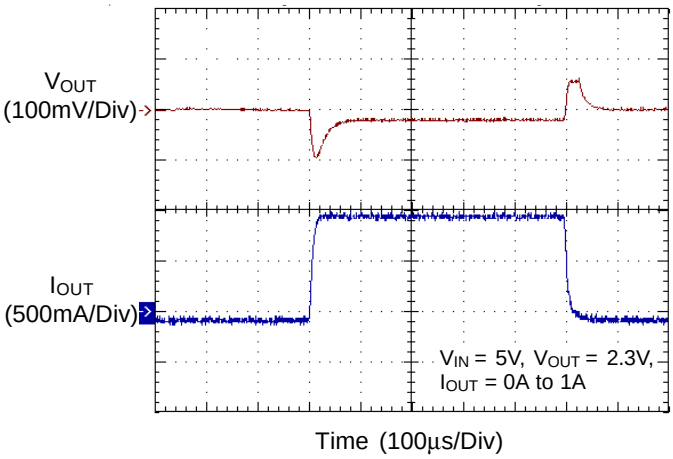
Output Ripple



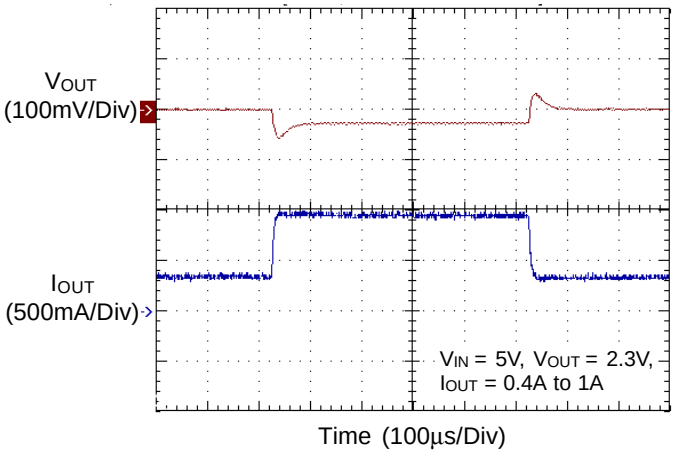
Output Ripple



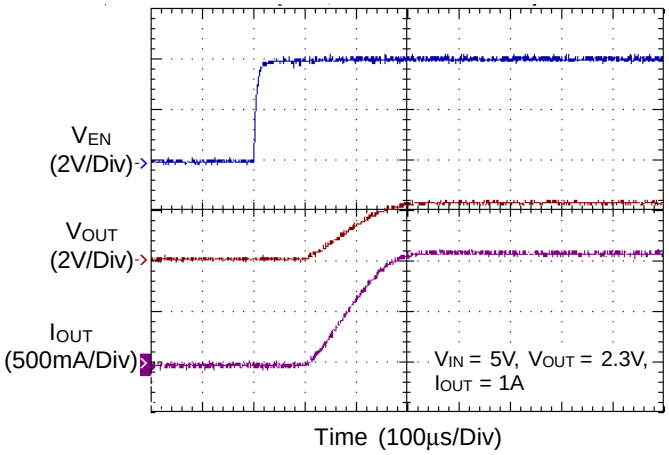
Load Transient Response



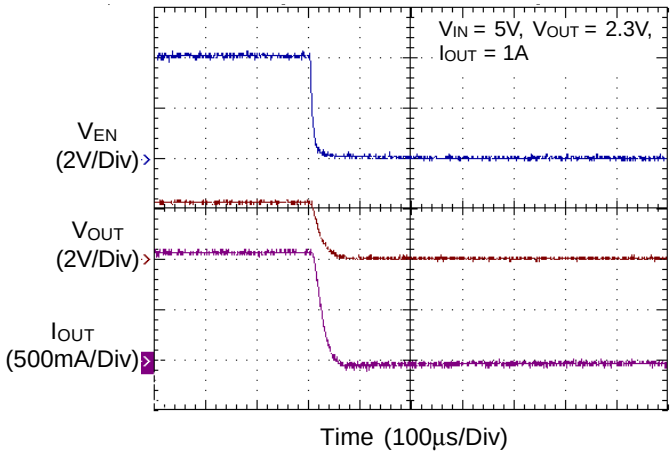
Load Transient Response



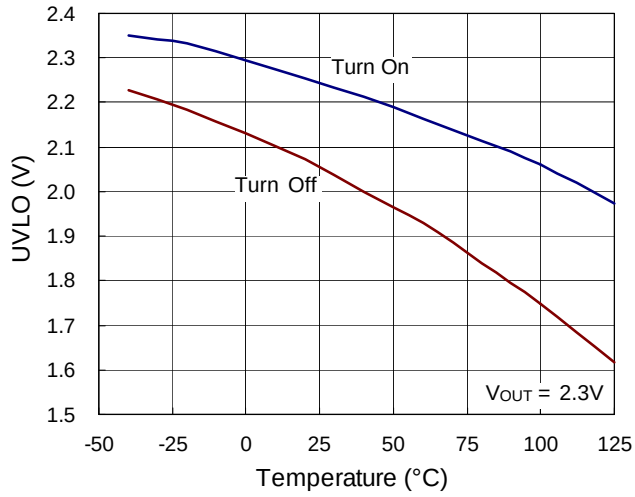
Power On from EN



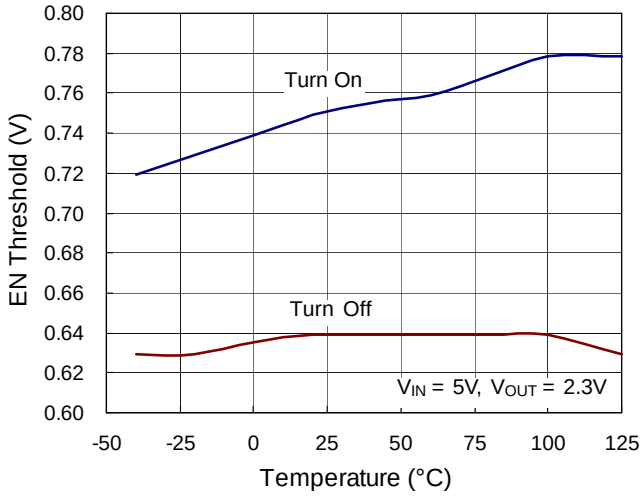
Power Off from EN



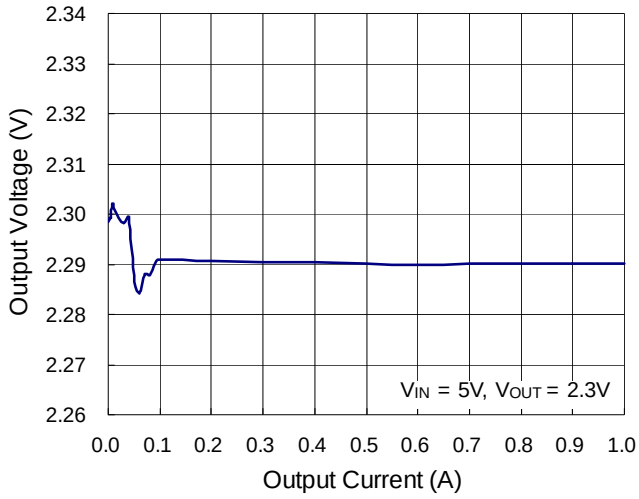
UVLO vs. Temperature



En Threshold vs. Temperature



Output Voltage vs. Output Current



Application Information

The basic RT8057 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times (1+\frac{R1}{R2})$$

where VREF equals to 0.6V typical. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

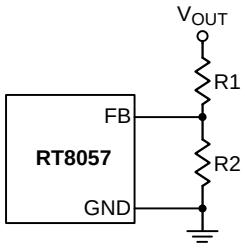


Figure 1. Setting the Output Voltage

Soft-Start

The RT8057 contains an internal soft-start clamp that gradually raises the clamp on the FB pin.

100% Duty Cycle Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle.

The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-MOSFET and the inductor.

Low Supply Operation

The RT8057 is designed to operate down to an input supply voltage of 2.7V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-Channel and N-Channel power switches increases. The user should calculate the power dissipation when the RT8057 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 33% of its set voltage threshold after OCP occurs, the under voltage protection circuit will be triggered to auto re-soft-start.

Input Voltage Over Voltage protection (V_{IN} OVP)

When the input voltage (V_{IN}) is higher than 6V, V_{IN} OVP will be triggered and the IC stops switching. Once the input voltage drops below 6V, the IC will return to normal operation.

Output Over Voltage Protection (V_{OUT} OVP)

When the output voltage exceeds more than 5% of the nominal reference voltage, the feedback loop forces the internal switches off within 50µs. Therefore, the output over voltage protection is automatically triggered by the loop.

Short Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. A current runaway detector is used to monitor inductor current. As current increases beyond the control of current loop, switching cycles will be skipped to prevent current runaway from occurring.

Table 1. Inductors

Component Supplier	Series	Inductance (µH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR4018 T2R2M	2.2µH	60	2700	4 X 4 X 1.8

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not result in much difference. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR, but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects.

The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Table 2. Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
MuRata	GRM31CR71A475KA01	4.7μF	1206
MuRata	GRM31CR71A106KA01	10μF	1206

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8057, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-6SL 2x2 packages, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (165°C/W) = 0.606W for WDFN-6SL 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8057 package, the derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

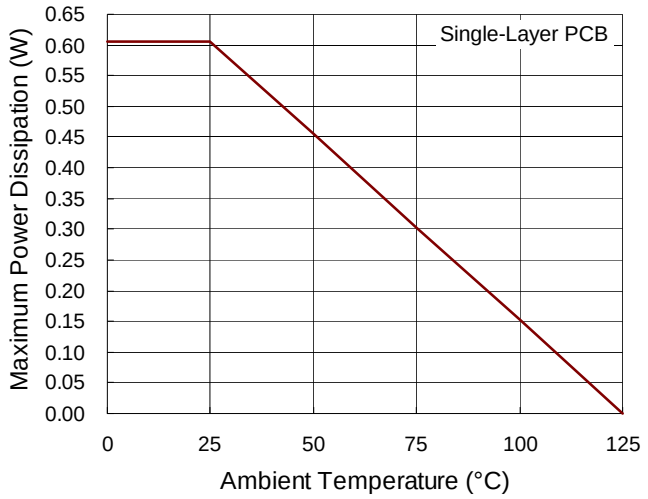


Figure 2. Derating Curve for the RT8057 Package

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8057.

- Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the VIN pin. This capacitor provides the AC current into the internal power MOSFETs.
- LX node experiences high frequency voltage swing and should be kept within a small area. Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick up.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND, or any other DC rail in the system).
- Connect the FB pin directly to the feedback resistors. The resistive voltage divider must be connected between V_{OUT} and GND.

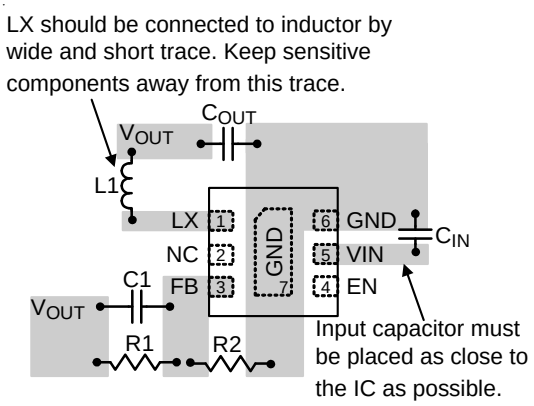
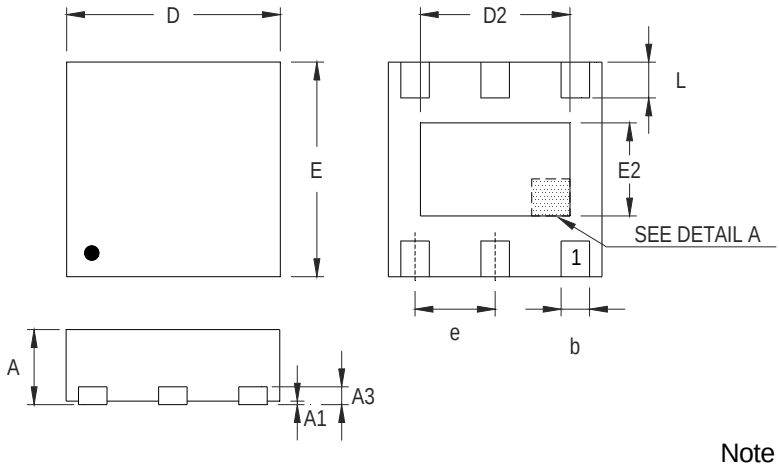
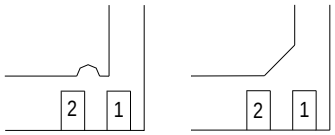


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.900	2.100	0.075	0.083
D2	1.550	1.650	0.061	0.065
E	1.900	2.100	0.075	0.083
E2	0.950	1.050	0.037	0.041
e	0.650		0.026	
L	0.200	0.300	0.008	0.012

W-Type 6SL DFN 2x2 Package

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