

PCN Number:	20160107000	PCN Date:	1/12/2016
Title:	Datasheet for LMK0482x		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification etc.

The product datasheet(s) is being updated as summarized below.

The following change history provides further details.



LMK04821, LMK04826, LMK04828

SNAS605AR – MARCH 2013 – REVISED DECEMBER 2015

Changes from Revision AQ (August 2014) to Revision AR

Page

• Added Support for 105°C thermal pad temperature	1
• Changed from I/O to I for pin 6 in <i>Pin Functions</i> table	7
• Deleted <i>programmable status pin</i> in Description column for pin 6 in <i>Pin Functions</i> table	7
• Changed from <i>No connection</i> to <i>Do not connect</i> for pins 7, 8, 9 in <i>Pin Functions</i> table	7
• Changed to <i>Reference Clock Input Port 1 for PLL 1</i> for Pins 34, 35 in <i>Pin Functions</i>	8
• Added <i>Reference Clock Input Port 2 for PLL1</i> for pins 40, 41 in <i>Pin Functions</i>	8
• Added ESD Ratings	9
• Added PCB temperature in <i>Recommended Operating Conditions</i>	9
• Added <i>Digital Input Timing</i> in <i>Electrical Characteristics</i>	22
• Changed Detailed block diagrams for LMK04821 and LMK04826/8	32
• Added 6 to DCLKout0 sequence and 7 to SDCLKout1 sequence in Figure 12	34
• Added 6 to DCLKout0 sequence and 7 to SDCLKout1 sequence in Figure 13	35
• Added <i>For each SDCLKoutY being used</i> in SYNC/SYSREF	36
• Deleted "SDCLKoutY_PD as required per output. " in Table 1	36
• Added footnote starting <i>SDCLKoutY_PD = 0</i> as... in Table 1	36
• Added <i>SDCLKout1_PD = 0, SDCLKout3_PD = 0</i> in Setup of SYSREF Example	37
• Changed DLD_HOLD_CNT to HOLDOVER_DLD_CNT in <i>Holdover Mode - Automatic Exit of Holdover</i>	45
• Changed <i>Recommended Programming Sequence</i>	49
• Added 0x171/0x172 to Register Map	53
• Added LMK04821 register setting	55
• Revised Register 0x143 table.....	67
• Added fixed register setting for 0x171	68
• Added fixed register setting for 0x172	68
• Added LMK04821 register setting	91
• Added LMK04821 register setting	92
• Changed RB_PLL1_LD description	92
• Changed RB_PLL2_LD description	92

Device Family	Change From:	Change To:	
LMK0482x	SNAS605AQ	SNAS605AR	
<p>These changes may be reviewed at the datasheet links provided. http://www.ti.com/product/LMK04828</p>			
Reason for Change:			
To more accurately reflect device characteristics.			
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):			
No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.			
Changes to product identification resulting from this PCN:			
None.			
Product Affected:			
LMK04821NKDR	LMK04826BISQ/NOPB	LMK04826BISQX/NOPB	LMK04828BISQE/NOPB
LMK04821NKDT	LMK04826BISQE/NOPB	LMK04828BISQ/NOPB	LMK04828BISQX/NOPB

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com