

HiperFET™
Power MOSFETs
Q-Class

IXFA4N100Q
IXFP4N100Q

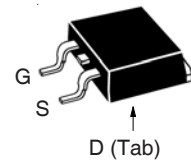
$V_{DSS} = 1000V$
 $I_{D25} = 4A$
 $R_{DS(on)} \leq 3.0\Omega$

N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Diode

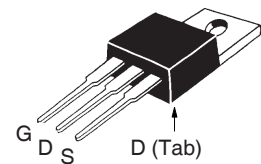


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	1000	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	1000	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ C$	4	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	16	A
I_A	$T_C = 25^\circ C$	4	A
E_{AS}	$T_C = 25^\circ C$	700	mJ
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	5	V/ns
P_D	$T_C = 25^\circ C$	150	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
M_C	Mounting Force (TO-263)	10..65/2.2..14.6	Nm/lb.in.
M_d	Mounting Torque (TO-220)	1.13/10	Nm/lb.in.
Weight	TO-263	2.5	g
	TO-220	3.0	g

TO-263 AA (IXFA)



TO-220AB (IXFP)



G = Gate D = Drain
 S = Source Tab = Drain

Features

- International Standard Packages
- Avalanche Rated
- Fast Intrinsic Diode
- Low Q_G
- Low $R_{DS(on)}$
- Low Drain-to-Tab Capacitance
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- DC Choppers
- Temperature and Lighting Controls

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 1mA$	1000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1.5mA$	2.5		4.5 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			50 μA 1 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			3.0 Ω

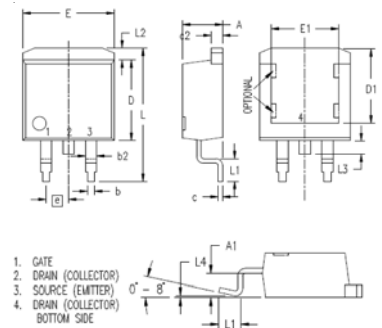
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = 0.5 \cdot I_{D25}$, Note 1	1.5	2.5	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		1050	pF
C_{oss}			120	pF
C_{rss}			30	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 4.7\Omega$ (External)		17	ns
t_r			15	ns
$t_{d(off)}$			32	ns
t_f			18	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		39	nC
Q_{gs}			9	nC
Q_{gd}			23	nC
R_{thJC}				0.80°C/W
R_{thCS}	TO-220	0.50		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			4 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			16 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = I_S, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			250 ns
Q_{RM}			0.52	μC
I_{RM}			1.80	A

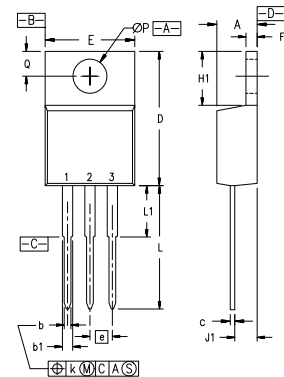
Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

TO-263 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

TO-220 Outline



Pins: 1 - Gate 2 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Figure 1. Output Characteristics at 25°C

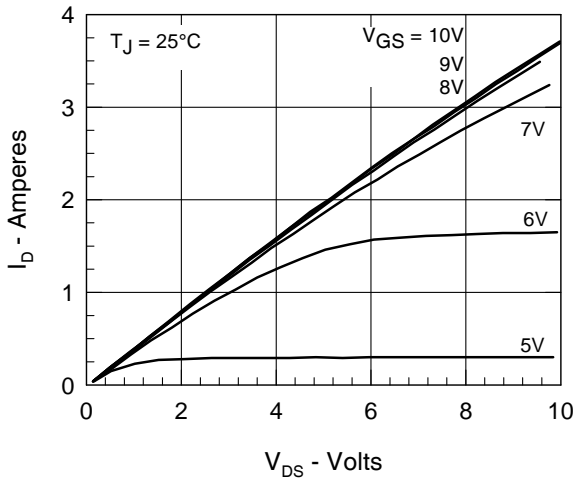


Figure 2. Extended Output Characteristics at 125°C

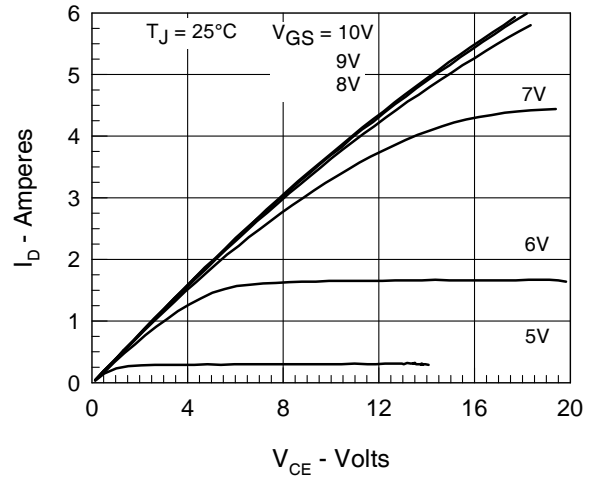


Figure 3. Output characteristics at 125°C

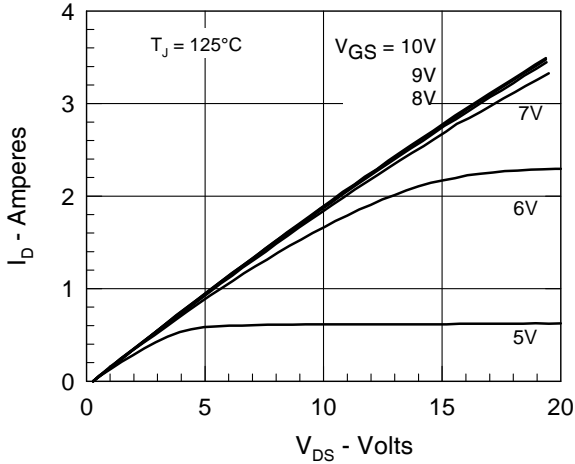


Figure 4. Admittance Curves

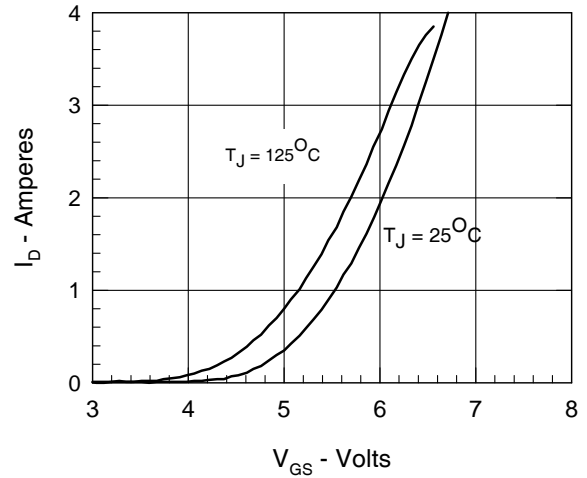


Figure 5. $R_{DS(on)}$ normalized to 0.5 I_{D25} value vs. I_D

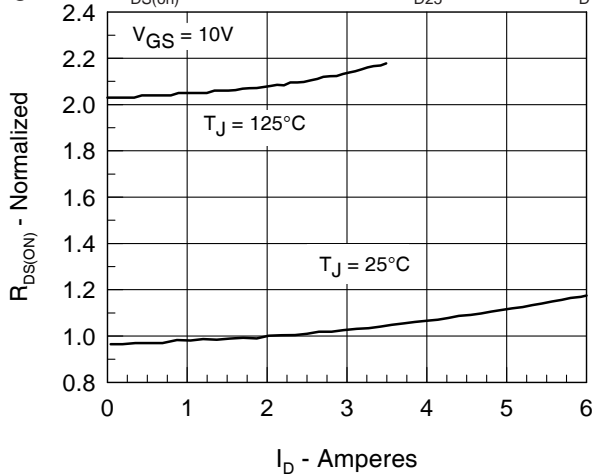


Figure 6. $R_{DS(on)}$ normalized to 0.5 I_{D25} value vs. T_J

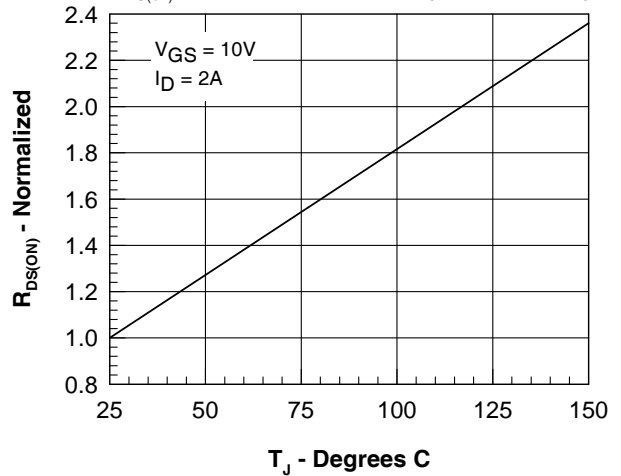


Figure 7. Gate Charge

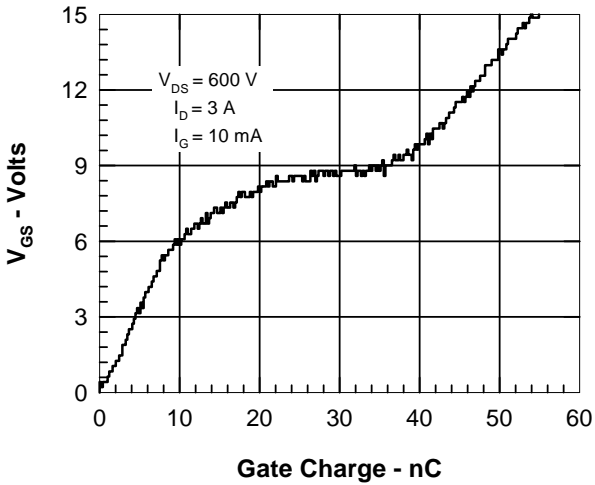


Figure 8. Capacitance Curves

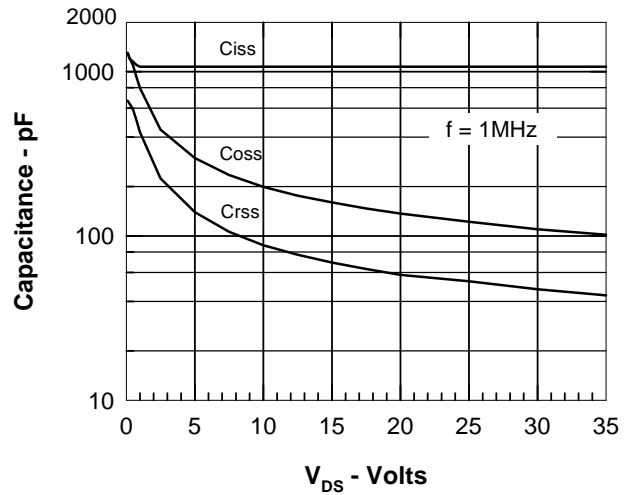


Figure 9. Forward Voltage Drop of the Intrinsic Diode

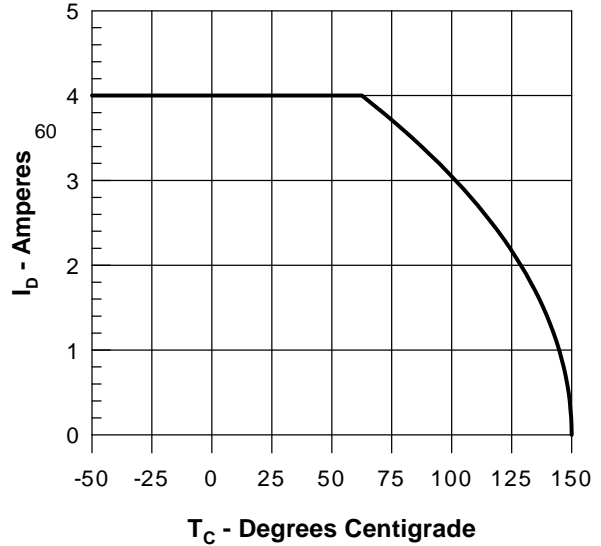
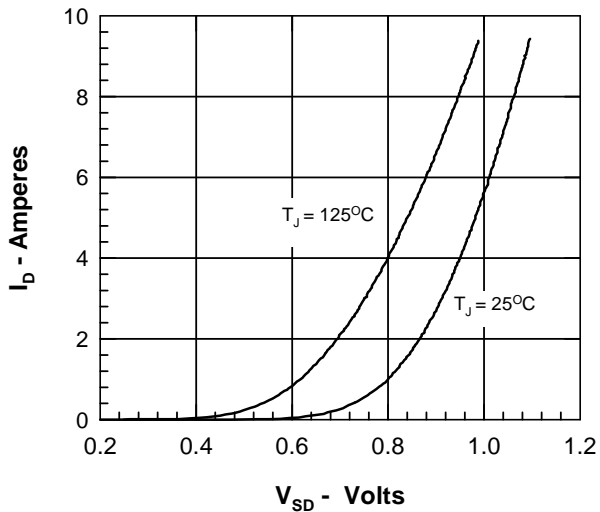
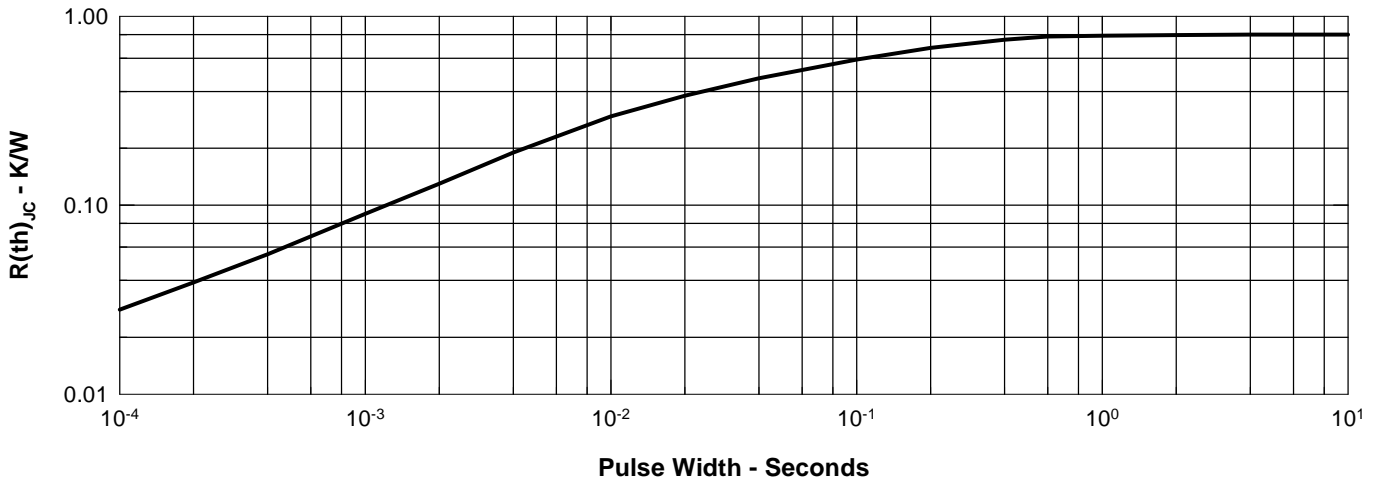


Figure 11. Transient Thermal Resistance





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