PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/13/8276
Dated 27 Dec 2013

M93S46, M93S56 & M93S66, MICROWIRE serial EEPROM with block protection Industrial grade Redesign & upgrade to the CMOSF8H process technology

Table 1. Change Implementation Schedule

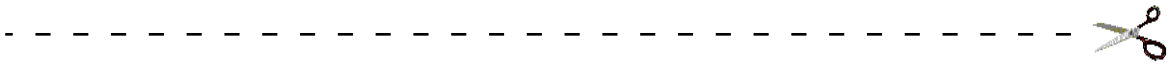
Forecasted implementation date for change	20-Dec-2013
Forecasted availability date of samples for customer	20-Dec-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	31-Jan-2014
Estimated date of changed product first shipment	28-Mar-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M93S46, M93S56, M93S66 Industrial grade
Type of change	Waferfab technology change
Reason for change	Line up to state-of-the-art of process
Description of the change	Redesign and upgrade to the new CMOSF8H process technology.
Change Product Identification	Process Technology identifier "K" for CMOSF8H
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/13/8276**
Please sign and return to STMicroelectronics Sales Office	**Dated 27 Dec 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Marketing Manager
Rodrigues, Benoit	Product Manager
Pavano, Rita	Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

M93S46, M93S56 & M93S66, 1-Kbit, 2-Kbit & 4-Kbit MICROWIRE serial access EEPROM with block protection Industrial grade Redesign and upgrade to the CMOSF8H process technology

What is the change?

The **M93S46, M93S56 and M93S66,** *1-Kbit, 2-Kbit and 4-Kbit MICROWIRE serial access EEPROM with block protection* product families for industrial grade, currently produced using the CMOSF6SP 36% process technology at ST Ang Mo Kio (Singapore) 6" or at GLOBALFOUNDRIES (Singapore) 8" wafer diffusion plants, have been **redesigned** and will be **upgraded** to the **CMOSF8H** process technology at **ST Rousset** (France) 8" wafer diffusion plant.

This upgraded version in CMOSF8H allows offering:

- Write cycles up to 4 millions
- Data retention up to 200 years

The new M93S46, M93S56 and M93S66 in CMOSF8H version are functionally compatible with the current CMOSF6SP 36% version as per common datasheet rev. 5 – March 2013, attached.

These new M93S46, M93S56 and M93S66 are described in a common datasheet for **M93Sxx** rev. 6.

Concurrent to this change, the new M93S46, M93S56 and M93S66 in CMOSF8H, in SO8N, will be assembled with 0.8 mil Copper wire.

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M93S46, M93S56 and M93S66 in the new CMOSF8H process technology will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the upgraded new M93S46, M93S56 and M93S66 in CMOSF8H with the new CMOSF8H will ramp up from January 2014 and shipments can start from end of March 2014 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the new M93S46, M93S56 and M93S66 in CMOSF8H will be qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

Qualification Plan QPMMY1330 is included inside this document, **Qualification Report QRMMY1330** will be available Week 05 / 2014.

What is the impact of the change?

- **Form:** Marking change (see **Device marking** paragraph)

- **Fit:** No change

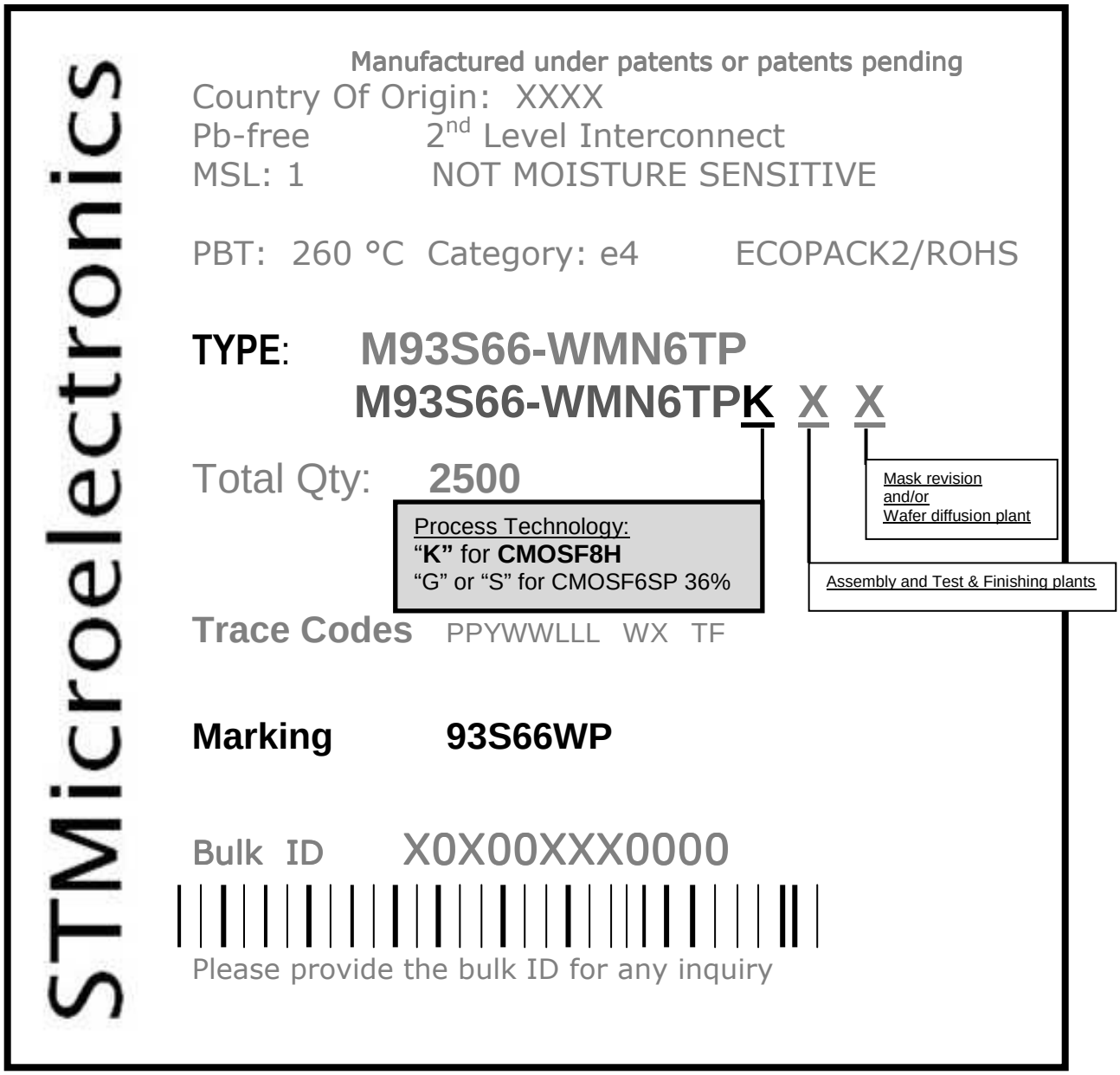
- **Function:** Change on DC characteristic **I_{CC1} standby supply current**

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "K" for the **upgraded version** in **CMOSF8H**, this identifier being "G" or "S" for the current version in CMOSF6SP 36%.

➔ *Example for M93S66-WMN6TP*



How can the change be seen?

- DEVICE MARKING

For the **SO8N** package, the difference is visible inside the trace code (*PYWWT*) where the last digit is "**K**" for the **upgraded version** in **CMOSF8H**, this digit being "G", or "S" for current versions.

	Upgraded CMOSF8H (ST Rousset)	Current CMOSF6SP 36% **(ST Ang Mo Kio)**	Current CMOSF6SP 36% **(GLOBALFOUNDRIES)**
SO8N Example: M93S66-WMN6TP			

Appendix A- Product Change Information

Product family / Commercial products:	M93S46, M93S56, M93S66 products families / Industrial grade
Customer(s):	All
Type of change:	Wafer fab process technology change
Reason for the change:	Line up to state-of-the-art of process
Description of the change:	Redesign and upgrade to the new CMOSF8H Process technology.
Forecast date of the change: **(Notification to customer)**	Week 51 / 2013
Forecast date of **Qualification samples availability for customer(s):**	Available
Qualification Report availability:	The **Qualification Plan QPMMY1330** is included inside this document. **Qualification Report QRMMY1330** will be available Week 05 / 2014.
Marking to identify the changed product:	Process Technology identifier "K**"** for CMOSF8H.
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 13 / 2014

Appendix B: Concerned Commercial Part Numbers:

Commercial Part Numbers	Package	Samples availability
M93S46-WMN6P	SO8N	(no sample for tube delivery)
M93S46-WMN6TP	SO8N	Available
M93S56-WMN6P	SO8N	(no sample for tube delivery)
M93S56-WMN6TP	SO8N	Available
M93S66-WMN6P	SO8N	(no sample for tube delivery)
M93S66-WMN6TP	SO8N	Available

Appendix C: Qualification Plan:

See following pages

M93Sxx Redesign and Upgrade to the CMOSF8H process technology Qualification Plan QPMMY1330 (1/3)

- The new version of the M93Sxx (xx = 46, 56, 66) in CMOSF8H will be qualified using the standard STMicroelectronics corporate procedures for quality and reliability.
- The CMOSF8H process technology and EEPROM new design core have been qualified for Industrial and Automotive products on 3 lots using the driver product M95640 (refer to qualification report QREE0921).
- The M93Sxx microwire serial access EEPROM products are designed with the same technology and similar architecture as the driver product M95640.

M93Sxx Redesign and Upgrade to the CMOSF8H process technology Qualification Plan QPMMY1330 (2/3)

- M93Sxx devices are derived from M93Cxx by metal mask option (same design core), allowing a qualification by similarity, except for all ESD and Latch-up tests.

- The product vehicles used for the die and package qualifications are presented in *Table 1* and *Table 2* respectively.

Table 1. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M93Sxx	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)
M93Cxx (2)	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.
2. M93Sxx are derived from M93Cxx devices by metal mask option (same design core). Die qualification results obtained on M93Cxx are applicable to M93Sxx devices, except for all ESD / Latch-up tests.

Table 2. Product vehicle used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M93Cxx	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen

M93Sxx Redesign and Upgrade to the CMOSF8H process technology
Qualification Plan QPMMY1330 (3/3)

- The reliability test plan related to the new M93Sxx is presented as follows :

Test	Test short description					
	Method	**Conditions**	**Sample size / lot**	**No. of lots**	**Duration**	**Acceptance Criteria**
ESD HBM	**Electrostatic discharge (human body model)**					
	AEC-Q100-002 JESD22-A114	C = 100 pF, R = 1500 Ohms	27	1	N/A	PASS 4000 V
ESD MM	**Electrostatic discharge (machine model)**					
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ohms	12	1	N/A	PASS 400 V
ESD CDM	**Electrostatic discharge (charge device model)**					
	AEC-Q100–011 JESD22-C101	Field induced charging method	18	1	N/A	PASS 1500 V
LU	**Latch-up (current injection and over-voltage stress)**					
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	1	N/A	Class II – Level A

Document Revision History

Date	Rev.	Description of the Revision
November 19, 2013	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

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