



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/14/8744
Dated 21 Oct 2014

CR95HF, Redesign for improvement

Table 1. Change Implementation Schedule

Forecasted implementation date for change	14-Oct-2014
Forecasted availability date of samples for customer	14-Oct-2014
Forecasted date for STMicroelectronics change Qualification Plan results availability	14-Oct-2014
Estimated date of changed product first shipment	20-Jan-2015

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	CR95HF-VMD5T
Type of change	Product design change
Reason for change	New functions & usages
Description of the change	Improvement & design corrective actions
Change Product Identification	Marking changed to CR95HFV5 LE
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Fidelis, Sylvain	Marketing Manager
Rodrigues, Benoit	Product Manager
Pavano, Rita	Q.A. Manager

CR95HF, Redesign for improvement

What is the change?

The **CR95HF**, NFC Reader IC, assembled in VFQFPN32 and processed with the CMOSF9 process technology at ST Rousset (France) 8" wafer diffusion plant, has been **redesigned** for **improvement**.

Following parameters will be updated in revised datasheet rev. 10, October 2014.

- Corrected function :
 - o **ISO/IEC 14443-A 4-bit frame report** supported:
 - Used during ISO/IEC 14443-A anti-collision process to return ACK & NAK values.
- Improved performance
 - o **Data exchange buffer** size increased from 256 to **528 bytes**:
 - Used for data transmission or reception. Will allow bigger RF frame management.
 - o **Main supply extended to Max 5.5 V** (VPS_Main).
- Design flexibility
 - o **Parity bit management** support:
 - Directly manages the value of parity bit to be included in a standard ISO/IEC 14443-A frame.
 - o Enhance Error code list:
 - Allows user to more visibility on CR95HF behavior.
 - Backward compatibility with previous error code.
 - o Optional parameters for Protocol Select Command added:
 - Brings more flexibility in timing definition (Frame Waiting Time, TR0, TR1 ...).
- Customer information
 - o Response to IDN command (ASCII): **FS2JAST4** (ROM code Rev **4**)
(was **FS2JAST2** for ROM code Rev **2**)

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the CR95HF with the new design will bring new functions and usages to our customers.

When?

The production of the upgraded CR95HF will ramp up from October 2014 and shipments can start from January 2015 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the CR95HF will be qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

The **Qualification Report QRMMY1123 rev. 3** is available and included inside this document.

What is the impact of the change?

- **Form:** Marking change (see **Device marking** paragraph)
- **Fit:** No change
- **Function:**
 - 4-bit frame supported
 - Data buffer extended to 528 bytes
 - Main supply VPS_Main range extended to (V) [2.7 - 5]
 - Parity bit management supported
 - Error code list enhanced
 - Optional parameter for Protocol Select Command
 - IDN command response changed

How can the change be seen?

- **BOX LABEL MARKING**

The difference is visible inside the **Finished Good Part Number** where the mask revision identifier is “E” for the **new design**, this identifier being “A” for the current version.

STMicroelectronics

Manufactured under patents or patents pending
Country Of Origin: XXXX
Pb-free 2nd Level Interconnect
MSL: 1 NOT MOISTURE SENSITIVE

PBT: 260 °C Category: e4 ECOPACK2/ROHS

TYPE: **CR95HF-VMD5T**
CR95HF-VMD5T L B E

Total Qty: **3000**

Process Technology


Assembly and Test & Finishing plants

Mask revision:
“E” for new design
“A” for previous version

Trace Codes PPYWLLLL WX TF

Marking **CR95HFV5**

Bulk ID **X0X00XXX0000**



Please provide the bulk ID for any inquiry

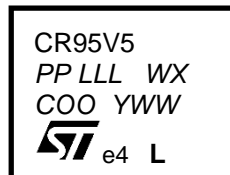
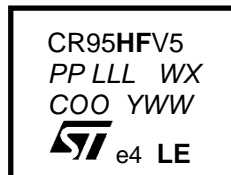
How can the change be seen?
- DEVICE MARKING

The difference is visible inside the **product name**:

- **New design** is **CR95HFV5**, current design being CR95V5
- **Additional marking** being "**LE**" for **new design**, current one being "L"

New design

Current



Appendix A- Product Change Information

Product family / Commercial products:	CR95HF-VMD5T
Customer(s):	All
Type of change:	Design change
Reason for the change:	New functions & usages
Description of the change:	Improvement & design corrective actions
Forecast date of the change: (Notification to customer)	Week 42/ 2014
Forecast date of <u>Qualification samples</u> availability for customer(s):	Available
Forecast date for the internal STMicroelectronics change, <u>Qualification Report</u> availability:	The Qualification Report QRMMY1123 <u>rev. 3</u> is available and included inside this document.
Marking to identify the changed product:	CR95HFV5 LE
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	CR95HF-VMD5T
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 03 / 2015

Appendix B: Qualification Report (rev.2):

See following pages

New product / CR95HF
using the CMOSF9 technology in the Rousset 8" Fab

Table 1. Product information

General information	
Commercial product	CR95HF-VMD5T
Product description	13.56-MHz multi-protocol contactless transceiver IC with SPI and UART serial access
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF9
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France

Table 2. Package description

Package description	Qualified assembly plant location	Qualified final test plant location
32-lead VFQFPN (5 x 5 mm)	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product CR95HF using the CMOSF9 silicon process technology in the ST Rousset 8" diffusion fab.

The voltage range covered by this document is:

- Main supply VPS_Main: 2.7 to 5.5 V

The temperature range covered by this document is:

- -25 to 85 °C

The CMOSF9 silicon process technology is already qualified in the ST Rousset 8" diffusion fab and in production for MMS products.

This document serves for the qualification of the named product, using the named silicon process technology in the named diffusion fab.

1.2 Conclusion

The new product CR95HF using the CMOSF9 silicon process technology in the ST Rousset 8" diffusion fab has passed the reliability requirements and the product described in [Table 1](#) is qualified.

Refer to [Section 3: Reliability test results](#) for details on the reliability test results.

2 Device characteristics

The CR95HF is an integrated transceiver IC for contactless applications.

The CR95HF manages frame coding and decoding in Reader mode for standard applications such as near field communication (NFC), proximity and vicinity standards.

The CR95HF embeds an Analog Front End to provide the 13.56 MHz Air Interface.

The CR95HF supports ISO/IEC 14443 Type A and B, ISO/IEC 15693 (single or double subcarrier) and ISO/IEC 18092 protocols.

The CR95HF also supports the detection, reading and writing of NFC Forum Type 1, 2, 3 and 4 tags.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the qualification is presented in [Table 3](#).

Table 3. Product vehicle used for qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
CR95HF	CMOSF9	ST Rousset 8"	32-lead VFQFPN (5 x 5 mm)	Subcon Amkor

3.1 Reliability test plan and result summary

The reliability test plan and the result summary is presented in [Table 4](#).

Table 4. Reliability test plan and result summary (32-lead VFQFPN 5 x 5 mm / Amkor)⁽¹⁾

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						CR95HF			
						Lot 1	Lot 2	Lot 3	Lot 4 ⁽²⁾
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	231	1	N/A	0/231	-	-	-
HTSL ⁽³⁾	High temperature storage life								
	JESD22-A103	Retention bake at 150 °C	77	1	1008 hrs	0/77	-	-	-
TC ⁽³⁾	Temperature cycling								
	JESD22-A104	-65 °C / +150 °C	77	1	1000 cycles	0/77	-	-	-
AC ⁽³⁾	Autoclave (pressure pot)								
	JESD22-A102	121 °C, 100% RH at 2 ATM	77	1	96 hrs	0/77	-	-	-
HTOL ⁽⁴⁾	High temperature operating life								
	JESD22-A108	HTOL 140 °C, 5 V	77	3	1008 hrs	0/77	0/77	0/77	-
ESD HBM ⁽⁴⁾	Electrostatic discharge (human body model)								
	JESD22-A114	C = 100 pF, R = 1500 Ω	27	3	N/A	Pass 2000V	Pass 2000V	Pass 2000V	Pass 2000V
ESD MM ⁽⁴⁾	Electrostatic discharge (machine model)								
	JESD22-A115	C = 200 pF, R = 0 Ω	15	3	N/A	Pass 200V	Pass 200V	Pass 200V	Pass 200V
ESD CDM	Electrostatic discharge (charge device model)								
	JESD22-C101	Field induced charging method	18	1	N/A	Pass 1000V	-	-	-
LU ⁽⁴⁾	Latch-up (current injection and overvoltage stress)								
	JESD78A	At maximum operating temperature (85 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A	Class II Level A

1. See [Table 5: List of terms](#) for a definition of abbreviations.
2. Reliability results on lot 4 obtained on improved design (PCN MMS-MMY/14/8744).
3. HTSL-, TC-, AC- dedicated parts are first subject to preconditioning flow.
4. Performed on engineering ceramic package CDIP24.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD22-C101: Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 5. List of terms

Terms	Description
HTOL	High temperature operating life
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
05-Jun-2012	1	Initial release.
14-Oct-2013	2	<i>Section 1.1: Objectives</i> updated.
10-Oct-2014	3	<i>Table 4</i> updated with reliability results obtained on improved design (PCN MMS-MMY/14/8744). <i>Section 1.1: Objectives</i> updated.

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