Keywords: T1, E1, T1/E1, 8MHz, backplane, PCM, pulse code modulation, elastic store, DS0, 2.048MHz, system clock, framer, byte interleaved, IBO, interleave bus operation, SCTs, single chip transceiver, stream

APPLICATION NOTE 301

Legacy T1/E1 8MHz Backplane Operation

May 29, 2001

Abstract: This application note provides the requirements for multiplexing four PCM streams into one 8MHz system backplane using Dallas Semiconductor/Maxim SCTs and framers that do not contain interleave bus operation (IBO) modes internally.The DS2155, DS26528, DS26524, DS26522, DS26521, DS26519 and DS26518 all contain IBO functionality without external circuitry and are recommended for new designs.

Introduction

This application note applies to the following products:

T1 Framers	E1 Framers	T1 SCTs	E1 SCTs
DS2141A	DS2143	DS2151	DS2153
DS21Q41B	DS21Q43A	DS2152	DS2154

This application note will discuss the requirements for multiplexing four PCM streams into one 8MHz system backplane using Dallas Semiconductor SCTs and framers that do not contain interleave bus operation (IBO) functionality internally. The DS2155, DS26528, DS26524, DS26522, DS26521, DS26519 and DS26518 all contain IBO functionality internally and do not need the extra logic shown below.

T1 or E1 PCM signals can interface to an 8MHz system backplane. Typically, this application is used to multiplex four PCM streams onto a single 8MHz PCM stream. To accomplish this, the elastic stores are enabled and placed in the 2.048MHz SYSCLK mode. **Figure 1** illustrates a circuit in which a single SYNC signal is generated for all four framers. Each framer in turn is driven with an 8.192MHz clock burst of 8 cycles. Each clock burst causes the elastic store to output one DS0. This results in a byte-interleaved 8.192MHz PCM steam (see **Figure 2**).

Figures 1 and 2 apply to the DS2152 and DS2154. Figure 1 shows the 8.192MHz clock can optionally be derived from a master DS2152/54.
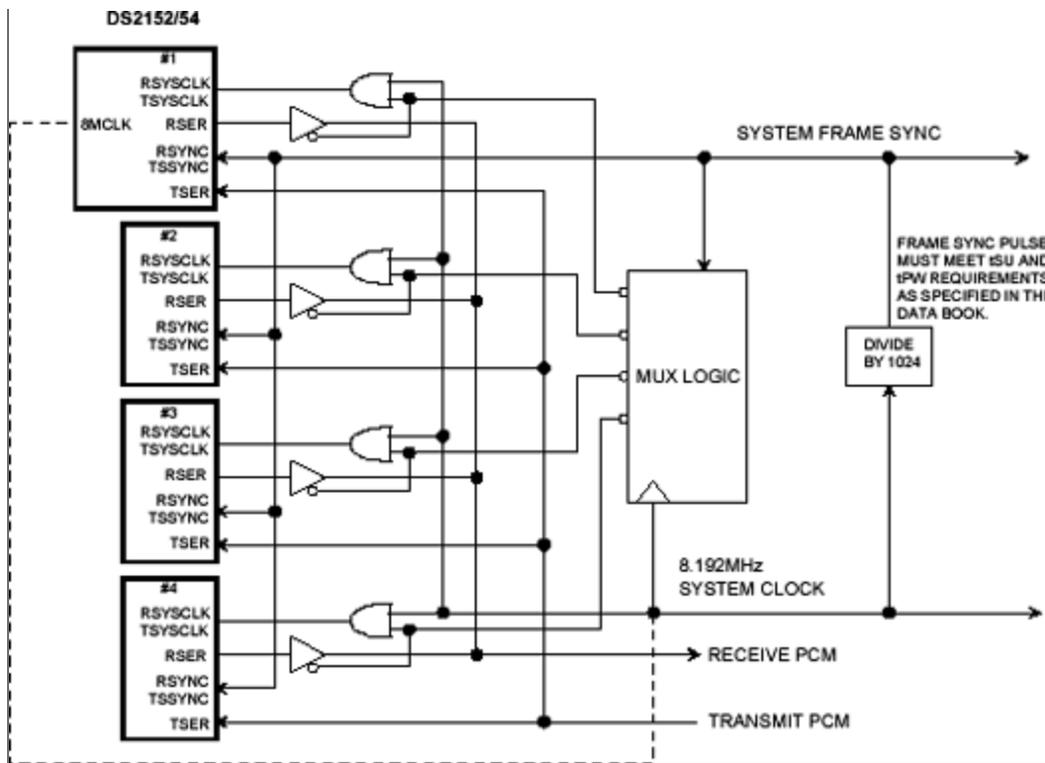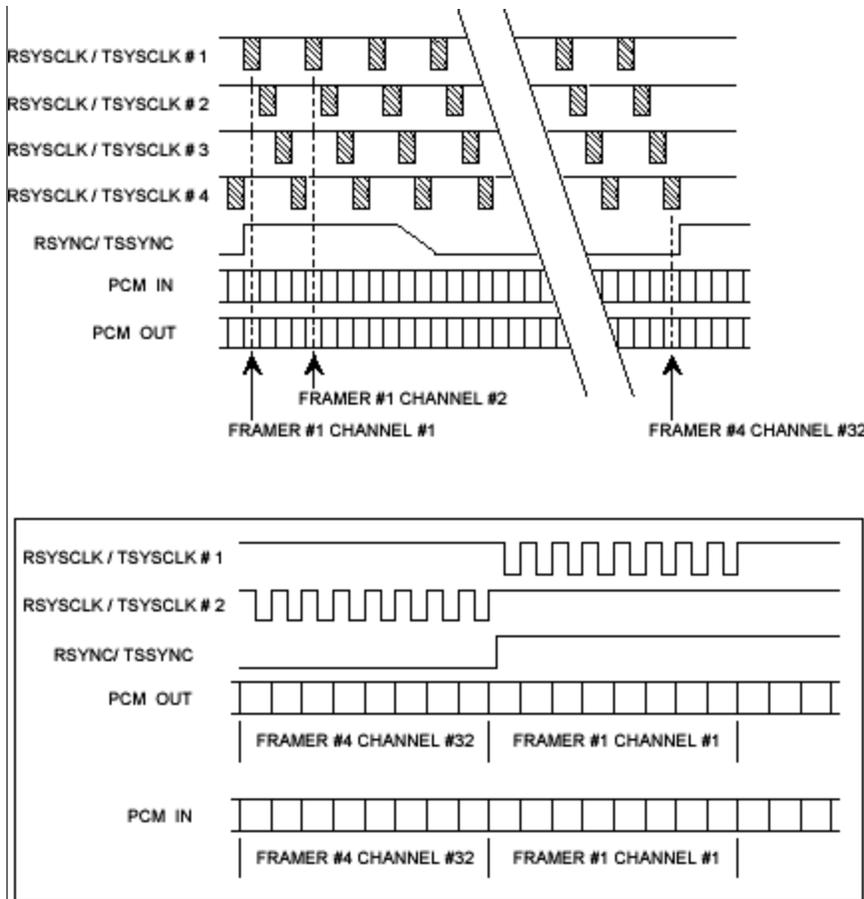
Figure 1.

Figure 2.

Master Clock Source

In Figure 1, the 8.192MHz system clock may be derived from a T1/E1 line as indicated by the dotted line. This line becomes the timing master for the other three devices. In this example, device #1 is used as the master. The other three devices may experience frame slips since there is no guarantee that their inbound T1/E1 rates are synchronous to device #1's inbound rate. The elastic stores manage frame slip events in a logical manner by either repeating or deleting a full frame.

Master Clock Failure

In the event that the master line fails, the following events will occur. RCLK will be replaced by MCLK. If the jitter attenuator is enabled in the receive path, this transition will be very smooth. Consequently, the 8.192MHz clock output on the 8 MCLK pin will make a slight and smooth transition to be phase locked to the clock at MCLK. The 8.192MHz system timing will not experience any disturbance of the byte interleave structure. Device #1 will report a receive carrier loss (RCL) event via the status registers. When the host detects the failure of the master line, processor selection logic may be used to switch to another active line.

Figures 3 and **4** apply to the DS2141, DS21Q41, DS2143, DS21Q43, DS2151, and DS2153.
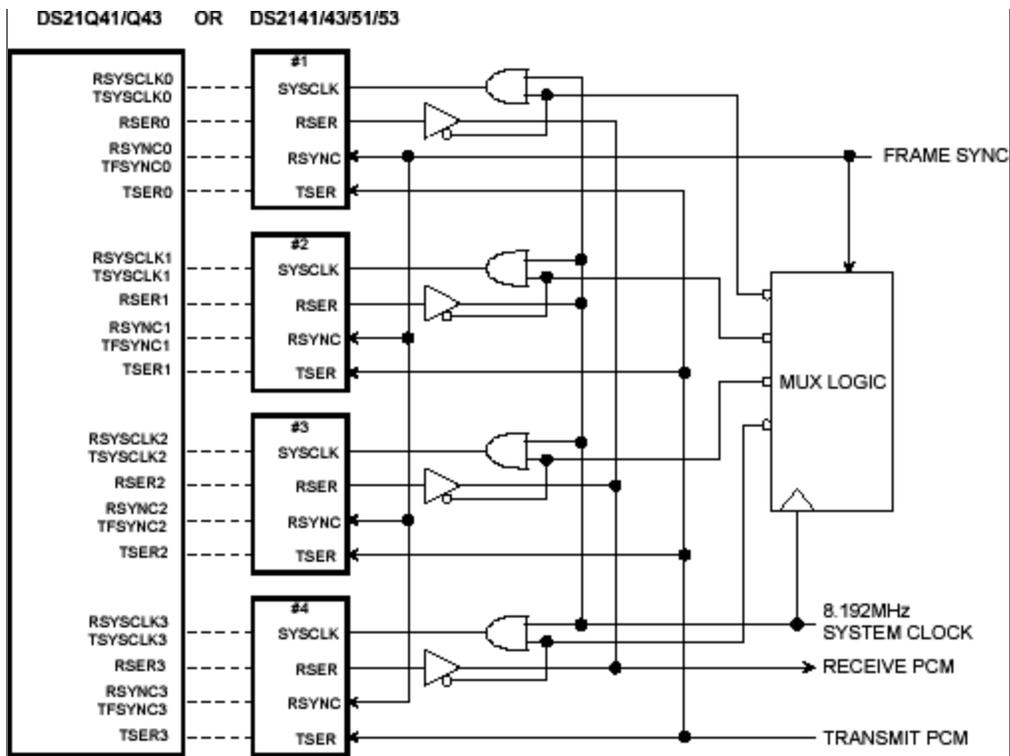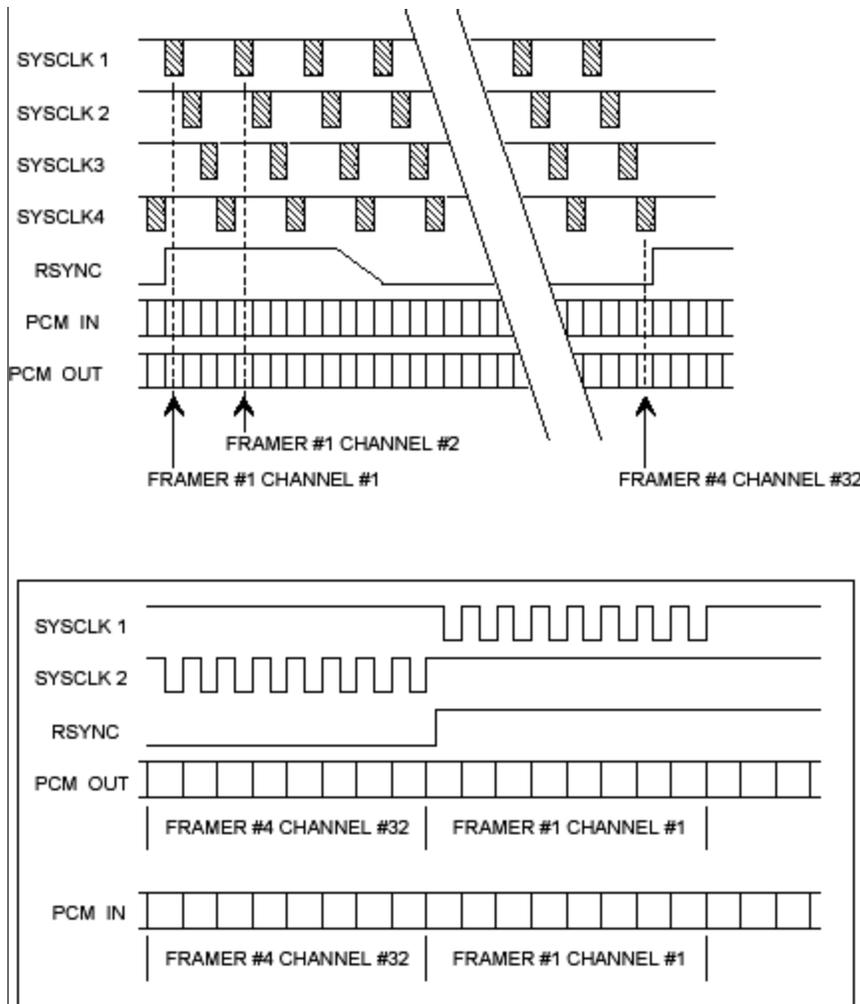
Figure 3.

Figure 4.

Backplane Information

If you have further questions on backplane operation of our legacy T1/E1 products, please contact the Telecommunication Applications support team.

For more information about our legacy T1/E1 products, please consult the data sheets available on our website at www.maximintegrated.com/telecom.

Related Parts		
DS2143	E1 Controller	
DS2152	Enhanced T1 Single Chip Transceiver	
DS2154	Enhanced E1 Single Chip Transceiver	
DS26518	8-Port T1/E1/J1 Transceiver	Free Samples
DS26519	16-Port T1/E1/J1 Transceiver	Free Samples

DS26521	Single T1/E1/J1 Transceiver	Free Samples
DS26522	Dual T1/E1/J1 Transceiver	Free Samples
DS26524	Quad T1/E1/J1 Transceiver	Free Samples
DS26528	Octal T1/E1/J1 Transceiver	Free Samples

More Information
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