MAX2082

Low-Power, High-Performance Octal Ultrasound Transceiver with Integrated AFE, Pulser, T/R Switch, and CWD Beamformer

General Description

The MAX2082 is the world's first fully-integrated octal ultrasound transceiver. The device is optimized for high-channel-count, high-performance portable and cart-based ultrasound systems. The easy-to-use transceiver allows the user to achieve high-end 2D and Doppler imaging capability using substantially less space and power.

The transceiver transmitters are high-performance, 3-level 2A pulsers capable of generating high-voltage pulses up to ±105V.

The highly compact receiver with T/R switch, LNA, input coupling and feedback capacitors, variable gain amplifier (VGA), anti-aliasing filter (AAF), analog-to-digital converter (ADC), and digital highpass filter (HPF) achieves an ultra-low noise figure with $R_S = R_{IN} = 200\Omega$ at a very low 131mW per-channel power dissipation at 50Msps. The receive channel has been optimized for second harmonic imaging with -66dBFS second harmonic distortion performance at f_{RF} = 5MHz over the full gain range. The full receive channel exhibits an exceptional 76dBFS SNR at 5MHz with a 2MHz bandwidth.

Separate mixers for each channel are made available for optimal CWD sensitivity yielding an impressive 149dBc/Hz dynamic range per channel at 1kHz offset from the 1.25MHz carrier.

The MAX2082 octal ultrasound front-end is available in a small 10mm x 23mm CSBGA package and is specified over a 0°C to +70°C temperature range.

Benefits and Features

- Minimizes PCB Area and Design Cost
  - 8 Full Channels of HV Pulser, T/R-Switch, LNA Input and Feedback Coupling Caps, LNA, VGA, AAF, CWD Mixers, 12-Bit ADC, and Digital HPF in a Small 10mm x 23mm CSBGA Package
- Integrated HV Pulser for Simpler System Design
  - High-Voltage 3 Level Pulsers (Up to ±105V) with Active Return to Zero and Internal Power-Supply Drivers for Reduced External Components
  - Programmable Pulser Current Capability from 0.5A to 2A for Reduced Power Consumption in Lower Voltage Transmit Modes Like CWD
  - Extremely Low Propagation Delay Pulsers (18ns) with Excellent Rise and Fall Matching for Excellent THD2 Performance (-43dBc at 5MHz)
- Integrated High-Performance Receiver Improves System Sensitivity
  - Ultra-Low Full-Channel Receiver Noise Figure of 2.8dB at $R_{IN} = R_S = 200\Omega$ (Without T/R Switch)
  - High Dynamic Range Receiver with 76dBFS SNR at f_{IN} = 5MHz and 2MHz Bandwidth
  - Ultra-Low Power Receiver (131mW Per Channel)

Applications

- Ultrasound Imaging

***Ordering Information* appears at end of data sheet.**

19-6601; Rev 0; 9/14

maxim integrated™

Typical Application Circuit

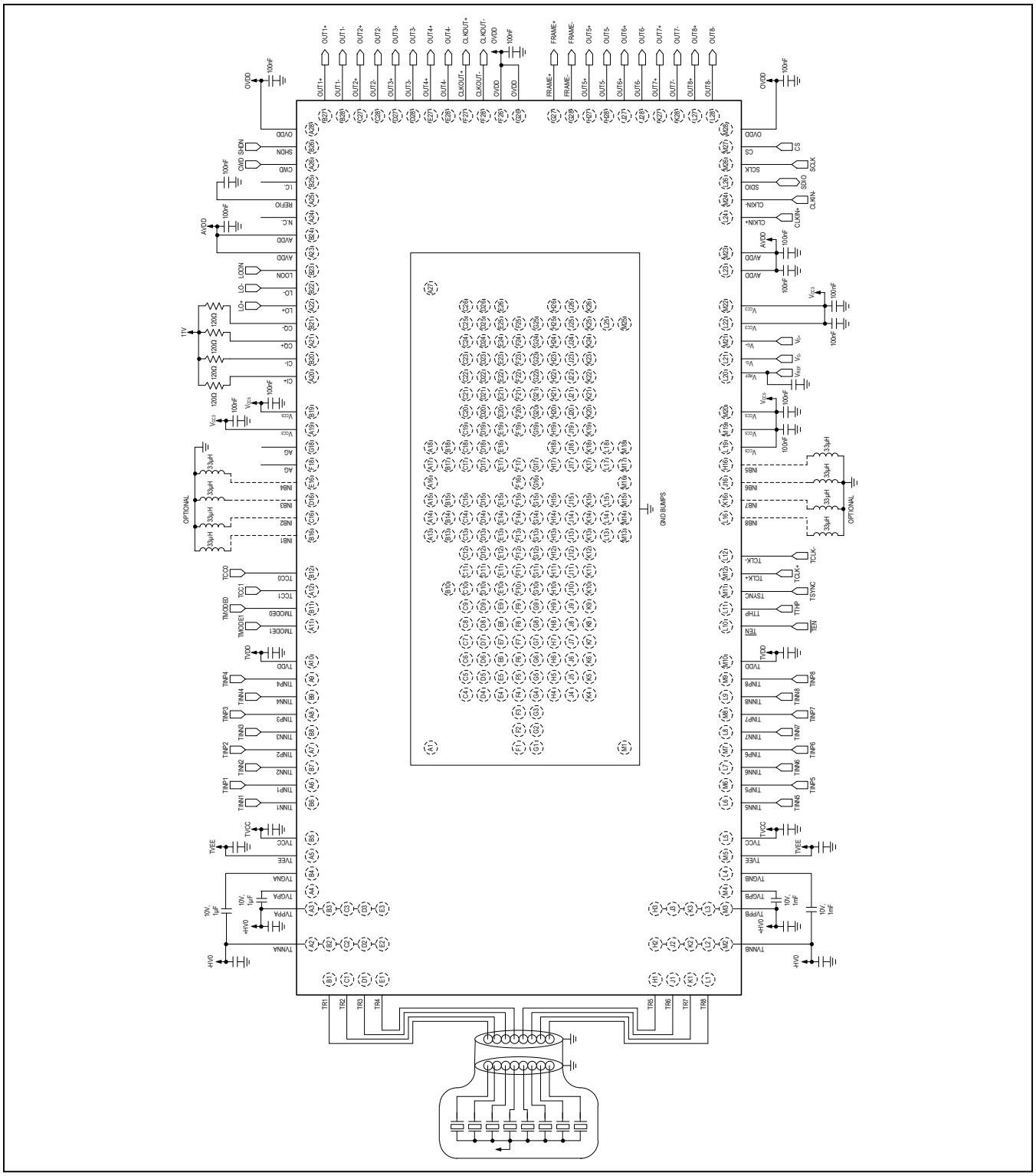


TABLE OF CONTENTS

General Description . . . 1
Benefits and Features . . . 1
Applications . . . 1
Typical Application Circuit . . . 2
Absolute Maximum Ratings . . . 8
Package Thermal Characteristics . . . 8
Octal Ultrasound Front-End Specifications . . . 8
DC Electrical Characteristics—T/R Switch and Transmitter . . . 8
AC Electrical Characteristics—T/R Switch and Transmitter . . . 15
DC Electrical Characteristics—LNA, VGA, ADC (CWD Beamformer Off) . . . 17
AC Electrical Characteristics—VGA MODE (CWD Beamformer Off) . . . 18
DC Electrical Characteristics—CWD MODE (VGA, AAF, and ADC Off) . . . 21
AC Electrical Characteristics—CWD MODE (VGA, AAF, and ADC Off) . . . 22
Electrical Characteristics——AFE Clock and Timing . . . 24
Timing Diagrams . . . 26
Typical Operating Characteristics . . . 31
Bump Configuration . . . 37
Bump Description . . . 38
Functional Diagram . . . 42
Detailed Description . . . 43
Transmit Pulser . . . 43
- Modes of Operation . . . 43
  - Shutdown Mode (TMODE0, TMODE1 = 00) . . . 43
  - Octal 3 Level Mode (TMODE0, TMODE1 = 10) . . . 43
  - Disable Transmit Mode (TMODE0, TMODE1 = 11) . . . 43
- Current Capability Selection . . . 43
- Sync Feature . . . 44
- T/R Switch and Control . . . 44
- Grass Clipping Diodes . . . 44
- Active Damp Circuit . . . 45
- Independent (Floating) Power-Supply Enable (TEN) . . . 45
- Thermal Protection . . . 45

Analog Front End (AFE) . . . 45
- Modes of Operation . . . 45
- Low-Noise Amplifier (LNA) . . . 45
- Variable-Gain Amplifier (VGA) . . . 45
- Overload Recovery . . . 46
- Octal Continuous-Wave (CW) Mixer . . . 46

TABLE OF CONTENTS (continued)

CW Mixer Output Summation . . . 46
LO Phase Select . . . 46
VGA and CW Mixer Operation . . . 46
External Voltage Reference . . . 46
ADC Clock Input . . . 46
Power-Down and Low-Power Mode . . . 48
Programmable, Digital Highpass 2-Pole Filter . . . 48
Digital Highpass Filter Characteristics . . . 48
System Timing Requirements . . . 54
Clock Output (CLKOUT+, CLKOUT-) . . . 54
Frame-Alignment Output (FRAME+, FRAME-) . . . 55
Serial-Output Data (OUT_+, OUT_-) . . . 55
Differential LVDS Digital Outputs . . . 55
Output Driver Level Tests . . . 56
Data Output Test Patterns . . . 56
Power Management . . . 56
Power-On and Reset . . . 56
Power-Down and Low-Power (Nap) Mode and Channel Selection . . . 56
3-Wire Serial Peripheral Interface (SPI) . . . 57
SPI Communication Format . . . 57
Output Clock Phase . . . 57
Custom Test Pattern . . . 61
Clock Input Termination . . . 64
CW Doppler Mode Control . . . 67
Soft Reset . . . 68
AFE Programming and Data Transfer . . . 68
CWD Beamformer Programming and Clocking . . . 68
Applications Information . . . 69
Layout Concerns . . . 69
Power-Supply Sequencing . . . 69
Ordering Information . . . 70
Chip Information . . . 70
Package Information . . . 70
Revision History . . . 71

LIST OF FIGURES

Figure 1. CWD LOON LO Turn-On/Turn-Off Setup Time 26
Figure 2. HV Burst Test (Three Levels) 26
Figure 3. Propagation Delay Timing 27
Figure 4. Output Rise/Fall Timing 27
Figure 5. T/R Switch Turn-On/Off TIme 28
Figure 6. Bandwidth 29
Figure 7. Jitter Timing 30
Figure 8. Simplified Clock Input Schematic 45
Figure 9. CWD Analog Front-End Beamformer Simplified Block Diagram 47
Figure 10. CWD Output Beamforming Example 47
Figure 11. Simplified Clock Input Schematic 48
Figure 12. Two-Stage Digital Highpass Filter with 1-Stage Multiplier 49
Figure 13. Digital HPF Magnitude Frequency Response (1 Stage) 51
Figure 15. Digital HPF Phase Response (1 Stage) 51
Figure 14. Digital HPF Magnitude Frequency Response (1 Stage) at Corner Frequency 51
Figure 16. Digital HPF Group-Delay Frequency Response (1 Stage) 51
Figure 17. Digital HPF Impulse-Time Response (1 Stage) 52
Figure 19. Digital HPF Magnitude Frequency Response (2 Stage) 52
Figure 18. Digital HPF Impulse-Time Response Detailed Plot (1 Stage) 52
Figure 20. Digital HPF Magnitude Frequency Response (2 Stage) at Corner Frequency 52
Figure 21. Digital HPF Phase Response (2 Stage) 53
Figure 23. Digital HPF Impulse-Time Response (2 Stage) 53
Figure 22. Digital HPF Group-Delay Frequency Response (2 Stage) 53
Figure 24. Digital HPF Impulse-Time Response Detailed Plot (2 Stage) 53
Figure 25. Digital HPF Gain vs. Filter Coefficient 54
Figure 26. ADC Timing (Overall) 54
Figure 27. ADC Timing (Detail) 55
Figure 28. Serial Output Detailed Timing Diagram 55
Figure 29. SPI Timing Diagram 58
Figure 30. Output Clock Phase 61
Figure 31. Ultrasound-Specific IMD3 69

LIST OF TABLES

Table 1. Transmit Pulser Operating Modes and Truth Table 44
Table 2. Transmit Pulser Output Current 44
Table 3. Digital Filter Cutoff-Frequency Setting 49
Table 4. Gain-Compensation Settings for Different Filter Cutoff-Frequency Settings 50
Table 5. User-Programmable ADC Control Registers 59
Table 6. PLL Sampling Rate and Power Management (00h) 59
Table 7. PLL Frequency-Control Settings (00h[6:4]) 59
Table 8. Power-Management Programming 60
Table 9. Output Data Format and Test Pattern/Digital HPF Select (01h) 60
Table 10. LVDS Output Data Format Programming (01h[1:0]) 61
Table 11. Test Pattern Programming and Digital Highpass Filter Selection 61
Table 12. Pseudorandom Data Test Pattern 62
Table 13. LVDS Output Driver Level (02h) 62
Table 14. Test Data (OUT_) Level Programming 62
Table 15. Test CLKOUT_ Level Programming 62
Table 16. Test FRAME Level Programming 62
Table 17. LVDS Output Common-Mode Voltage Adjustment 62
Table 18. LVDS Output Driver Management (03h) 63
Table 19. LVDS Output Drive Current Configuration 63
Table 20. LVDS Output Driver Internal Termination Configuration 63
Table 21. CLKIN Termination Control (04h) 63
Table 22. Channel Power Management: SHDN0 (05h) 64
Table 23. Channel Power Management: SHDN1 (06h) 64
Table 24. Digital Highpass Filter Control Coefficients (07h; If TEST_DATA 01[4]) = 0) 64
Table 25. Digital Highpass Filter Configuration 64
Table 26. Custom Test Pattern 1 (07h; If TEST_DATA 01[4]) = 1) 64
Table 27. Digital Highpass Filter Attenuation (08h; If TEST_DATA 01[4]) = 0) 65
Table 28. Digital Highpass Filter Attenuation 65
Table 29. Custom Test Pattern 2 (08h; If TEST_DATA 01[4]) = 1) 65
Table 30. Custom Test Pattern 3 (09h) 65
Table 31. AFE Settings (0Ah) 65

LIST OF TABLES (continued)

Table 32. AFE Input Impedance and LNA Gain Control 65
Table 33. AFE AAF Filter Bandwidth Control 66
Table 34. CWD Power Mode 66
Table 35. VGA Output Clamp Control 66
Table 36. CW Beamformer 1 (0Bh) 66
Table 37. CW Beamformer 2 (0Ch) 66
Table 38. CW Beamformer 3 (0Dh) 66
Table 39. CW Beamformer 4 (0Eh) 66
Table 40. CW Beamformer 5 (0Fh) 67
Table 41. Phase Rotation Bit Weight 67
Table 42. Phase Rotation Summary 67
Table 43. Special Function Register (10h) 67
Table 44. Status Byte (Reads from 10h) 68
Table 45. SPI Commands (Writes to 10h) 68

Absolute Maximum Ratings

V_{CC5}, V_{CC3} to GND .....-0.3V to +5.5V
AVDD, OVDD to GND .....-0.3V to +2.1V
V_{CC5} - V_{CC3} to GND ..... > -0.3V
V_{REF}, GC+/- to GND .....-0.3 to (V_{CC3} + 0.3V)
CI+/-, CQ+/- to GND .....-0.3V to +13V
AG, LO+/- to GND .....-0.3 to (V_{CC5} + 0.3V)
INB_ Current .....±20mA DC
REFIO, CLKIN+/-, LOON to GND ..... -0.3V to the lower of (V_{AVDD} + 0.3V) and 2.1V
OUT+/-, SDIO, SCLK, CS, CLKOUT+/-, FRAME+/-, SHDN, CWD to GND -0.3V to the lower of (V_{OVDD} + 0.3V) and 2.1V
TVDD, TVCC to GND .....-0.3V to +5.6V
TVEE to GND .....-5.6V to +0.3V
TVNNA, TVNNB to GND .....-110V to +0.3V
TVPPA, TVPPB to GND .....-0.3V to +110V
TR_ Output Voltage Range .....$V_{TVNN\_}$ to $V_{TVPP\_}$
TINP_, TINN_, TCC_, TSYNC, TEN, THP to GND .....-0.3V to +5.6V
TMODE_, TCLK+, TCLK-, to GND..... -0.3V to (V_{TVCC} + 0.3V)
TVGPA, TVGPB to GND .....max[($V_{TVPP\_}$ - 5.6V), (V_{TVEE} + 0.6V)] to ($V_{TVPP\_}$ + 0.3V)
TVGNA, TVGNB to GND..... ($V_{TVNN\_}$ – 0.3V) to min [(V_{TVCC} + 0.6V), ($V_{TVNN\_}$ + 5.6V)]
TVPP, TVNN, CI+/-, CQ+/-, V_{CC5}, TVCC, TVEE, TVDD, V_{CC3}, AVDD/OVDD, V_{REF}, analog and digital control signals must be applied in this order
Continuous Current (INGP_, INGN_).....±100mA
Continuous Power Dissipation (T_A = +70°C)
CSBGA (derate 28.6mW/°C above +70°C).....3500mW
Operating Ambient Temperature Range (Note 1) ..0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C

Note 1: T_C is the temperature on the bump of the package. T_A is the ambient temperature of the device and PCB.

Package Thermal Characteristics (Note 2)

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....23°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5.2°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Octal Ultrasound Front-End Specifications

DC Electrical Characteristics—T/R Switch and Transmitter

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES (TVDD, TVCC, TVEE, TVPP_, TVNN_)						
Logic Supply Voltage	V_{TVDD}		1.7	3	5.25	V
Positive Drive Supply Voltage	V_{TVCC}		4.9	5	5.1	V
Negative Drive Supply Voltage	V_{TVEE}		-5.1	-5	-4.9	V
High-Side Supply Voltage	$V_{TVPP\_}$		0		+105	V
Low-Side Supply Voltage	$V_{TVNN\_}$		-105		0	V
External Floating Power-Supply Current from $TV_{GN\_}$	$I_{TVGN\_}$	TEN = high (Note 4), V_{TVGN} - V_{TVNN} = +5V		14		mA
External Floating Power-Supply Current from $TV_{GP\_}$	$I_{TVGP\_}$	TEN = high (Note 4) V_{TVPP} - V_{TVGP} = +5V		18		mA

DC Electrical Characteristics—T/R Switch and Transmitter (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS/OUTPUTS (TINN_, TINP_, TMODE_, TSYNC, TCC_, TEN)						
Low-Level Input Threshold	V_{IL}				0.2 x V_{TVDD}	V
High-Level Input Threshold	V_{IH}		0.8 x V_{TVDD}			V
Logic-Input Capacitance	C_{IN}			5		pF
Logic-Input Leakage (All Inputs Except TEN)	I_{IN}	V_{IN} = 0V or V_{TVDD}	-1	0	+1	µA
TEN Pulldown Resistance	R_{TEN}		6.7	10	14	kΩ
THP Low-Level Output Voltage	V_{OL}	Pullup resistor to TVDD (R_{PULLUP} = 1kΩ)			0.1 x V_{TVDD}	V
CLOCK INPUTS (TCLK+, TCLK-)—DIFFERENTIAL MODE						
Differential Clock Input Voltage Range	V_{TCLKD}		0.2		2	V_{P-P}
Common-Mode Voltage	V_{TCLKCM}			V_{TVCC}/2		V
Common-Mode Voltage Range	V_{CL}		V_{TVCC}/2 - 0.45		V_{TVCC}/2 + 0.45	V
Input Resistance	R_{TCLK+}, R_{TCLK-}	Differential		6.7		kΩ
		Common mode		21.5		kΩ
Input Capacitance	C_{TCLK+}, C_{TCLK-}	Capacitance to GND (each input)		5		pF
CLOCK INPUTS (TCLK+, TCLK-)—SINGLE-ENDED MODE (VTCLK- < 0.1V)						
Low-Level Input	V_{IL}	TCLK+			0.2 x V_{TVDD}	V
High-Level Input	V_{IH}	TCLK+	0.8 x V_{TVDD}			V
Single-Ended Mode Selection Threshold Low	V_{IL}	TCLK-			0.1	V
Single-Ended Mode Selection Threshold High	V_{IH}	TCLK-	1			V
Input Capacitance (TCLK_)	$C_{TCLK\_}$			5		pF
Logic-Input Leakage (TCLK+)	I_{TCLK+}	V_{TCLK+} = 0V or V_{TVDD}	-1	0	+1	µA
Pullup Current (TCLK-)	I_{TCLK-}	V_{TCLK-} = 0V		120	180	µA

DC Electrical Characteristics—T/R Switch and Transmitter (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY CURRENT—SHUTDOWN MODE (TMODE0 = Low, TMODE1 = Low)							
TVDD Supply Current	I_{TVDD}	All inputs connected to GND or TVDD				3	µA
TVCC Supply Current	I_{TVCC}	All inputs connected to GND or TVDD				22	µA
TVEE Supply Current	I_{TVEE}	All inputs connected to GND or TVDD				13	µA
TVPP_ Supply Current	$I_{TVPP\_}$	All inputs connected to GND or TVDD				10	µA
TVNN_ Supply Current	$I_{TVNN\_}$	All inputs connected to GND or TVDD				10	µA
SUPPLY CURRENT—DISABLE MODE (TMODE0 = High, TMODE1 = High)							
TVDD Supply Current	I_{TVDDQ}	All inputs connected to GND or TVDD	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{TCLKD} = 0.2V		110	190	
TVEE Supply Current	I_{TVEEQ}	TINN_ = TINP_ = GND			0.27	0.4	mA
		TINN_ = TINP_ = V_{TVDD}			9.9	13.3	
TVCC Supply Current	I_{TVCCQ}	TINN_ = TINP_ = GND			0.5	0.75	mA
		TINN_ = TINP_ = V_{TVDD}			10.1	13.6	
TVCC Supply Current Increase in Clocked Mode	ΔI_{TVCC}	Differential clock mode			3.5	5	mA
TVNN_ Total Supply Current (Quiescent Mode)	$I_{TVNNQ\_}$	All inputs connected to GND or TVDD			200	305	µA
TVPP_ Total Supply Current (Quiescent Mode)	$I_{TVPPQ\_}$	All inputs connected to GND or TVDD			220	340	µA
Total Power Dissipation per Channel (Disable Mode)	P_{PDIS1}	T/R switch off, damp off (transparent mode)			5.7		mW
	P_{PDIS2}	TINN_ = TINP_ = V_{TVDD}			17.8		

DC Electrical Characteristics—T/R Switch and Transmitter (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY CURRENT—OCTAL THREE-LEVEL MODE, NO LOAD (TMODE0 = High, TMODE1 = Low)							
TVDD Supply Current (Quiescent Mode)	I_{TVDD}	All inputs connected to GND or TVDD	Transparent or single-ended clock mode		1.7	3	µA
			Differential clock mode, V_{TCLKD} = 0.2V		110	190	
TVEE Supply Current (Quiescent Mode)	I_{TVEEQ}	TINN_ = TINP_ = GND			0.27	0.4	mA
		TINN_ = TINP_ = V_{TVDD}			9.9	13.3	
TVCC Supply Current (Quiescent Mode)	I_{TVCCQ}	TINN_ = TINP_ = GND			0.5	0.75	mA
		TINN_ = TINP_ = V_{TVDD}			10.1	13.6	
TVCC Supply Current Increase in Clocked Mode	ΔI_{TVCC}	Differential clock mode			3.5	5	mA
TVNN_ Total Supply Current (Quiescent Mode)	$I_{TVNNQ\_}$	All inputs connected to GND or TVDD			200	305	µA
TVPP_ Total Supply Current (Quiescent Mode)	$I_{TVPPQ\_}$	All inputs connected to GND or TVDD			220	340	µA
Total Power Dissipation per Channel (Quiescent Mode)	P_{PDIS1}	T/R switch off, damp off (transparent mode)			5.7		mW
	P_{PDIS2}	TINN_ = TINP_ = V_{TVDD} (transparent mode)			17.8		
TVDD Supply Current	I_{TVDD1}	CW Doppler (Note 5), transparent or single-ended clock mode			2.2	3.3	mA
	I_{TVDD2}	B mode (Note 6), transparent or single-ended clock mode, Figure 2			10	20	µA
TVEE Supply Current	I_{TVEE1}	8 channels switching, CW Doppler (Note 5), TCC0 = high, TCC1 = high			65	92	mA
	I_{TVEE2}	8 channels switching, B mode (Note 6), Figure 2, TCC0 = low, TCC1 = low			10.3	15.2	

DC Electrical Characteristics—T/R Switch and Transmitter (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TVCC Supply Current	I_{TVTCC1}	8 channels switching, CW Doppler (Note 5), TCC0 = high, TCC1 = high		45	60	mA
	I_{TVCC2}	8 channels switching, B mode (Note 6), Figure 2, TCC0 = low, TCC1 = low		10.5	15.4	
TVDD Supply Current Increase in Clocked Mode	ΔI_{TVDD}	Differential clock mode		1.8		mA
TVCC Supply Current Increase in Clocked Mode	ΔI_{TVCC}	Differential clock mode		3.8		mA
TVNN_ Supply Current	I_{TVNN1}	8 channels switching, CW Doppler (Note 5) TCC0 = high, TCC1 = high, R_L = 1kΩ, C_L = 200pF		157	200	mA
	I_{TVNN2}	8 channels switching, B mode (Note 7), Figure 2, TCC0 = low, TCC1 = low, R_L = 1kΩ, C_L = 200pF		1.7	2.8	
TVPP_ Supply Current	I_{TVPP1}	8 channels switching, CW Doppler (Note 5) TCC0 = high, TCC1 = high, R_L = 1kΩ, C_L = 200pF		186	230	mA
	I_{TVPP2}	8 channels switching, B mode (Note 6), Figure 2, TCC0 = low, TCC1 = low, R_L = 1kΩ, C_L = 200pF		2.7	4.5	
Power Dissipation per Channel (Octal Three-Level Mode)	PD_{CW}	1 channel switching, CW Doppler (Note 5)		285		mW
	PD_{PW}	1 channels switching, B mode (Note 6), Figure 2, TCC0 = low, TCC1 = low, R_L = 1kΩ, C_L = 200pF		68		
SUPPLY CURRENT—OCTAL THREE-LEVEL MODE, NO LOAD (TMODE0 = High, TMODE1 = Low, TEN = High, $V_{TVPP\_}$ - $V_{TVGP\_}$ = +5V, $V_{TVGN\_}$ - $V_{TVNN\_}$ = +5V)						
TVEE Supply Current (Quiescent Mode)	$I_{TVEEQ\_}$			25		µA
TVCC Supply Current (Quiescent Mode)	$I_{TVCCQ\_}$	All inputs connected to GND		280		µA

DC Electrical Characteristics—T/R Switch and Transmitter (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TVNN_ Supply Current (Quiescent Mode)	$I_{TVNNQ\_}$	All inputs connected to GND			40		µA
TVPP_ Supply Current (Quiescent Mode)	$I_{TVPPQ\_}$	All inputs connected to GND			40		µA
OUTPUT STAGE							
TVNNA, TVNNB Connected Low-Side Output Impedance	R_{OLS}	$I_{OUT\_}$ = -50mA	TCC0 = low, TCC1 = low		8.5		Ω
			TCC0 = high, TCC1 = low		10		
			TCC0 = low, TCC1 = high		13.5		
			TCC0 = high, TCC1 = high		26	46	
TVPPA, TVPPB Connected High-Side Output Impedance	R_{OHS}	$I_{OUT\_}$ = +50mA	TCC0 = low, TCC1 = low		9		Ω
			TCC0 = high, TCC1 = low		10.5		
			TCC0 = low, TCC1 = high		14.5		
			TCC0 = high, TCC1 = high		27	52	
Clamp nFET Output Impedance	R_{ONG}	$I_{OUT\_}$ = -50mA,			13.5		Ω
Clamp pFET Output Impedance	R_{OPG}	$I_{OUT\_}$ = +50mA			13.5		Ω
Active Damp Output Impedance	R_{DAMP}	Before grass-clipping diode			500		Ω
TVNNA, TVNNB Connected Low-Side Output Current	I_{OLS}	V_{DS} = 100V	TCC0 = low, TCC1 = low		2.0		A
			TCC0 = high, TCC1 = low		1.5		
			TCC0 = low, TCC1 = high		1.0		
			TCC0 = high, TCC1 = high		0.5		

DC Electrical Characteristics—T/R Switch and Transmitter (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TVPPA, TVPPB Connected High-Side Output Current	I_{OHS}	V_{DS} = 100V	TCC0 = low, TCC1 = low		2.0		A
			TCC0 = high, TCC1 = low		1.5		
			TCC0 = low, TCC1 = high		1.0		
			TCC0 = high, TCC1 = high		0.5		
GND-Connected nFET Output Current	I_{ONG}	V_{DS} = 100V			1		A
GND-Connected pFET Output Current	I_{OPG}	V_{DS} = 100V			1		A
Diode Voltage Drop (Blocking Diode and Grass-Clipping Diode)	V_{DROP}	$I_{OUT\_}$ = ±50mA			1.7		V
Grass-Clipping Diode Reverse Capacitance	C_{REV}				2.5		pF
TR_ Equivalent Large-Signal Shunt Capacitance	C_{HS}	200V_{P-P} signal			80		pF
T/R Switch On-Impedance	R_{ON}	f = 5MHz,V_{TR} = 0V			11.5		Ω
T/R Switch Off-Impedance	R_{OFF}				1		MΩ
T/R Switch Output Offset	TR_{OFF}	INB_, TR_ unconnected, V_{TVCC} = +5V, V_{TVEE} = -5V		-40		+40	mV
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold	t_{SDN}	Temperature rising			+145		C
Thermal-Shutdown Hysteresis	t_{HYS}				20		C

AC Electrical Characteristics—T/R Switch and Transmitter

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0, TCC0 = 0, TCC1 = 0, RL = 1kΩ, C_L = 200pF, unless otherwise noted. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Input to Output Rise Propagation Delay	t_{PLH}	From 50% TINP_/TINN_ (transparent mode) to 10% OUT_ transition swing, Figure 3		18		ns
Logic Input to Output Fall Propagation Delay	t_{PHL}	From 50% TINP_/TINN_ (transparent mode) to 10% OUT_ transition swing, Figure 3		18		ns
Logic Input to Output Rise to GND Propagation Delay	t_{PL0}	From 50% TINP_/TINN_ (transparent mode) to 10% OUT_ transition swing, Figure 3		18		ns
Logic Input to Output Fall to GND Propagation Delay	t_{PH0}	From 50% TINP_/TINN_ (transparent mode) to 10% OUT_ transition swing, Figure 3		18		ns
TR_ Fall Time (V_{TVPPA} to V_{TVNNA}, V_{TVPPB} to V_{TVNNB})	t_{FPN}	Figure 4		30		ns
TR_ Rise Time (V_{TVNNA} to V_{TVPPA}, V_{TVNNB} to V_{TVPPB})	t_{RNP}	Figure 4		30		ns
TR_ Rise Time (GND to V_{TVPPA}, GND to V_{TVPPB})	t_{R0P}	Figure 4		15		ns
TR_ Fall Time (GND to V_{TVNNA}, GND to V_{TVNNB})	t_{F0N}	Figure 4		15		ns
TR_ Rise Time (V_{TVNNA} to GND, V_{TVNNB} to GND)	t_{RN0}	Figure 4		21		ns
TR_ Fall Time (V_{TVPPA} to GND, V_{TVPPB} to GND)	t_{FP0}	Figure 4		21		ns
T/R Switch Turn-On Time	t_{ONTRSW}	Figure 5		0.65	1.2	µs
T/R Switch Turn-Off Time	$t_{OFFTRSW}$	Figure 5 (Note 8)		0.02	0.1	µs
Output Enable Time (Shutdown Mode to Normal Operation)	t_{EN1}				100	µs
Output Disable Time (Normal Operation to Shutdown Mode)	t_{DIS1}				10	µs
Output Enable Time (Transmit Disable Mode to Normal Operation)	t_{EN2}				52	ns
Output Disable Time (Normal Operation to Transmit Disable Mode)	t_{DIS2}				65	ns

AC Electrical Characteristics—T/R Switch and Transmitter (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{TVDD} = 3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{GND} = 0V, SHDN = 0, R_{IN} = 200Ω, high LNA gain. T_A = 0°C to +70°C. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_, TEN = 0. Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Enable Time (Normal Operation to Sync Mode)	t_{EN3}				4	µs
Output Disable Time (Sync Mode to Normal Operation)	t_{DIS3}				500	ns
TCLK_ Frequency	$f_{TCLK\_}$	V_{TVDD} = 2.5V			200	MHz
Input Setup Time (TINN_, TINP_)	t_{SETUP}	V_{TVDD} = 2.5V			2	ns
Input Hold Time (TINN_, TINP_)	t_{HOLD}	V_{TVDD} = 2.5V			0.8	ns
Second-Harmonic Distortion (Low Voltage)	THD2LV	$f_{OUT\_}$ = 5MHz, V_{TVPPA} = $-V_{TVNNA}$ = +5V, V_{TVPPB} = $-V_{TVNNB}$ = +5V, square wave (all modes)		-40		dBc
Second-Harmonic Distortion (High Voltage)	THD2HV	$f_{OUT\_}$ = 5MHz, V_{TVPPA} = $-V_{TVNNA}$ = +100V, V_{TVPPB} = $-V_{TVNNB}$ = +100V, square wave (all modes)		-43		dBc
Pulse Cancellation	PC1	$f_{OUT\_}$ = 5MHz, V_{TVPPA} = $-V_{TVNNA}$ = +100V, V_{TVPPB} = $-V_{TVNNB}$ = +100V, 2 periods, all harmonics of the summed signed with respect to the carrier		-40		dBc
	PC2	$f_{OUT\_}$ = 5MHz, V_{TVPPA} = $-V_{TVNNA}$ = +100V, V_{TVPPB} = $-V_{TVNNB}$ = +100V, 2 periods, $[(V_0 + V_{180})_{RMS}/(2 \times V_{0RMS})]_{db}$		-40		
Pulser Bandwidth	BW	V_{TVPPA} = +60V, V_{TVNNA} = -60V, Figure 6		20		MHz
RMS Output Jitter	t_J	$f_{OUT\_}$ = 5MHz, V_{TVPPA} = $-V_{TVNNA}$ = +5V, V_{TVPPB} = $-V_{TVNNB}$ = +5V, both in clocked mode or transparent mode, Figure 7		6.25		ps
T/R Switch Harmonic Distortion	THD_{TRSW}	R_{LOAD} = 200Ω, V_{SIGNAL} = $100mV_{P-P}$		-50		dB
T/R Switch Turn-On/Off Voltage Spike	V_{SPIKE}	R_{LOAD} = 1kΩ at both sides of T/R switch		50		mV
Crosstalk	CT	f = 5MHz, adjacent channels, $R_{IB\_\_}$ = 200Ω		-51		dB

DC Electrical Characteristics—LNA, VGA, ADC (CWD Beamformer Off)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, V_{GND} = 0V, T_A = 0°C to +70°C, SHDN = 0, CWD = 0, LOON = 0, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage	V_{CC3}	V_{CC3} pins	3.13	3.3	3.47	V
5V Supply Voltage	V_{CC5}	V_{CC5} pins	4.5	4.75	5.25	V
1.8V Supply Voltage	$V_{TCC1.8}$	AVDD and OVDD pins	1.7	1.8	1.9	V
External Reference Voltage Range	V_{REF}	(Note 9)	2.475		2.525	V
External Reference Current		Total current into the V_{REF} pin		5		µA
3V Supply Current Per Channel	I_{CC3}	Total I divided by 8, V_{GC+} - V_{GC-} = -0.4V		9.5	16	mA
11V Supply Current Per Channel	I_{CC11}	Total I divided by 8		0		mA
5V Supply Current Per Channel	I_{CC5}	Total I divided by 8		6.4	9	mA
1.8V Supply Current Per Channel	$I_{TCC1.8}$	Total I divided by 8, AVDD + OVDD		32	37.9	mA
		Total I divided by 8, AVDD		20	22.8	mA
		Total I divided by 8, OVDD		12	15.1	mA
DC Power Per Channel	P_NM	V_{GC+} - V_{GC-} = -0.4V		131		mW
Differential Analog Control Voltage Range	VGAIN_RANG	V_{GC+} - V_{GC-}		±3		V
5V Supply Nap Current	$I_{\_NP\_5V\_TOT}$	SHDN = 1, nap mode (all 8 channels)		30		mA
3V Supply Nap Current	$I_{\_NP\_3V\_TOT}$	SHDN = 1, nap mode (all 8 channels)		0.035		mA
1.8V Supply Nap Current		SHDN = 1, nap mode (all 8 channels)		40		mA
5V Supply Power-Down Current	$I_{\_PD\_5V\_TOT}$	SHDN = 1, power-down mode (all 8 channels)		1		µA
3V Supply Power-Down Current	$I_{\_PD\_3V\_TOT}$	SHDN = 1, power-down mode (all 8 channels)		1		µA
1.8V Supply Power-Down Current		SHDN = 1, power-down mode (all 8 channels)		0.38		mA
Common-Mode Voltage for Differential Analog Control	V_{GAIN_COMM}	(V_{GC+} - V_{GC-})/2		1.65 ±5%		V
Source/Sink Current for Gain Control Pins	$I_{\_GC\_}$	Per pin		±1.6		µA

AC Electrical Characteristics—VGA MODE (CWD Beamformer Off)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Resolution					12		Bits
Minimum ADC Sample Rate					25		Msps
Maximum ADC Sample Rate				50			Msps
Mode-Select Response Time (Note 7)		CWD stepped from 0 to 1, DC stable within 10%			1		µs
		CWD stepped from 1 to 0, DC stable within 10%			1		
Input Impedance		50Ω mode, f_{RF} = 2MHz			50		Ω
		100Ω mode, f_{RF} = 2MHz			100		
		200Ω mode, f_{RF} = 2MHz			200		
		500Ω mode, f_{RF} = 2MHz			500		
Noise Figure (High LNA Gain)		R_S = R_{IN} = 50Ω, V_{GC+} - V_{GC-} = +3V	Not including T/R switch		5.4		dB
			With T/R switch		6.5		
		R_S = R_{IN} = 100Ω, V_{GC+} - V_{GC-} = +3V	Not including T/R switch		3.9		
			With T/R switch		5.0		
		R_S = R_{IN} = 200Ω, V_{GC+} - V_{GC-} = +3V	Not including T/R switch		2.8		
			With T/R switch		3.7		
		R_S = R_{IN} = 500Ω, V_{GC+} - V_{GC-} = +3V	Not including T/R switch		2.1		
			With T/R switch		3.5		
Noise Figure (Low LNA Gain)		R_S = R_{IN} = 200Ω, V_{GC+} - V_{GC-} = +3V	Not including T/R switch		4.4		dB
			With T/R switch		5.2		
8-Channel Correlated Noise Power		No input signal, ratio of 8-channel noise power to single-channel noise power			9.0		dBFS
		5MHz signal applied to all 8 channels, V_{GC+} - V_{GC-} = 0V, f_{RF} = 5MHz at -3dBFS, ratio of 8-channel noise power to single-channel noise power			8.5		

AC Electrical Characteristics—VGA MODE (CWD Beamformer Off) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LNA Gain (Low LNA Gain)				12.5		dB
LNA Gain (High LNA Gain)				18.5		dB
Maximum Gain (High LNA Gain)		V_{GC+} - V_{GC-}= +3V (max gain), T/R switch input to ADC Input		44.3		dB
Minimum Gain (High LNA Gain)		V_{GC+} - V_{GC-} = -3V (min gain), T/R switch input to ADC Input		4.9		dB
Maximum Gain (Low LNA Gain)		V_{GC+} - V_{GC-} = +3V (max gain), T/R switch input to ADC Input		39.4		dB
Minimum Gain (Low LNA Gain)		V_{GC+} - V_{GC-} = = -3V (min gain), T/R switch input to ADC input		0.03		dB
Gain Range				39		dB
AA Filter 3dB Corner Frequency		9MHz setting		9		MHz
		10MHz setting		10		
		15MHz setting		15		
		18MHz setting		18		
AA Filter 3dB Corner Frequency Accuracy				±10		%
Digital Highpass Filter 3dB Corner Frequency		2 poles, coefficients R1 = R2 = 63/64, f_{CLK} = 50Msps		0.185		MHz
		2 poles, coefficients R1 = R2 = 54/64, f_{CLK} = 50Msps		1.736		
Clamp Level		Clamp on (V_{P-P} on AAF Output/ADC Input, digital HPF bypassed)		92		%FS
Absolute Gain Matching		T_A = +25°C, V_{GC+} - V_{GC-} = -3V to +3V (Note 10)	-1.6	±0.5	+1.6	dB
Input Gain Compression		LNA = high gain, V_{GC+} - V_{GC-} = -3V (VGA = min gain), gain ratio with 330mV_{P-P}/50mV_{P-P} input tones		0.5		dB
		LNA = low gain, V_{GC+} - V_{GC-} = -3V (VGA = min gain), gain ratio with 600mV_{P-P}/50mV_{P-P} input tones		0.7		

AC Electrical Characteristics—VGA MODE (CWD Beamformer Off) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VGA Gain Response Time		Gain step up (V_{IN} = 5mV_{P-P}, V_{GC+} - V_{GC-} changed from -3V to +3V, settling time is measured within 1dB final value)		0.8		µs
		Gain step down (V_{IN} = 5mV_{P-P}, V_{GC+} - V_{GC-} changed from +3V to -3V, settling time is measured within 1dB final value)		1.8		
VGA Output Offset Under Pulsed Overload		Over drive is ±10mA in clamping diodes, V_{GC+} - V_{GC-} = 1.0V (gain = 30dB), 16 pulses at 5MHz, repetition rate 20kHz; offset is measured at output when RF duty cycle is off		< 3.3		%FS
Signal-to-Noise Over ADC Nyquist Band (25MHz)		$V_{OUT\_}$ = -1dBFS, V_{IN} = 200mV_{P-P}, f_{RF} = 5MHz at -1dBFS, anti-alias filter = 9MHz, 50Msps sample rate		67		dBFS
Signal-to-Noise Over 2MHz Bandwidth		V_{GC+} - V_{GC-} = -1.0V (gain = 16dB), $V_{OUT\_}$ = -1dBFS, V_{IN} = 200mV_{P-P}, f_{RF} = 5MHz at -1dBFS, anti-alias filter = 9MHz, 50Msps sample rate		76		dBFS
Near-Carrier Signal-to-Noise Ratio		V_{GC+} - V_{GC-} = 0V (gain = 22dB), f_{RF} = 5.3MHz at -1dBFS, measured at 1kHz from f_{RF}, 50Msps sample rate		-137		dBFS/Hz
Second Harmonic (HD2)		V_{IN} = 50mV_{P-P}, f_{RF} = 2MHz, ADC out = -3dBFS		-67		dBc
		V_{IN} = 50mV_{P-P}, f_{RF} = 5MHz, ADC out = -3dBFS		-63		
IM3 Distortion		V_{IN}= 50mV_{P-P}, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz ADC out = -3dBFS (Note 11)		-49		dBc
Nap Mode Power-Up Response Time		V_{GC+} - V_{GC-}= 0.6V (gain = 28dB), f_{RF} = 5MHz, ADC out = -3dBFS, settled with in 1dB from transition on SHDN pin (includes ADC)		2		µs
Nap Mode Power-Down Response Time		To reach DC current target ±10%, on V_{CC5}, V_{CC3}, AVDD, OVDD from transition on SHDN pin		4		µs

AC Electrical Characteristics—VGA MODE (CWD Beamformer Off) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sleep Mode Power-Up Response Time		V_{GC+} - V_{GC-}= 0.6V (gain = 28dB), f_{RF} = 5MHz, $V_{OUT\_}$ = -1dBFS, settled within 1dB from transition on SHDN		2		ms
Sleep Mode Power-Down Response Time		V_{GC+} - V_{GC-}= 0.6V (gain = 28dB), f_{RF} = 5MHz, DC power reaches 1mW/channel, from transition on SHDN (includes ADC)		4		ms
Adjacent-Channel Crosstalk		$V_{OUT\_}$ = -3dBFS, f_{RF} = 5MHz, V_{GC+} - V_{GC-} = 0.6V (gain = 28dB)		-59		dBc
Alternate-Channel Crosstalk		$V_{OUT\_}$ = -3dBFS, f_{RF} = 5MHz, V_{GC+} - V_{GC-} = 0.6V (gain = 28dB)		-75		dBc
Phase Matching Between Channels		V_{GC+} - V_{GC-} = 0.6V (gain = 28dB), f_{RF} = 5MHz, $V_{OUT\_}$ = -3dBFS		±1.2		Degrees

DC Electrical Characteristics—CWD MODE (VGA, AAF, and ADC Off)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 1, LOON = 1, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, R_{IN} = 200Ω, CI+, CI-, CQ+, CQ- pulled up to +11V via four separate 0.1% 120Ω resistors. No RF signals applied, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Mixer LVDS LO Input Common-Mode Voltage	V_LVDS_CM	Pins LO+ and LO-		1.25 ± 0.2		V
LVDS LO Differential Input Voltage	V_LVDS_DM	Common-mode input voltage = 1.25V (Note 12)	200	700		mV_{P-P}
LVDS LO Input Common-Mode Current	I_LVDS_CM	Input bias current, common-mode input voltage = 1.25V (Note 12)		160		µA
LVDS LO Differential Input Resistance	R_LVDS_DM	(Note 13)		8		kΩ
FULL-POWER MODE						
5V Supply Current Per Channel	I_C_5V_F	Total I divided by 8		31.6	41	mA
3.3V Supply Current Per Channel	I_C_3_3V_F	Total I divided by 8		1.8	3	mA

DC Electrical Characteristics—CWD MODE (VGA, AAF, and ADC Off) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 1, LOON = 1, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, R_{IN} = 200Ω, CI+, CI-, CQ+, CQ- pulled up to +11V via four separate 0.1% 120Ω resistors. No RF signals applied, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8V Supply Current Per Channel	I_C_1_8V_F	Total I divided by 8, AVDD + OVDD		6.3		mA
11V Supply Current Per Channel	I_C_11V_F	Total I divided by 8		11.7	16.2	mA
External Reference Current		Total current into V_{REF} pin		70		µA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_F	(Note 14)		2.1		W
On-Chip Power Dissipation per Channel	PDIS_FP_F	(Note 14)		261		mW
LOW-POWER MODE						
5V Supply Current Per Channel	I_C_5V_L	Total I divided by 8		27	35	mA
3.3V Supply Current Per Channel	I_C_3_3V_L	Total I divided by 8		1.8	3	mA
1.8V Supply Current Per Channel	I_C_1_8V_L	Total I divided by 8, AVDD + OVDD		6.3		µA
11V Supply Current Per Channel	I_C_11V_L	Total I divided by 8		7		mA
External Reference Current	I_{REF}	Total Current into the V_{REF} pin		70		µA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_L	(Note 14)		1.7		W
On-Chip Power Dissipation per Channel	PDIS_FP_L	(Note 14)		214		mW

AC Electrical Characteristics—CWD MODE (VGA, AAF, and ADC Off)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, VA_{VDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, CWD = 1, SHDN = 0, LOON = 1, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, RIN = 200Ω, f_{RF} = 5MHz, high LNA Gain, CI+, CI-, CQ+, CQ- pulled up to +11V via four separate 0.1% 120Ω resistors. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. The rise/fall time of the LVDS clock driving LO+/LO- is required to be 0.5ns, reference noise less than 10nV/$\sqrt{Hz}$ from 1kHz to 20MHz (Note 15). Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CW DOPPER MIXER						
Mixer RF Frequency Range			0.9		7.6	MHz
LO Frequency Range			8.0		60	MHz
Mixer Output Frequency Range			DC		100	kHz

AC Electrical Characteristics—CWD MODE (VGA, AAF, and ADC Off) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, VA_{VDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, CWD = 1, SHDN = 0, LOON = 1, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, RIN = 200Ω, f_{RF} = 5MHz, high LNA Gain, CI+, CI-, CQ+, CQ- pulled up to +11V via four separate 0.1% 120Ω resistors. Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. The rise/fall time of the LVDS clock driving LO+/LO- is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz (Note 15). Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise specified.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FULL-POWER MODE							
Noise Figure		No carrier	Not including T/R switch		4.5		dB
			With T/R switch		4.7		
SNR at 100mV$_{P-P}$ Input		100mV$_{P-P}$ on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset			-144		dBc/Hz
SNR at 200mV$_{P-P}$ Input		200mV$_{P-P}$ on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset			-149		dBc/Hz
IM3 Distortion		V_{IN} = 100mV$_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, f_{LO} = 8 x 5MHz (Note 11)			-45		dBc
Mixer Output-Voltage Compliance		Valid voltage range (AC + DC) on summed mixer output pins (Note 16)		4.5		12	V
Channel-to-Channel Phase Matching		Measured under zero beat conditions. V_{IN} = 100mV$_{P-P}$, f_{RF} = 5MHz, f_{LO}/8 = 5MHz		-1	±0.5	+1	Degrees
Channel-to-Channel Gain Matching		Measured under zero beat conditions V_{IN} = 100mV$_{P-P}$, f_{RF} = 5MHz, f_{LO}/8 = 5MHz		-1	±0.5	+1	dB
Transconductance		f_{LO}/8 = 1.25MHz (Note 17)		20	23	27.5	mS
LOW-POWER MODE							
Noise Figure		No carrier	Not including T/R switch		4.4		dB
			With T/R switch		4.6		
SNR at 100mV$_{P-P}$ Input		100mV$_{P-P}$ on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset			-144		dBc/Hz
SNR at 200mV$_{P-P}$ Input		200mV$_{P-P}$ on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset			-148		dBc/Hz
IM3 Distortion		V_{IN} = 100mV$_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, f_{LO} = 8 x 5MHz (Note 11)			-44		dBc
Mixer Output-Voltage Compliance		Valid voltage range (AC+DC) on summed mixer output pins (Note 16)		4.5		12	V
Transconductance		f_{LO}/8 = 1.25MHz (Note 17)		19	21	26.5	mS

Electrical Characteristics——AFE Clock and Timing

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, f_{RF} = 5MHz, 50mV_{P-P}, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3, Note 18)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLKIN+, CLKIN-) DIFFERENTIAL MODE						
Differential Clock Input Voltage				0.4 to 2.0		V_{P-P}
Common-Mode Voltage	V_{CLKCM}	Self-biased		1.2		V
		DC-coupled clock signal		1.0 to 1.4		
Input Resistance	R_{CLK}	Differential, default setting		10		kΩ
		Differential, programmable internal termination selected		0.1		
		Common mode to GND		9		
Input Capacitance	C_{CLK}	Capacitance to GND, each input		3		pF
CLOCK INPUTS (CLKIN+, CLKIN-) SINGLE-ENDED MODE (CLKIN- < 0.1V)						
Single-Ended Mode-Selection Threshold (CLKIN-)					0.1	V
Single-Ended Clock Input High Threshold (CLKIN+)			1.5			V
Single-Ended Input Clock Low Threshold (CLKIN+)					0.3	V
Input Leakage (CLKIN+)		V_{IH} = 1.8V			+5	µA
		V_{IL} = 0V	-5			µA
Input Leakage (CLKIN-)		V_{IL} = 0V	-150		-50	µA
Input Capacitance (CLKIN+)				3		pF
DIGITAL INPUTS (CWD, LOON, SHDN, SCLK, SDIO, $\overline{CS}$)						
High-Level Input Threshold	V_{IH}		1.5			V
Low-Level Input Threshold	V_{IL}				0.3	V
Logic-Input Leakage	I_{IH}	V_{IH} = 1.8V			+5	µA
	I_{IL}	V_{IL} = 0V	-5			
Logic-Input Capacitance	C_{DIN}			3		pF
DIGITAL OUTPUTS (SDIO)						
High-Level Output Voltage	V_{OH}	I_{SOURCE} = -200µA	V_{OVDD} – 0.2			V
Low-Level Output Voltage	V_{OL}	I_{SINK} = 200µA			0.2	V
LVDS DIGITAL OUTPUTS (OUT_±, CLKOUT±, FRAME±) (I = 3.5mA, V_{CM} = 1.2V)						
Differential Output Voltage	$\lvert V_{OD} \rvert$	R_{LOAD} = 100Ω	225	300	490	mV
Output Offset Voltage	V_{OS}		1.125	1.200	1.375	V

Electrical Characteristics——AFE Clock and Timing (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, TMODE1 = 0, TMODE0 = 1, TCC1 = TCC0 = 0, THP = 1, TSYNC = 0, TEN = 0, TINP_ = TINN_ = 1, no TCLK_, f_{RF} = 5MHz, 50mV_{P-P}, Connect C = 1µF between TVPP_ to TVGP_ and TVNN_ to TVGN_. Typical values are at V_{TVDD} = 3.3V, V_{TVCC} = 5V, V_{TVEE} = -5V, $V_{TVNN\_}$ = -100V, $V_{TVPP\_}$ = 100V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3, Note 18)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-PORT INTERFACE TIMING						
SCLK Period	t_{SCLK}		50			ns
SCLK-to-$\overline{CS}$ Setup Time	t_{CSS}		10			ns
SCLK-to-$\overline{CS}$ Hold Time	t_{CSH}		10			ns
SDIO-to-SCLK Setup Time	t_{SDS}	Serial-data write	10			ns
SDIO-to-SCLK Hold Time	t_{SDH}	Serial-data write	0			ns
SCLK-to-SDIO Output Data Delay	t_{SDD}	Serial-data read			10	ns
LVDS DIGITAL OUTPUT TIMING CHARACTERISTICS						
Data Valid to CLKOUT_ Rise/Fall	t_{OD}		(t_{SAMPLE}/24) - 0.10	(t_{SAMPLE}/24) + 0.05	(t_{SAMPLE}/24) + 0.20	ns
CLKOUT_ Output-Width High	t_{CH}			t_{SAMPLE}/12		ns
CLKOUT_ Output-Width Low	t_{CL}			t_{SAMPLE}/12		ns
FRAME_ Rise to CLKOUT_ Rise	t_{DF}		(t_{SAMPLE}/24) - 0.10	(t_{SAMPLE}/24) + 0.05	(t_{SAMPLE}/24) + 0.20	ns
Sample CLKIN_ Rise to FRAME_ Rise	t_{SF}		(t_{SAMPLE}/2) + 1.6	(t_{SAMPLE}/24) + 2.3	(t_{SAMPLE}/24) + 3.3	ns
CWD LO TIMING						
LOON Setup Time	t_{SU}	Setup time from LOON high to LVDS LO clock low-to-high transition (Figure 1)	5			ns

Note 3: Minimum and maximum limits at T_A = +25°C and +70°C are guaranteed by design, characterization, and/or production test.

Note 4: Maximum operating current from $V_{TVGN\_}$ and $V_{TVGP\_}$ external power sources can vary depending on application requirements. The suggested typical values assume 8 channels running in continuous transmission (CWD) at 5MHz with TCC0 = TCC1 = high.

Note 5: CW Doppler: continuous wave, f = 5MHz, V_{DD} = +3V, V_{CC} = -V_{EE} = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = +5V.

Note 6: B mode: f = 5MHz, P_{RF} = 5kHz, 1 period, V_{DD} = +3V, V_{CC} = -V_{EE} = +5V, $V_{PP\_}$ = -$V_{NN\_}$ = +100V.

Note 7: This response time does not include the CW output highpass filter. When switching to VGA mode, the CW outputs stop drawing current and the output voltage goes to the rail. If a highpass filter is used, the recovery time may be excessive and a switching network is recommended.

Note 8: T/R switch turn-off time is the time required to switch off the bias current of the T/R switch. The off-isolation is not guaranteed.

Note 9: Noise performance of the device is dependent on the noise contribution from V_{REF}. Use a low-noise supply for V_{REF}.

Note 10: Absolute Gain Matching is defined as the gain difference between any single channel and the average of numerous channels across multiple devices. This specification is valid for all VGA gain settings for devices sharing the same control voltages V_{GC+}, V_{GC-}.

Note 11: See in the *Ultrasound-Specific IMD3 Specification* section.

Note 12: The LVDS CWD LO clocks are DC-coupled. See the *CWD Beamformer Programming and Clocking* section for details of LO startup synchronization.

Note 13: An external 100Ω resistor terminates the LVDS differential signal path (LO+, LO-).

Note 14: Total on-chip power dissipation is calculated as $P_{DISS} = V_{CC5} \times I_{CC5} + V_{CC3} \times I_{CC3} + V_{AVDD} \times I_{AVDD} + V_{OVDD} \times I_{OVDD} + V_{REF} \times I_{REF} + [11V - (I11V/4) \times 120] \times I11V + V_{TVCC} \times I_{TVCC} + V_{TVEE} \times I_{TVEE} + V_{TVDD} \times I_{TVDD}$. Additional power is dissipated through the off-chip, 120Ω load resistors.

Note 15: The reference input noise is given for 8 channels, knowing that the reference-noise contributions are correlated in all 8 channels. If more channels are used, the reference noise must be reduced to get the best noise performance.

Note 16: Mixer output-voltage compliance is the range of acceptable voltages allowed on the CW mixer outputs.

Note 17: Transconductance is defined as the differential output current at baseband for each individual (I or Q) mixer output, divided by the single-ended, RF input voltage directly on a single, T/R switch input pin (TRj). This can be calculated as $g_{mI} = (I_{CI+} - I_{CI-})/V_{TRj}$ and $gmQ = (I_{CQ+} - I_{CQ-})/VTRj$; or equivalently as $gmI = (V_{CI+} - V_{CI-})/(R_L \times VTRj)$ and $g_{mQ} = (I_{CQ+} - I_{CQ-})/(R_L \times VTRj)$ (where j = 1, 2,…8 is a specific channel number, TRj is a single T/R switch input pin, and R_L is the load resistance on each, individual mixer output pin).

Note 18: All currents are global. In particular, $I_{NN\_} = I_{TVNNA} + I_{TVNNB}$, $I_{PP\_} = I_{TVPPA} + I_{TVPPB}$.

Timing Diagrams

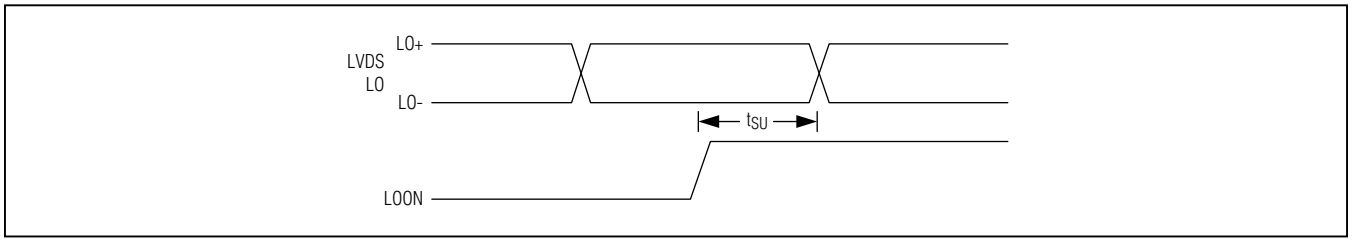


Figure 1. CWD LOON LO Turn-On/Turn-Off Setup Time

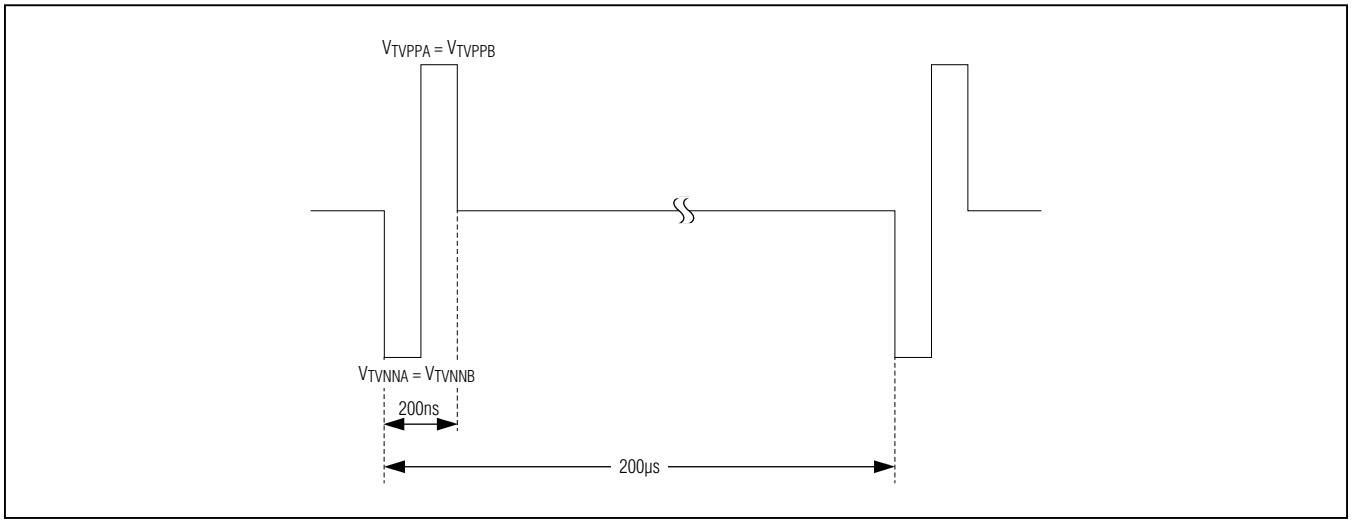


Figure 2. HV Burst Test (Three Levels)

Timing Diagrams (continued)

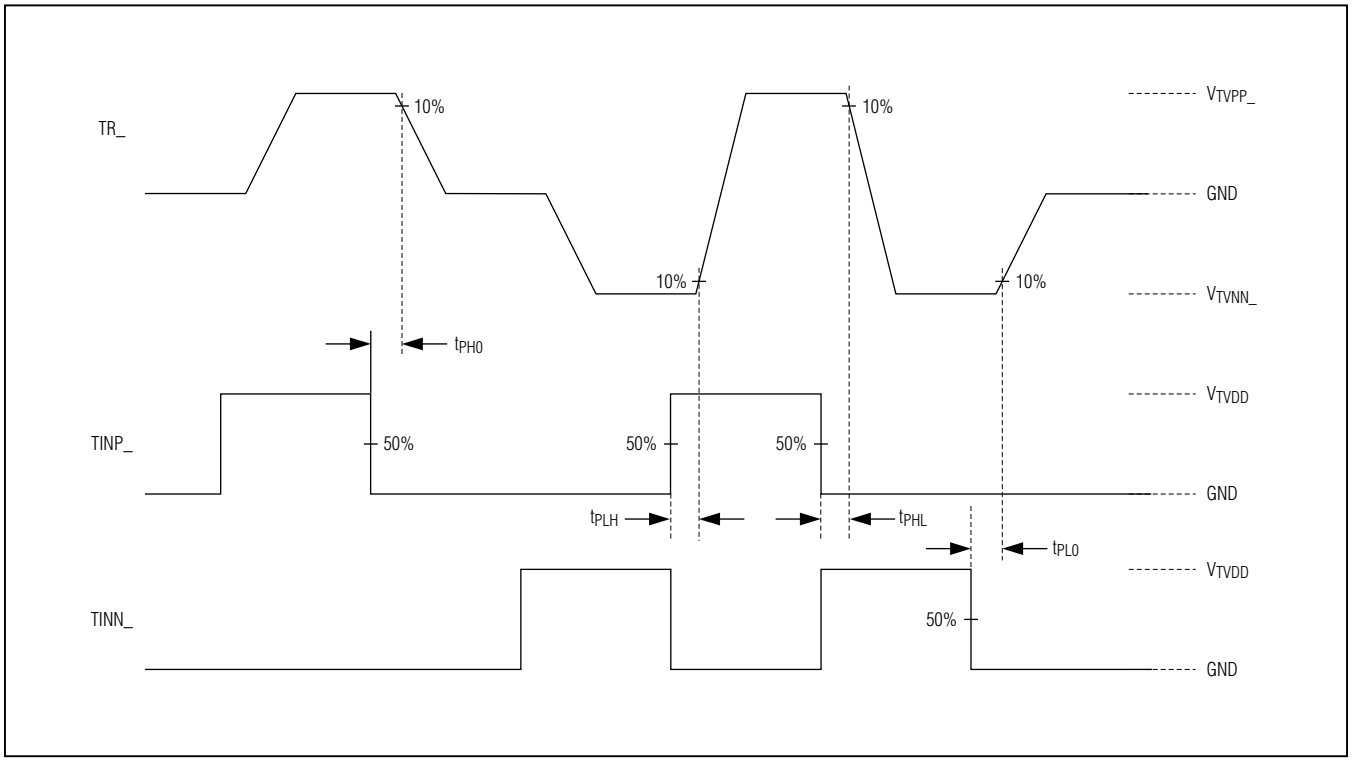


Figure 3. Propagation Delay Timing

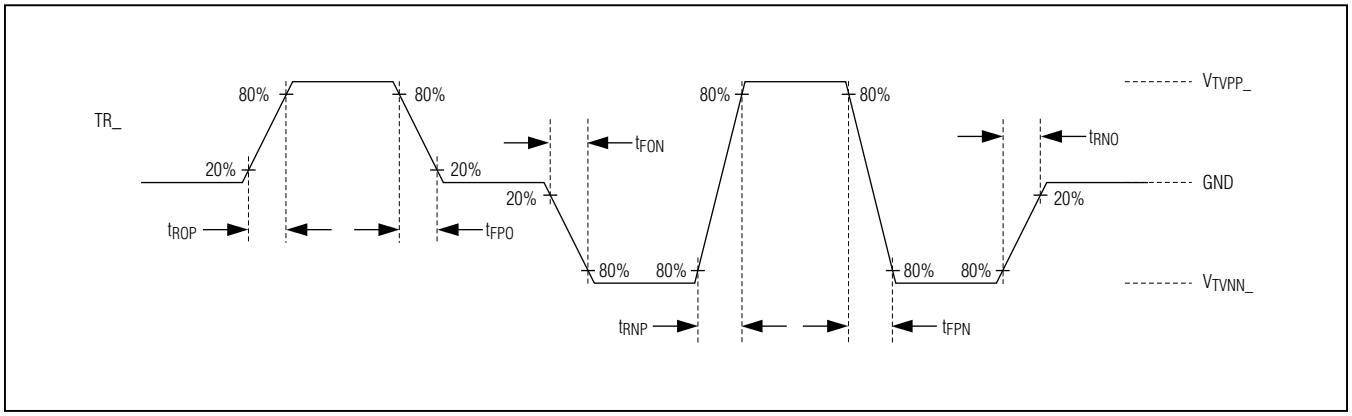


Figure 4. Output Rise/Fall Timing

Timing Diagrams (continued)

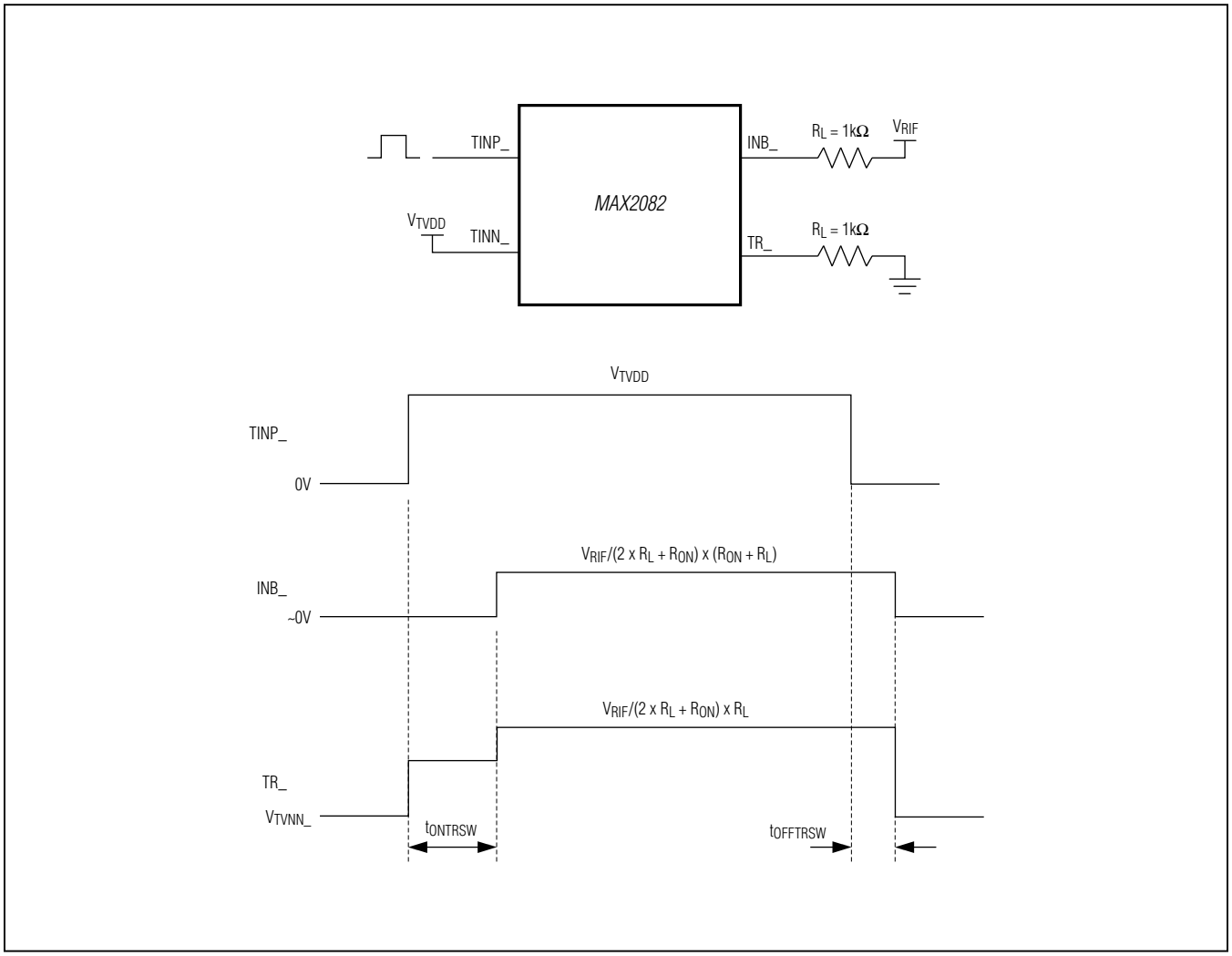


Figure 5. T/R Switch Turn-On/Off TIme

Timing Diagrams (continued)

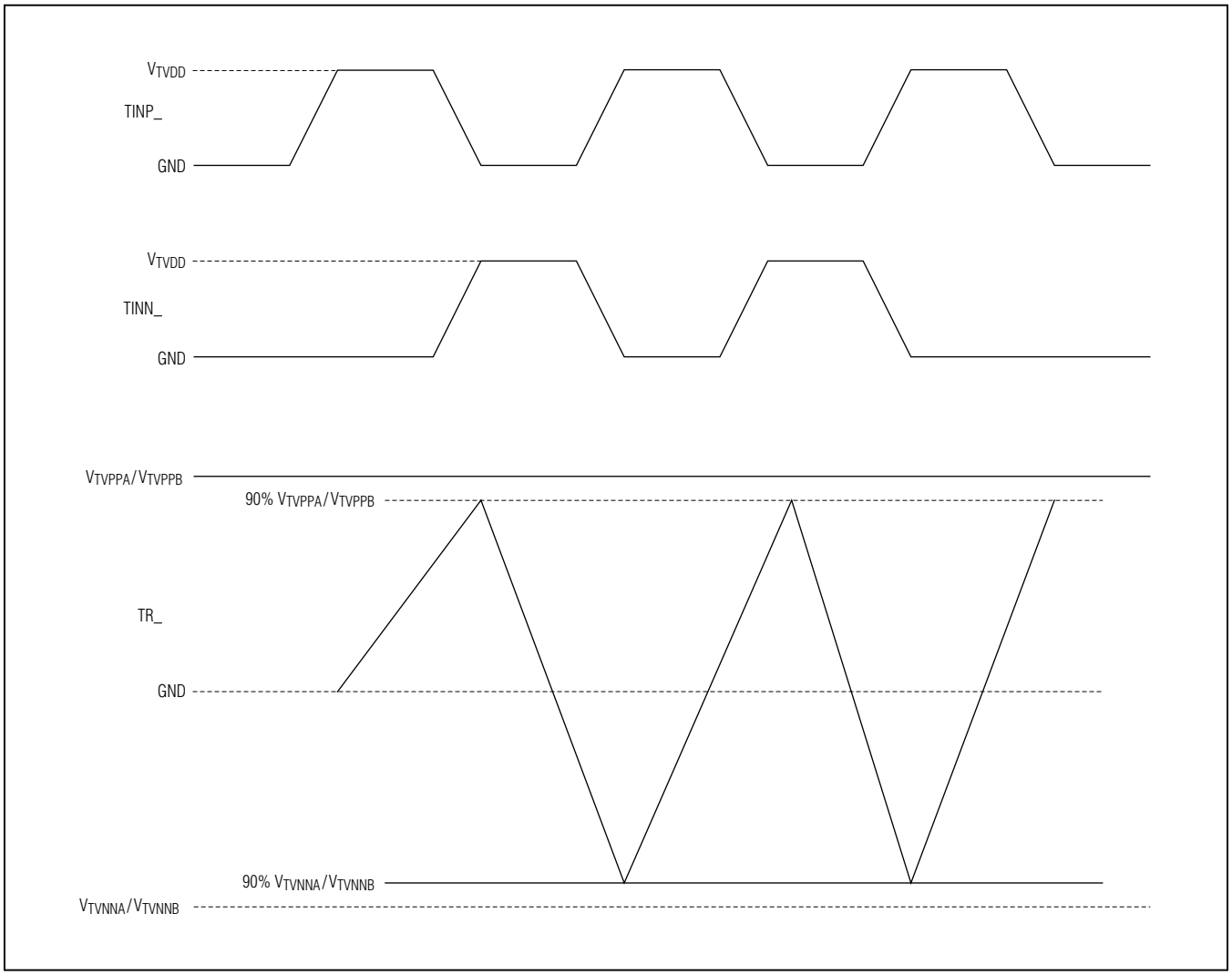


Figure 6. Bandwidth

Timing Diagrams (continued)

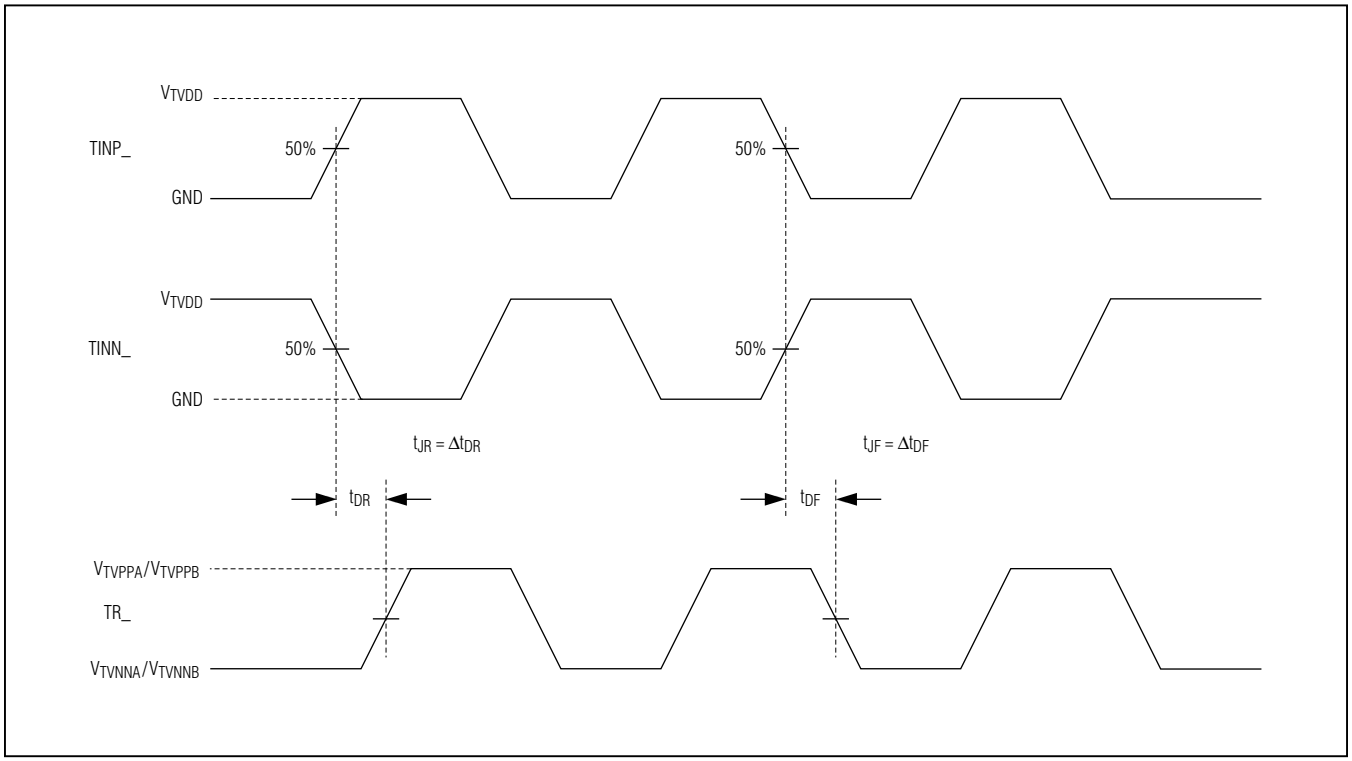
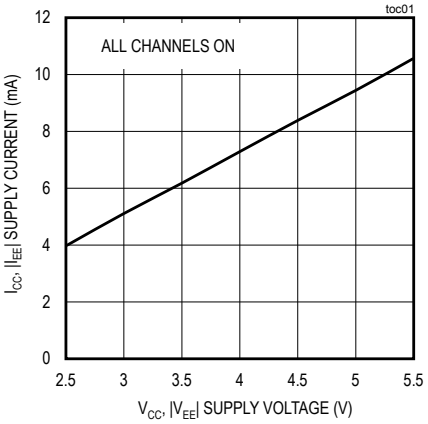


Figure 7. Jitter Timing

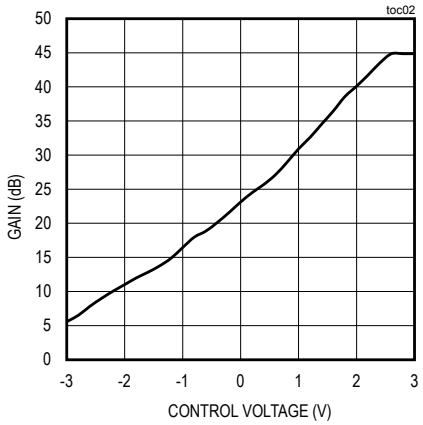
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

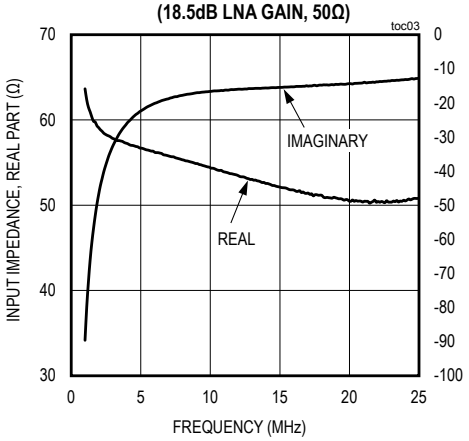
I_{CC}, $|I_{EE}|$ SUPPLY CURRENT vs. V_{CC}, $|V_{EE}|$ SUPPLY VOLTAGE



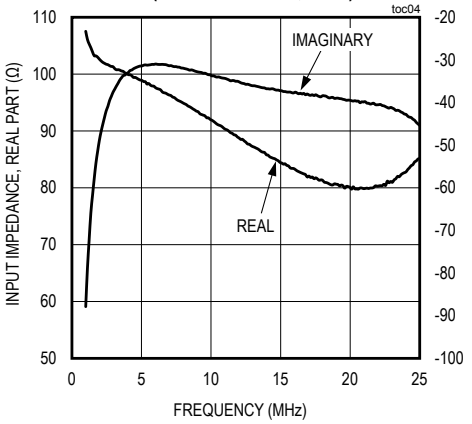
GAIN vs. DIFFERENTIAL ANALOG CONTROL VOLTAGE



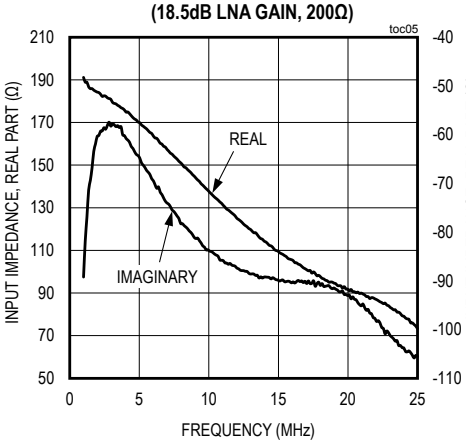
COMPLEX INPUT IMPEDANCE vs. FREQUENCY (18.5dB LNA GAIN, 50Ω)



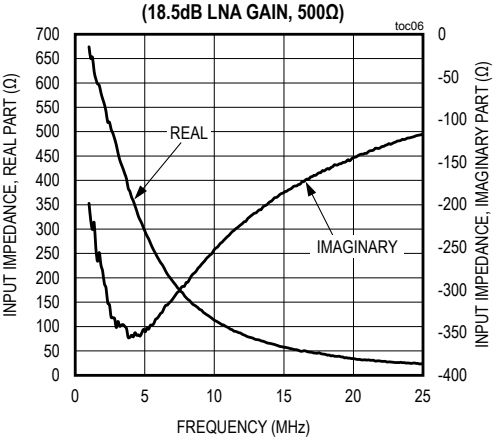
COMPLEX INPUT IMPEDANCE vs. FREQUENCY (18.5dB LNA GAIN, 100Ω)



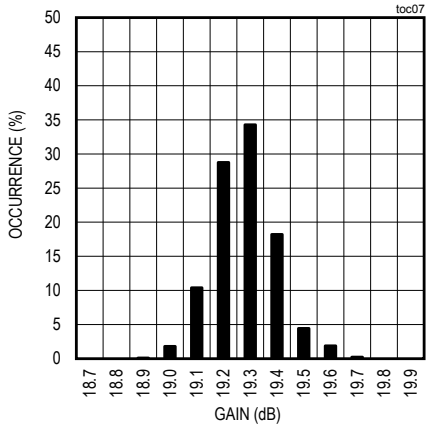
COMPLEX INPUT IMPEDANCE vs. FREQUENCY (18.5dB LNA GAIN, 200Ω)



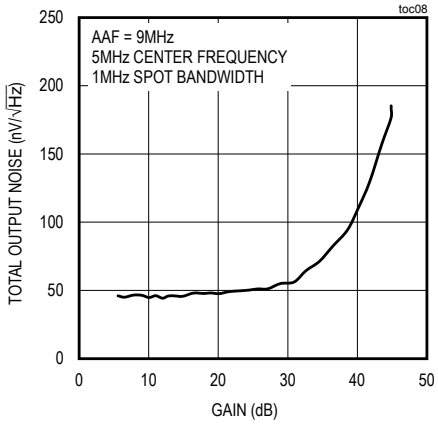
COMPLEX INPUT IMPEDANCE vs. FREQUENCY (18.5dB LNA GAIN, 500Ω)



GAIN DISTRIBUTION V_{GC+} - V_{GC-} = -0.35V



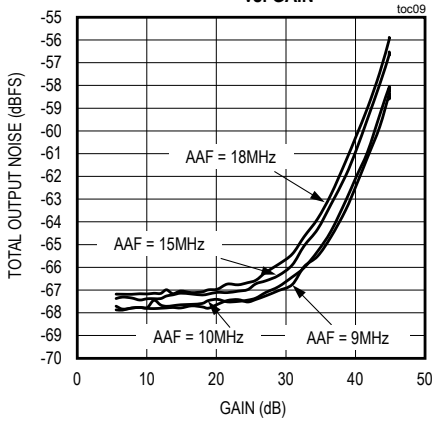
TOTAL OUTPUT SPOT NOISE vs. GAIN



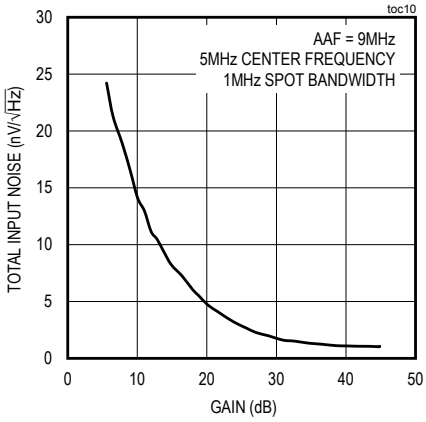
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

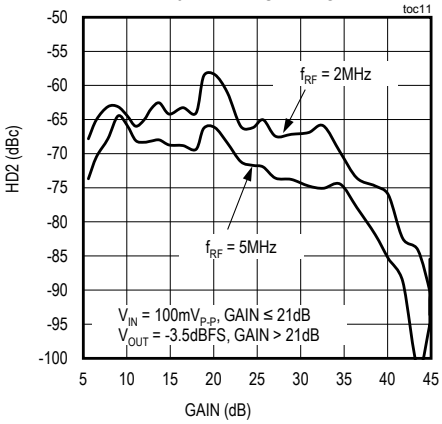
TOTAL OUTPUT NOISE vs. GAIN



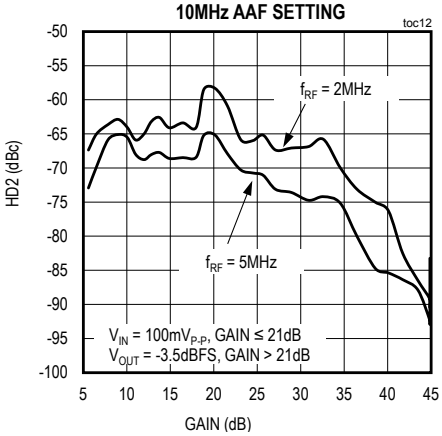
TOTAL INPUT SPOT NOISE vs. GAIN



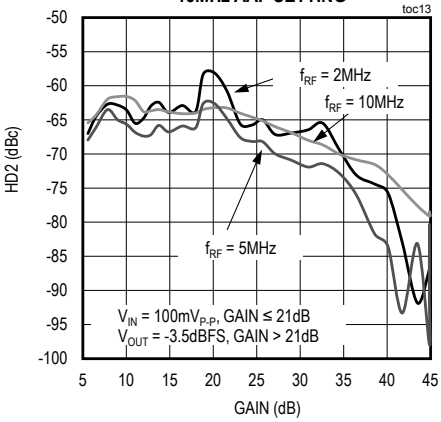
SECOND HARMONIC DISTORTION vs. GAIN 9MHz AAF SETTING



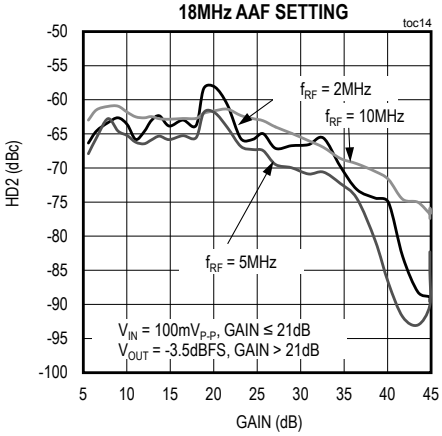
SECOND HARMONIC DISTORTION vs. GAIN 10MHz AAF SETTING



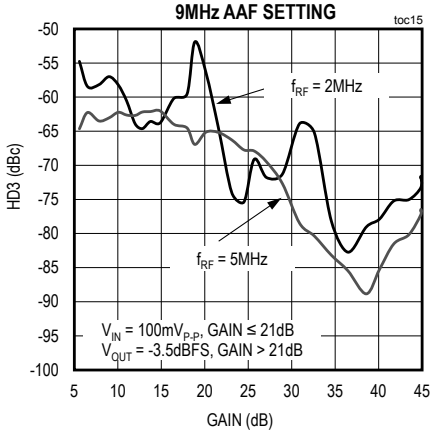
SECOND HARMONIC DISTORTION vs. GAIN 15MHz AAF SETTING



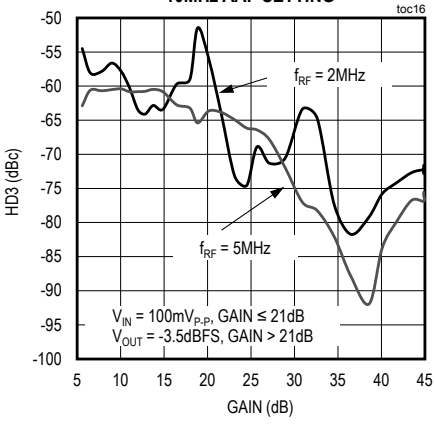
SECOND HARMONIC DISTORTION vs. GAIN 18MHz AAF SETTING



THIRD HARMONIC DISTORTION vs. GAIN 9MHz AAF SETTING



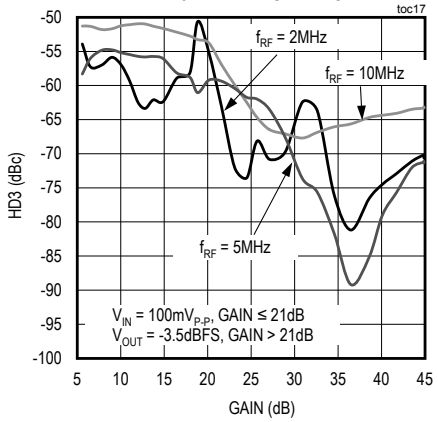
THIRD HARMONIC DISTORTION vs. GAIN 10MHz AAF SETTING



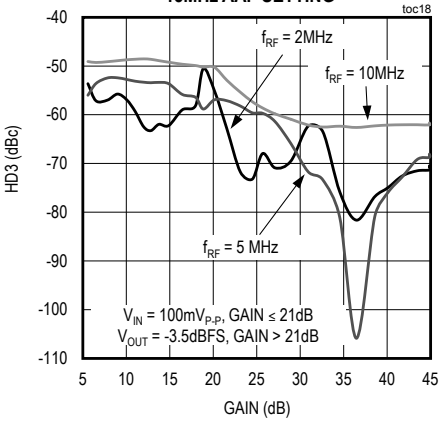
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

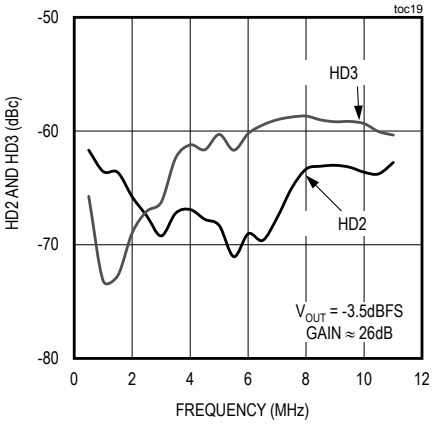
THIRD HARMONIC DISTORTION vs. GAIN 15 MHz AAF SETTING



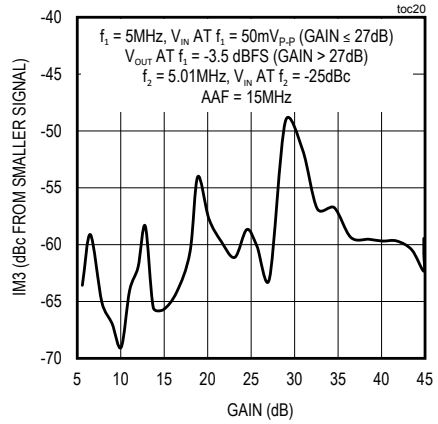
THIRD HARMONIC DISTORTION vs. GAIN 18MHz AAF SETTING



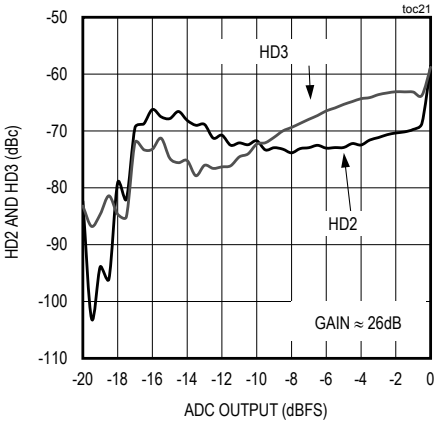
SECOND AND THIRD HARMONIC DISTORTION vs. FREQUENCY



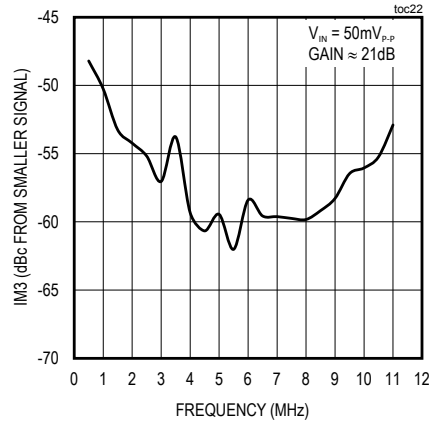
IM3 DISTORTION vs. GAIN



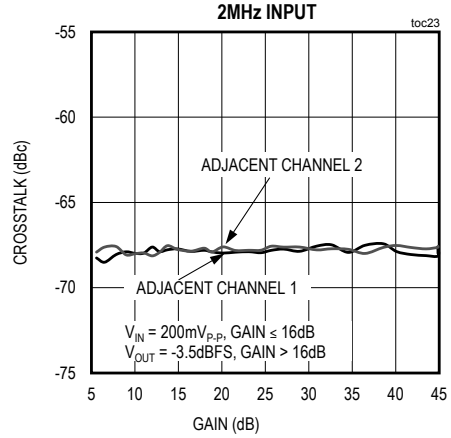
SECOND AND THIRD HARMONIC DISTORTIOI vs. ADC OUTPUT



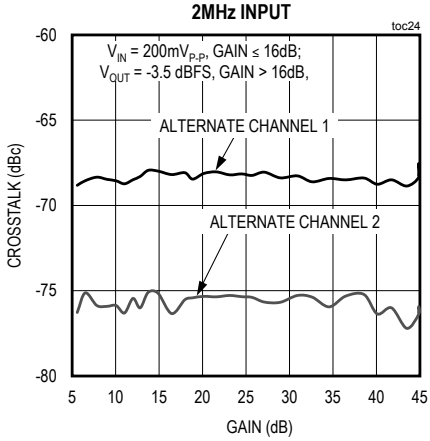
IM3 DISTORTION vs. FREQUENCY



ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN 2MHz INPUT



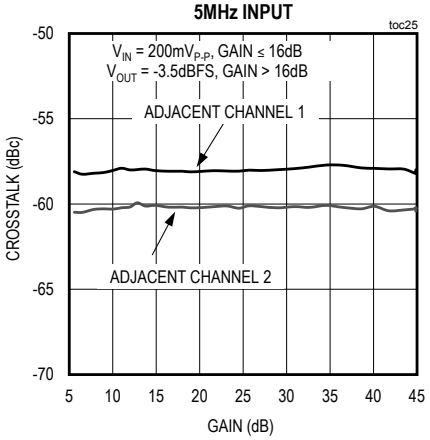
ALTERNATE CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN 2MHz INPUT



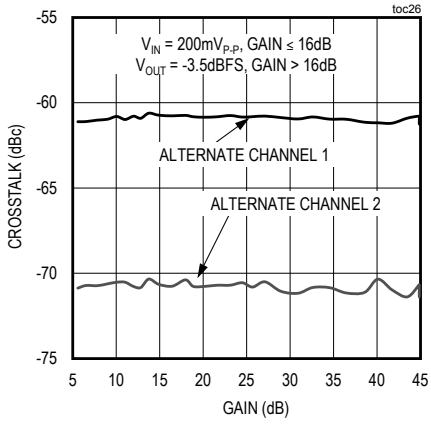
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

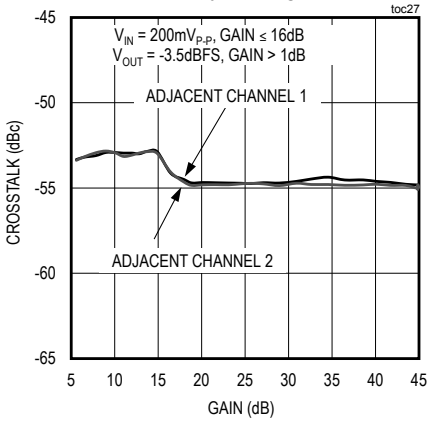
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN 5MHz INPUT



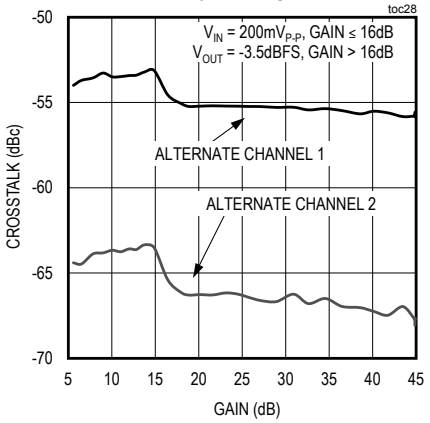
ALTERNATE CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN 5MHz INPUT



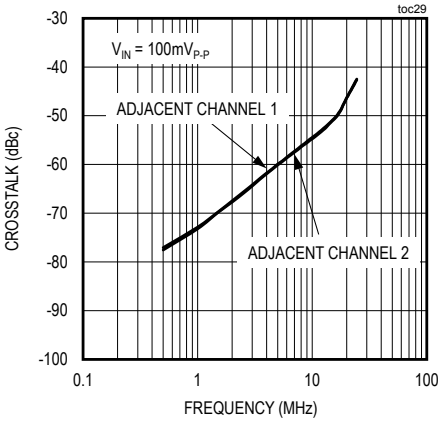
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN 10MHz INPUT



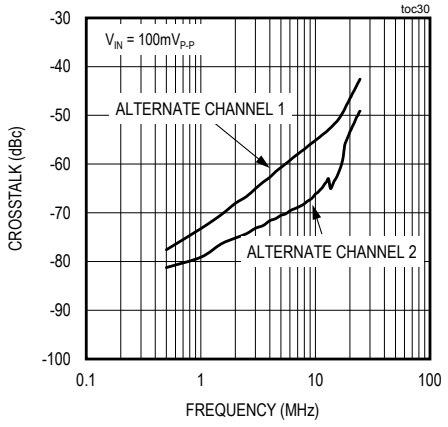
ALTERNATE CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN 10MHz INPUT



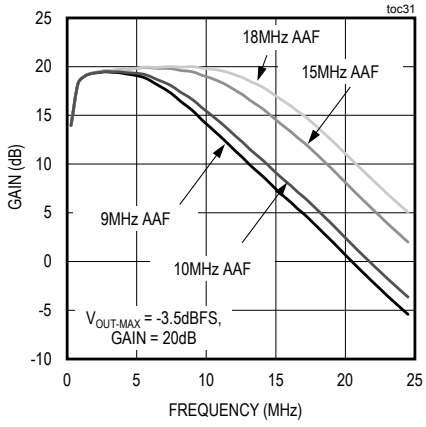
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



ALTERNATE CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



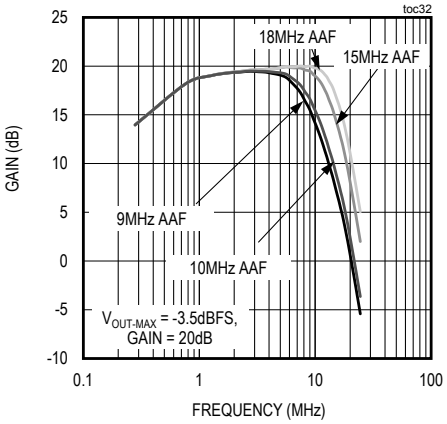
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY (GAIN = 20dB)



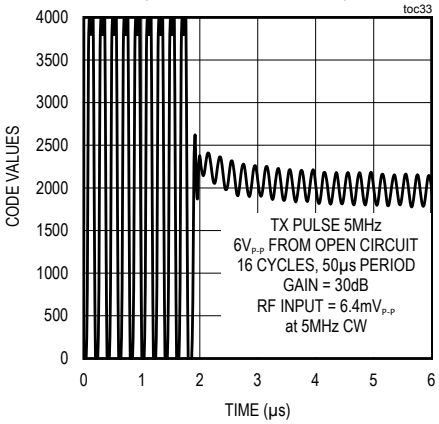
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

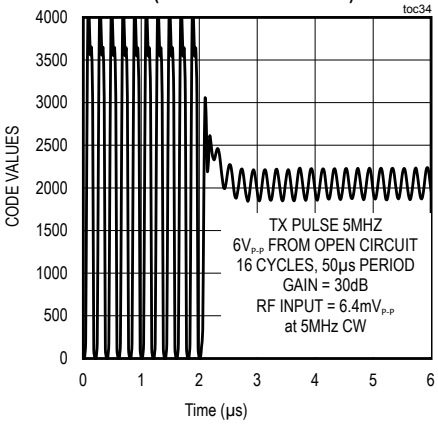
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY (GAIN = 20dB)



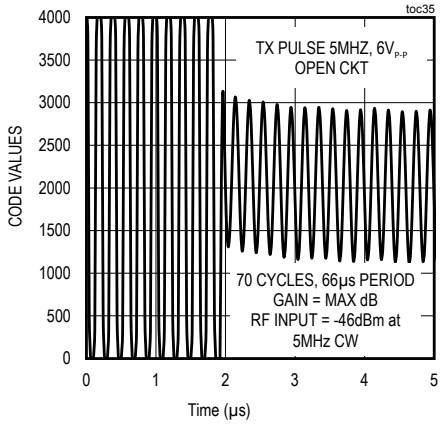
LNA OVERLOAD RECOVERY (DIGITAL HPF DISABLED)



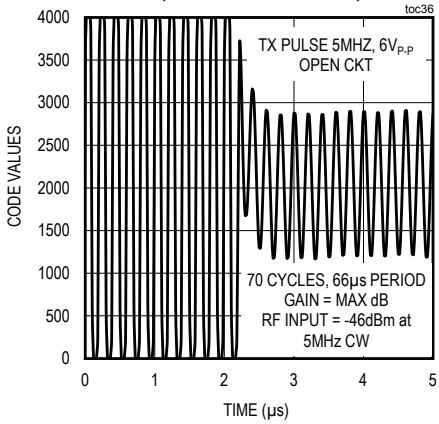
LNA OVERLOAD RECOVERY (DIGITAL HPF ENABLED)



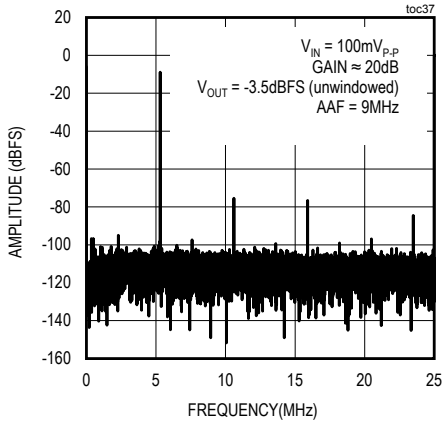
VGA OVERLOAD RECOVERY (DIGITAL HPF DISABLED)



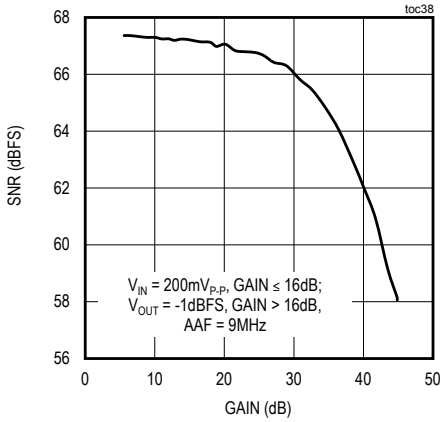
VGA OVERLOAD RECOVERY (DIGITAL HPF ENABLED)



FFT PLOT 8192 POINTS



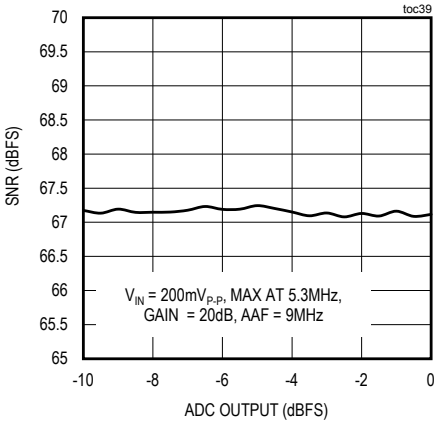
SNR vs. GAIN



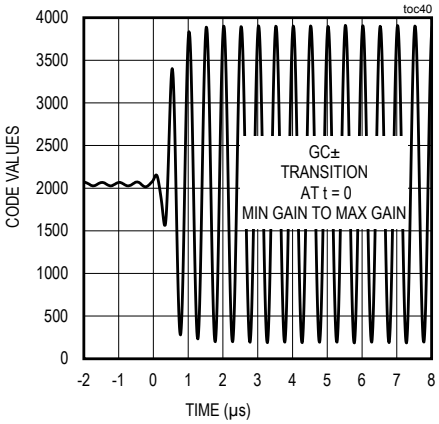
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

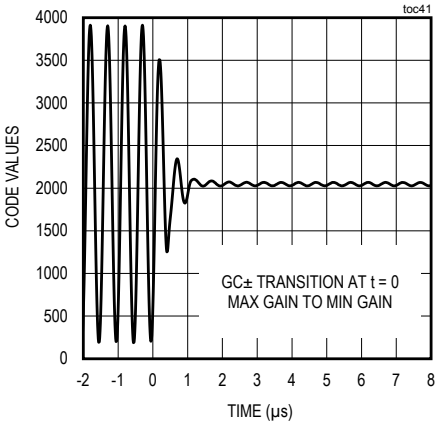
SNR vs. ADC OUTPUT



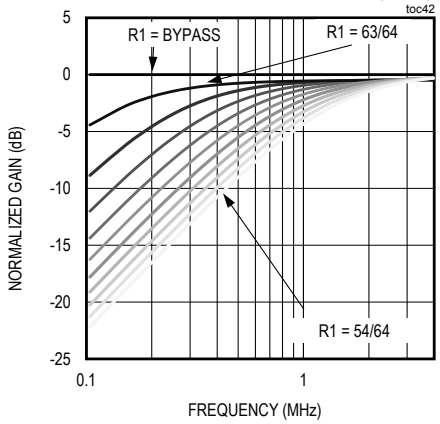
VGA GAIN CONTROL RESPONSE TIME (UP)



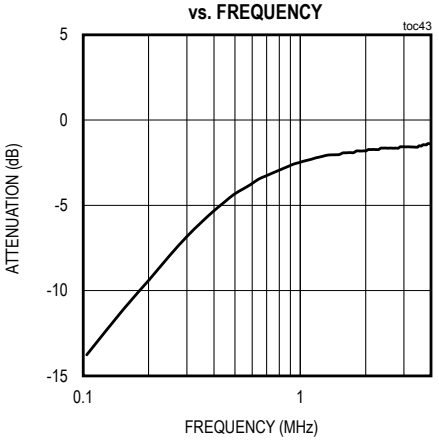
VGA GAIN CONTROL RESPONSE TIME (DOWN)



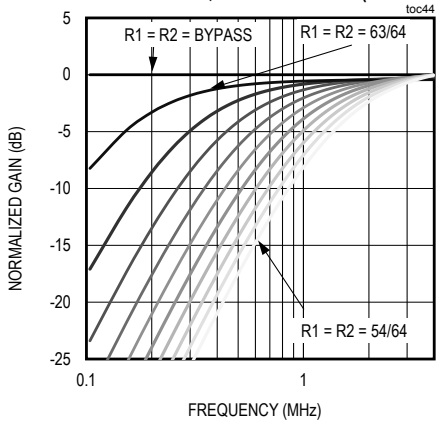
DIGITAL HIGHPASS FILTER NORMALIZED MAGNITUDE RESPONSES vs. FREQUENCY, FIRST SECTION (HPF1)



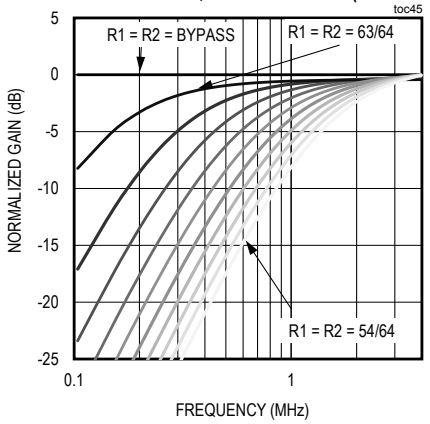
INPUT NETWORK ATTENUATION DUE TO AC-COUPLING vs. FREQUENCY



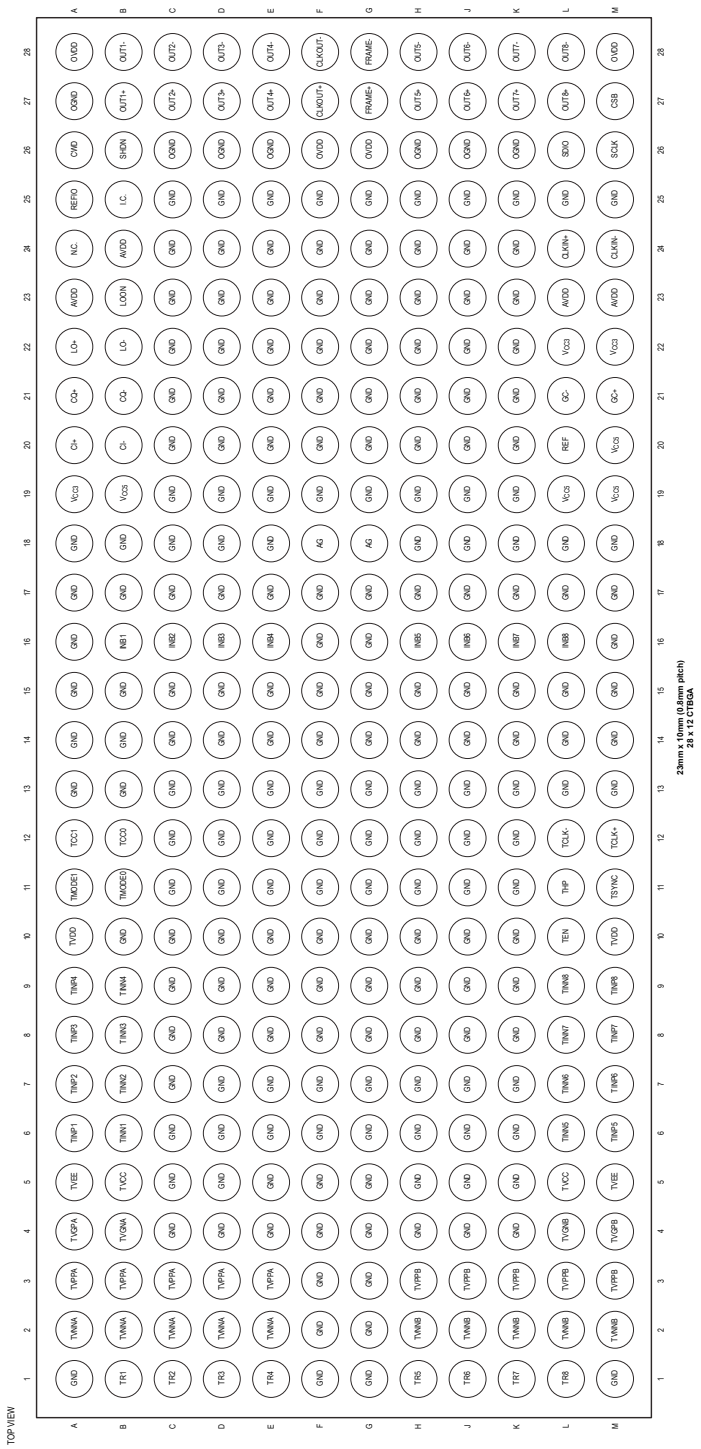
DIGITAL HIGHPASS FILTER NORMALIZED MAGNITUDE RESPONSES vs. FREQUENCY, BOTH SECTIONS (HPF1 + HPF2)



DIGITAL HIGHPASS FILTER NORMALIZED MAGNITUDE RESPONSES vs. FREQUENCY, BOTH SECTIONS (HPF1 + HPF2)



Bump Configuration



Bump Description

BUMP	NAME	FUNCTION
A1, A13–A18, A27, B10, B13-B15, B17, B18, C4-C15, C17-C26, D4-D15, D17-D26, E4-E15, E17-E26, F1-F17, F19-F25, G1-G17, G19-G25, H4-H15, H17-H26, J4-J15, J17-J26, K4-K15, K17-K26, L13-L15, L17, L18, L25, M1, M13-M18, M25	GND	Ground
A2, B2, C2, D2, E2	TVNNA	High-Voltage Negative Supply Input. Bypass TVNNA to GND with a 0.1µF capacitor as close as possible to the device.
A3, B3, C3, D3, E3	TVPPA	High-Voltage Positive Supply Input. Bypass TVPPA to GND with a 0.1µF capacitor as close as possible to the device.
A4	TVGPA	Driver Voltage Supply Output. Connect 1µF capacitor to TVPPA as close as possible to the device.
A5, M5	TVEE	TVEE Supply Voltage Input. Bypass TVEE (both pins) to GND with a 0.1µF capacitor as close as possible to the device.
A6	TINP1	Digital Signal Positive Input 1 (see Table 1).
A7	TINP2	Digital Signal Positive Input 2 (see Table 1).
A8	TINP3	Digital Signal Positive Input 3 (see Table 1).
A9	TINP4	Digital Signal Positive Input 4 (see Table 1).
A10, M10	TVDD	Logic Supply Voltage Input. Bypass TVDD (both pins) to GND with a 0.1µF capacitor as close as possible to the device.
A11	TMODE1	Mode Control Input. Control operation mode (see Table 1).
A12	TCC1	Current Control Input. Control current capability (see Table 2).
A19, L22, M22	V_{CC3}	3.3V Power-Supply Voltage Input. Bypass to GND with a 0.1µF capacitor as close as possible to the part.
A20	CI+	8-Channel CW Positive In-Phase Output. Connect to 11V with a 120Ω external resistor.
A21	CQ+	8-Channel CW Positive Quadrature Output. Connect to 11V with a 120Ω external resistor.
A22	LO+	Positive CW Local Oscillator Input. This clock is then divided in the beamformer.
A23, B24, L23, M23	AVDD	1.8V Analog ADC Power-Supply Voltage Input. Bypass AVDD to GND with a 0.1µF capacitor as close as possible to the device.
A24	N.C.	No Connection. Not internally connected.
A25	REFIO	I/O Reference (For Internal Calibration). Bypass REFIO to GND with a 0.1µF capacitor as close as possible to the device (do not drive REFIO).

Bump Description (continued)

BUMP	NAME	FUNCTION
A26	CWD	VGA/CW Mode Select. Set CWD low to enable the VGAs and disable the CW mixers. Set CWD high to enable the CW mixers and disable the VGAs.
A28, F26, G26, M28	OVDD	1.8V Digital ADC Power-Supply Voltage Input. Bypass OVDD to GND with a 0.1µF capacitor as close as possible to the device.
B1	TR1	Transmit Pulser Output, Receiver Input Channel 1
B4	TVGNA	Driver Voltage Supply Output. Connect 1µF capacitor to TVNNA as close as possible to the device.
B5, L5	TVCC	TVCC Supply Voltage Input. Bypass TVCC (both pins) to GND with a 0.1µF capacitor as close as possible to the device.
B6	TINN1	Digital Signal Negative Input 1 (see Table 1).
B7	TINN2	Digital Signal Negative Input 2 (see Table 1).
B8	TINN3	Digital Signal Negative Input 3 (see Table 1).
B9	TINN4	Digital Signal Negative Input 4 (see Table 1).
B11	TMODE0	Mode Control Input. Control operation mode (see Table 1).
B12	TCC0	Current Control Input. Control current capability (see Table 2).
B16	INB1	Low Voltage T/R switch output/LNA input channel 1
B19, L19, M19, M20	V_{CC5}	4.75V Power-Supply Voltage Input. Bypass to GND with a 0.1µF capacitor as close as possible to the device.
B20	CI-	8-Channel CW Negative In-Phase Output. Connect to 11V with a 120Ω external resistor.
B21	CQ-	8-Channel CW Negative Quadrature Output. Connect to 11V with a 120 Ω external resistor.
B22	LO-	Negative CW Local Oscillator Input. This clock is then divided in the beamformer.
B23	LOON	LO On Control Input. Turns LO on starting on the next rising or falling edge of LO.
B25	I.C.	Internally Connected. Leave unconnected.
B26	SHDN	Power-Down (Nap or Sleep Mode Programmable Through Serial Interface)
B27	OUT1+	Channel 1 Positive LVDS Output
B28	OUT1-	Channel 1 Negative LVDS Output
C1	TR2	Transmit Pulser Output, Receiver Input Channel 2
C16	INB2	Low Voltage T/R Switch Output/LNA Input Channel 2
C27	OUT2+	Channel 2 Positive LVDS Output
C28	OUT2-	Channel 2 Negative LVDS Output
D1	TR3	Transmit Pulser Output, Receiver Input Channel 3
D16	INB3	Low Voltage T/R Switch Output/LNA Input Channel 3
D27	OUT3+	Channel 3 Positive LVDS Output
D28	OUT3-	Channel 3 Negative LVDS Output
E1	TR4	Transmit Pulser Output, Receiver Input Channel 4

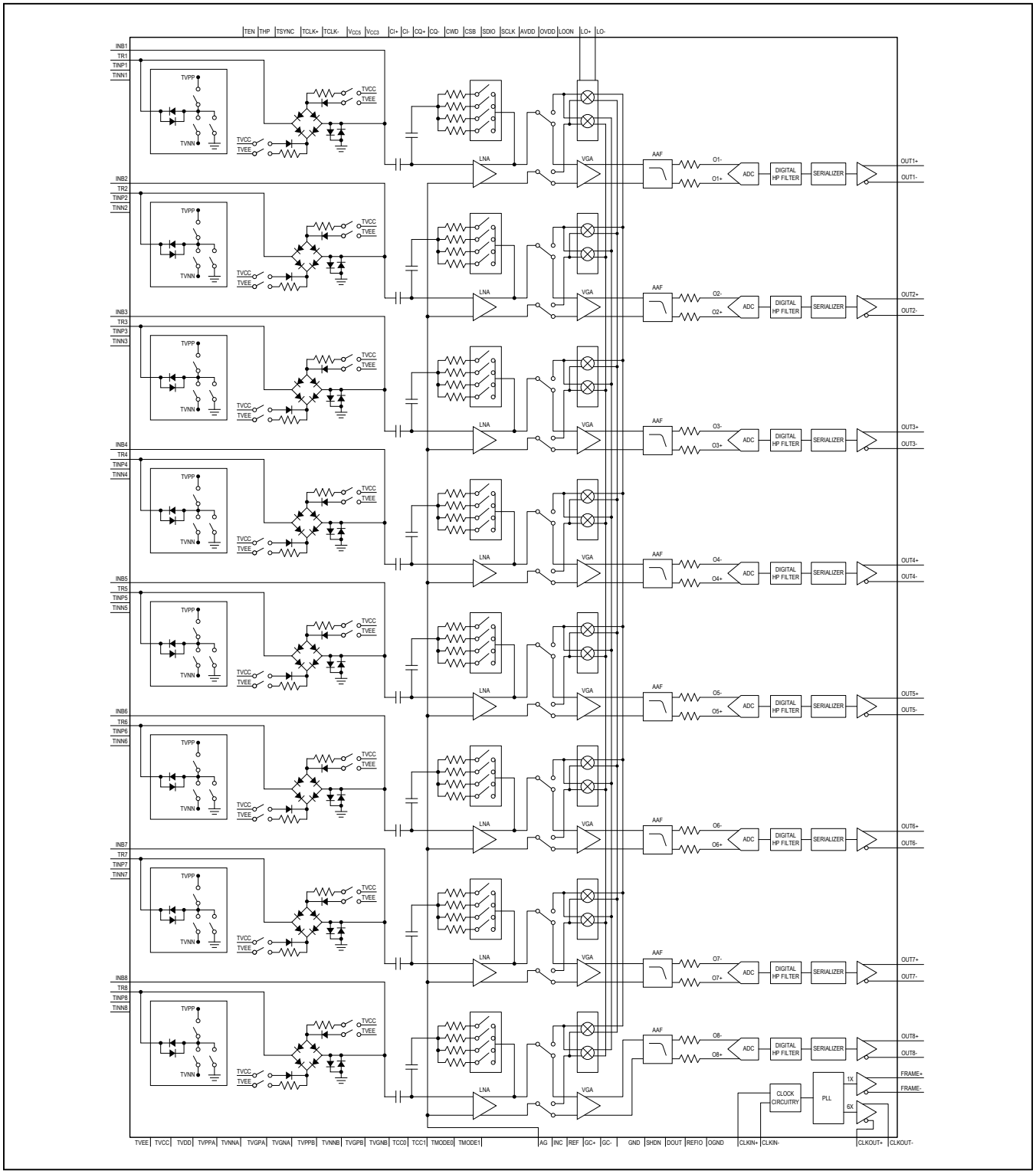
Bump Description (continued)

BUMP	NAME	FUNCTION
E16	INB4	Low Voltage T/R Switch Output/LNA Input Channel 4
E27	OUT4+	Channel 4 Positive LVDS Output
E28	OUT4-	Channel 4 Negative LVDS Output
F18, G18	AG	Analog Ground for LNA Inputs. Leave AG unconnected.
F27	CLKOUT+	Positive LVDS Serial-Clock Output
F28	CLKOUT-	Negative LVDS Serial-Clock Output
G27	FRAME+	Positive Frame-Alignment LVDS Output
G28	FRAME-	Negative Frame-Alignment LVDS Output
H1	TR5	Transmit Pulser Output, Receiver Input Channel 5
H2, J2, K2, L2, M2	TVNNB	High-Voltage Negative Supply Input. Bypass TVNNB to GND with a 0.1µF capacitor as close as possible to the device.
H3, J3, K3, L3, M3	TVPPB	High-Voltage Positive Supply Input. Bypass TVPPB to GND with a 0.1µF capacitor as close as possible to the device.
H16	INB5	Low Voltage T/R Switch Output/LNA Input Channel 5
H27	OUT5+	Channel 5 Positive LVDS Output
H28	OUT5-	Channel 5 Negative LVDS Output
J1	TR6	Transmit Pulser Output, Receiver Input Channel 6
J16	INB6	Low Voltage T/R Switch Output/LNA Input Channel 6
J27	OUT6+	Channel 6 Positive LVDS Output
J28	OUT6-	Channel 6 Negative LVDS Output
K1	TR7	Transmit Pulser Output, Receiver Input Channel 7
K16	INB7	Low Voltage T/R Switch Output/LNA Input Channel 7
K27	OUT7+	Channel 7 Positive LVDS Output
K28	OUT7-	Channel 7 Negative LVDS Output
L1	TR8	Transmit Pulser Output, Receiver Input Channel 8
L4	TVGNB	Driver Voltage Supply Output. Connect 1µF capacitor to TVNNB as close as possible to the device.
L6	TINN5	Digital Signal Negative Input 5 (see Table 1).
L7	TINN6	Digital Signal Negative Input 6 (see Table 1).
L8	TINN7	Digital Signal Negative Input 7 (see Table 1).
L9	TINN8	Digital Signal Negative Input 8 (see Table 1).
L10	TEN	Internal Supply Generator Control Input. Drive TEN high to disable the internal power supply when using an external power supply on TVGPA, TVGPB, TVGNA, and TVGNB. TEN has an internal 10kΩ pulldown resistor to GND.
L11	THP	Open-Drain Thermal-Protection Output. THP asserts and sinks a 3mA current to GND when the junction temperature exceeds +150 C.

Bump Description (continued)

BUMP	NAME	FUNCTION
L12	TCLK-	CMOS Control Input. Clock negative phase input. Data inputs are clocked in at the edge of TCLK+ and TCLK- in differential clocked mode. Clock maximum frequency is 160MHz (max). If TCLK- is connected to GND, TCLK+ input is single-ended logic-level clock input. Otherwise, TCLK and TCLK+ are self-biased differential clock inputs.
L16	INB8	Low Voltage T/R switch output/LNA input channel 8
L20	V_{REF}	Voltage Reference Input. Bypass V_{REF} to GND with a capacitor.
L21	GC-	Negative Gain Control Voltage. Set V_{GC+} - V_{GC-} = +3V for maximum gain. Set V_{GC+} - V_{GC-} = -3V for minimum gain.
L24	CLKIN+	Positive Differential ADC Clock Input
L26	SDIO	Serial-Data Input
L27	OUT8+	Channel 8 Positive LVDS Output
L28	OUT8-	Channel 8 Negative LVDS Output
M4	TVGPB	Driver Voltage Supply Output. Connect 1µF capacitor to TVPPB as close as possible to the device.
M6	TINP5	Digital Signal Positive Input 5 (see Table 1).
M7	TINP6	Digital Signal Positive Input 6 (see Table 1).
M8	TINP7	Digital Signal Positive Input 7 (see Table 1).
M9	TINP8	Digital Signal Positive Input 8 (see Table 1).
M11	TSYNC	CMOS Control Input. Drive TSYNC high to enable clocked-input mode. Drive TSYNC low to operate in transparent mode (see the *Truth Tables* section).
M12	TCLK+	CMOS Control Input. Clock positive phase input. Data inputs are clocked in at the rising edge of TCLK in differential clocked mode or at the rising edge of TCLK+ in single-ended clocked mode. Clock maximum frequency is 160MHz.
M21	GC+	Postive Gain Control Voltage. Set V_{GC+} - V_{GC-} = +3V for maximum gain. Set V_{GC+} - V_{GC-} = -3V for minimum gain.
M24	CLKIN-	Negative Differential ADC Clock Input. Connect to GND for a single ended clock
M26	SCLK	Serial-Clock Input.
M27	$\overline{CS}$	Chip Select

Functional Diagram



Detailed Description

The MAX2082 is a fully integrated high-density octal ultrasound transceiver optimized for low-cost, high-channel count, high-performance portable and cart based ultrasound systems. The easy-to-use integrated receiver allows the user to achieve high-end 2D and Doppler imaging capability using substantially less space and power. The integrated octal 3-level pulser, T/R switch, input coupling caps, LNA, VGA, AAF, ADC, and digital HPF achieves an ultra-low noise figure with a low per channel power dissipation at 50Msps.

The transmitters are high-performance, three-level, 2A, high-voltage (HV) pulser devices capable of generating high-frequency, HV bipolar pulses (up to ±105V) from low-voltage control logic inputs for driving. All eight channels have embedded overvoltage-protection diodes and integrated active return-to-zero clamp. These pulsers have embedded independent (floating) power supplies (FPSs) and level shifters that allow signal transmission without the need for external HV capacitors.

Each channel is controlled by two logic inputs (TINN_/TINP_) and the active return to zero features half the current driving of the pulser (1A typ).

The pulsers can operate both in clocked and transparent mode. In clocked mode, data inputs can be synchronized with a clean differential or single-ended clock to reduce phase noise associated with FPGA output signals that are detrimental for Doppler analysis. In transparent mode, the synchronization feature is disabled and output reflects the data input after an 18ns delay. An adjustable maximum current (0.5A to 2A) reduces power consumption when full current capability is not required.

The pulsers feature integrated grass-clipping diodes (with low parasitic capacitance) for receive (Rx) and transmit (Tx) isolations. A damping circuit fully discharges the pulser's output internal node before the grass-clipping diodes. This damping circuit (typically 500Ω can be activated as soon as the transmit burst is over.

The full receive channel has been optimized for second-harmonic imaging. Dynamic range is also optimized for exceptional pulsed and color flow Doppler performance under high-clutter conditions. The bipolar front-end and CMOS ADC have also been optimized for an exceptionally low near carrier modulation noise for excellent low velocity Doppler sensitivity.

The MAX2082 also includes an octal CWD beamformer for a full Doppler solution. Separate mixers for each channel are made available for optimal CWD sensitivity.

Transmit Pulser

Modes of Operation

Operating modes for the pulsers and T/R switches are controlled by TMODE[1:0] (Table 1).

Shutdown Mode (TMODE0, TMODE1 = 00)

All channels are disabled, no transmission/ reception is possible. This mode has the lowest power consumption for the pulsers and T/R switch. Shut down the AFE through the serial interface to further reduce power consumption.

Octal 3 Level Mode (TMODE0, TMODE1 = 10)

The pulser uses all eight independent channels. Each channel can generate a three-level pulse. The high-side and low-side FET of each channel are capable of providing 2.0A current, while the clamp is capable of 1A current.

Disable Transmit Mode (TMODE0, TMODE1 = 11)

All eight high-voltage transmit channels are disabled, no pulse transmission is possible. The T/R switch can be turned on (to receive low-voltage signals) or off (for isolation).

Current Capability Selection

The pulser features current drive capability selection. Two control inputs (TCC0, TCC1) control the current drive capability (Table 2).This feature can be used to save power when working in low voltage mode (such as CWD application) and the maximum current capability is no longer required.

Table 1. Transmit Pulser Operating Modes and Truth Table

MODE INPUTS		OPERATING MODE	INPUTS		OUTPUTS	
TMODE0	TMODE1		TINN_	TIPP_	TR_	INB_ (LNA INPUT)
0	0	Shutdown	X		High Impedance	High Impedance (T/R switch off)
1	0	Octal 3 levels	0	0	Clamp on (damp off)	GND (T/R switch off)
			1	0	V_{TVNNA}/V_{TVNNB} (damp off)	GND (T/R switch off)
			0	1	V_{TVPPA}/V_{TVPPB} (damp off)	GND (T/R switch off)
			1	1	Clamp on (damp on)	T/R switch on
0	1	Reserved	Do not use			
1	1	Transmit disable	0	0	High Impedance (damp off)	GND (T/R switch off)
			1	0	High Impedance (damp off)	GND (T/R switch off)
			0	1	High Impedance (damp off)	GND (T/R switch off)
			1	1	High Impedance (damp on)	T/R switch on

Table 2. Transmit Pulser Output Current

TCC0	TCC1	PULSER OUTPUT CURRENT (TYP)
0	0	2A
1	0	1.5A
0	1	1A
1	1	0.5A

Sync Feature

The devices provide the ability to resynchronize all the data inputs by means of a clean clock signal. In ultrasound systems, the FPGA output signals are often affected by a high jitter. The jitter induces phase noise that is detrimental in Doppler analysis. The input clock can be either a differential signal or a single-ended signal running up to 160MHz. Data are clocked in on the rising edge of the TCLK+ input (falling edge of TCLK-). Connect TCLK- to GND for single-ended operation. The sync feature can be enabled or disabled by the TSYNC control input. Drive TSYNC input low to disable the synchronization function (no external clock signal). Drive TSYNC input high to enable the synchronization function (with an external clock signal). Figure 8 shows the simplified TCLK+ and TCLK- inputs schematic.

T/R Switch and Control

Each channel features a low-power T/R switch. The T/R switch recovery time after the transmission is less than 1.2µs. The T/R switches are controlled by the same pulser digital inputs (see Table 1). No dedicated input signals are required to activate/deactivate the T/R switches. The integrated T/R switches do not require any special timings and can operate synchronously with the digital pulser. In order to minimize the leakage current during transmission, it's recommended to switch off the T/R switches 3µs before the beginning of the transmit burst.

Grass Clipping Diodes

A pair of diodes in antiparallel configuration (referred to as grass-clipping diodes) is presented at each pulser's output. The diodes' reverse capacitance is extremely low, allowing a perfect isolation between the receive path and the actual pulser's output stage.

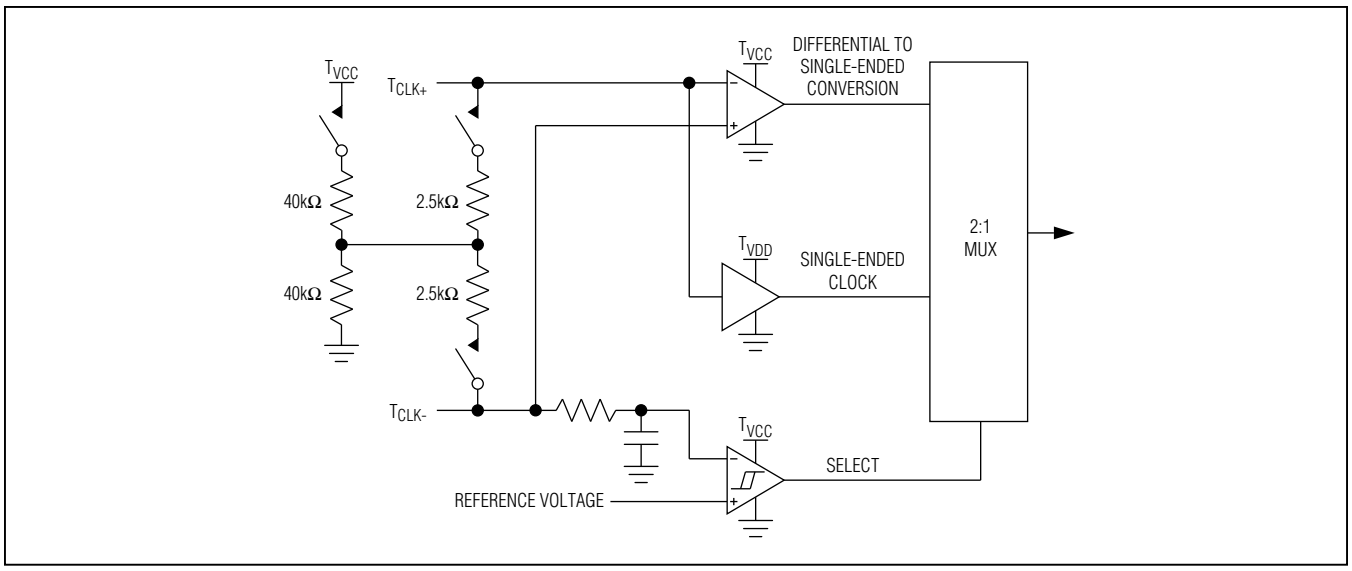


Figure 8. Simplified Clock Input Schematic

Active Damp Circuit

An active damp circuit is integrated between the internal pulser output node (before grass-clipping diodes) and GND. The purpose of this circuit is to fully discharge the pulser output internal node so that the node is not left in high-impedance condition as soon as the transmit burst is over. This results in two main advantages

1) The grass-clipping isolation is more effective
2) Suppression of any low frequency oscillation of such a node that could be detrimental for Doppler mode performances

Independent (Floating) Power-Supply Enable (TEN)

The device features the TEN control input to enable/disable the internal FPSs. This allows the usage of external high-efficiency power supplies to save system power. This option must be considered only for special applications requiring extremely low power dissipation. The low-power dissipation of the embedded FPSs already meets power requirements in most of the cases. Drive TEN low or leave unconnected to enable the internal FPSs; drive TEN high to disable the internal FPSs.

Thermal Protection

The devices feature an open-drain thermal-protection output (THP). When the internal junction temperature exceeds +145°C, the devices automatically enter shutdown mode and THP asserts. The devices reenter normal operation and the THP deasserts when the die temperature drops below +125°C.

Analog Front End (AFE)

Modes of Operation

Operating modes for the AFE are controlled by seventeen 8-bit registers (00h–10h). This is described in the Register Settings section.

Low-Noise Amplifier (LNA)

Each of the device's LNAs is optimized for excellent dynamic range and linearity performance characteristics, making it ideal for ultrasound imaging applications. When the LNA is placed in low-gain mode, the input resistance (R_{IN}), being a function of the gain A (R_{IN} = RF/(1 + A)), increases by a factor of approximately 2. Consequently, the switches that control the feedback resistance (R_{FB}) have to be changed. For instance, the 100Ω mode in high gain becomes the 200Ω mode in low gain (Table 32)

Variable-Gain Amplifier (VGA)

The device's VGAs are optimized for high linearity, high dynamic range, and low output-noise performance, all of which are critical parameters for ultrasound imaging applications. Each VGA path includes circuitry for adjusting analog gain, as well as an output buffer with differential output ports that drive the AAF and ADC. The VGA gain can be adjusted through the differential gain-control input (GC+ and GC-). Set the differential gain control input voltage at -3V for minimum gain and +3V for maximum gain. The differential analog control common-mode voltage is 1.65V (typ).

Overload Recovery

The device is also optimized for quick overload recovery for operation under the large input-signal conditions that are typically found in ultrasound input-buffer imaging applications. See the Typical Operating Characteristics for an illustration of the rapid recovery time from a transmit-related overload.

Dynamic offsets or DC offsets in the device can be removed by enabling the digital HPF function contained within the ADC. The unique structure of the digital HPF allows for the removal of up to ±117mV of dynamic or static DC offset, without reducing the dynamic range of the ADC.

Octal Continuous-Wave (CW) Mixer

The device CW mixers are designed using an active double-balanced topology. The mixers achieve high dynamic range and high-linearity performance, with exceptionally low thermal and jitter noise, ideal for ultrasound CWD signal reception.

The octal array exhibits quadrature and in-phase differential current outputs (CQ+, CQ-, CI+, CI-) to produce the total CWD beamformed signal. The maximum differential current output is typically 3mAP-P and the mixer output-compliance voltage ranges from 4.5V to 12V.

Each mixer can be programmed to 1 of 16 phases; therefore, 4 bits are required for each channel for programming. Each CW channel can be programmed to an off state by setting bit CW_SHDN_CHn to 1. The power-down mode (SHDN) line overrides this soft shutdown.

After the serial shift registers have been programmed, the $\overline{CS}$ signal, when going high, loads the phase information in the form of 5 bits per channel into the I/Q phase divider/selectors. This presets the dividers, selecting the appropriate mixer phasing. See Table 42 for mixer phase configurations.

CW Mixer Output Summation

The outputs from the octal-channel mixer array are summed internally to produce the total CWD summed beamformed signal. The octal array produces eight differential quadrature (Q) outputs and eight differential in-phase (I) outputs. All quadrature and in-phase outputs are summed into single I and Q differential current outputs (CQ+, CQ-, CI+, CI-).

CWD beamforming is achieved using a single 8 x LO high-frequency master clock that is divided down to the CWD frequency using internal dividers. The beamformer provides λ/16 resolution with an 8 x LO clock using both edges of the clock, assuming a 50% duty cycle. An easily available low-phase-noise 200MHz master clock can therefore be used to generate the necessary CWD frequencies with adequate resolution.

LO Phase Select

The LO phase dividers can be programmed through the shift registers to allow for 16 quadrature phases for a complete CW beamforming solution.

VGA and CW Mixer Operation

During normal operation, the device is configured so that either the VGA path is enabled while the mixer array is powered down (VGA mode), or the quadrature mixer array is enabled while the VGA path is powered down (CW mode). For VGA mode, set CWD to a logic-high, and for CW mode, set CWD to a logic-low.

External Voltage Reference

Connect an external, low-noise, 2.5V reference to the V_{REF} pin. Bypass V_{REF} to ground with a 0.1µF capacitor as close as possible to the device. The device noise performance is dependent on the external noise at V_{REF}.

ADC Clock Input

The input clock interface provides for flexibility in the requirements of the clock driver. The device accepts a fully differential clock or single-ended logic-level clock (Figure 11). The device is specified for an input sampling 25MHz to 50MHz frequency range. By default, the internal phase-locked loop (PLL) is configured to accept input clock frequencies from 39MHz to 50MHz. The PLL is programmed through the PLL Sampling Rate register (00h, Table 6). Table 7 details the complete range of PLL sampling frequency settings.

For differential clock operation, connect a differential clock to the CLKIN+ and CLKIN- inputs. The input common mode is established internally to allow for AC-coupling. The self-biased input common-mode voltage defaults to 1.2V. The differential clock signal can also be DC-coupled if the externally established common-mode voltage is constrained to the specified clock input common-mode range of 1V to 1.4V. A differential input termination of 100Ω can be switched in by programming the CLKIN Control register (04h[4], Table 21).

For single-ended operation, connect CLKIN- to GND and drive the CLKIN+ input with a logic-level signal. When the CLKIN- input is grounded (or pulled below the threshold of the clock-mode detection comparator), the differential-to-single-ended conversion stage is disabled and the logic-level inverter path is activated. The input common-mode self-bias is disconnected from CLKIN+, and provides a weak pullup bias to AVDD for CLKIN-.

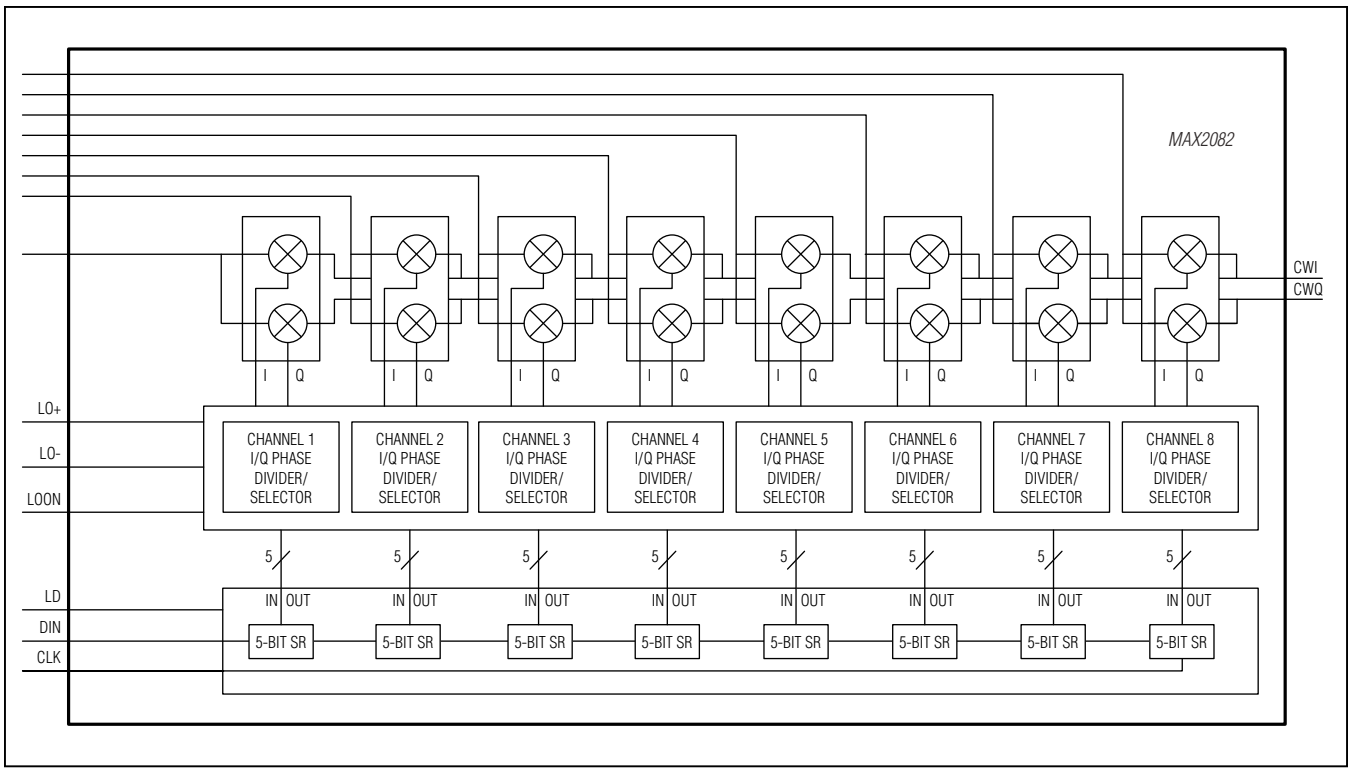


Figure 9. CWD Analog Front-End Beamformer Simplified Block Diagram

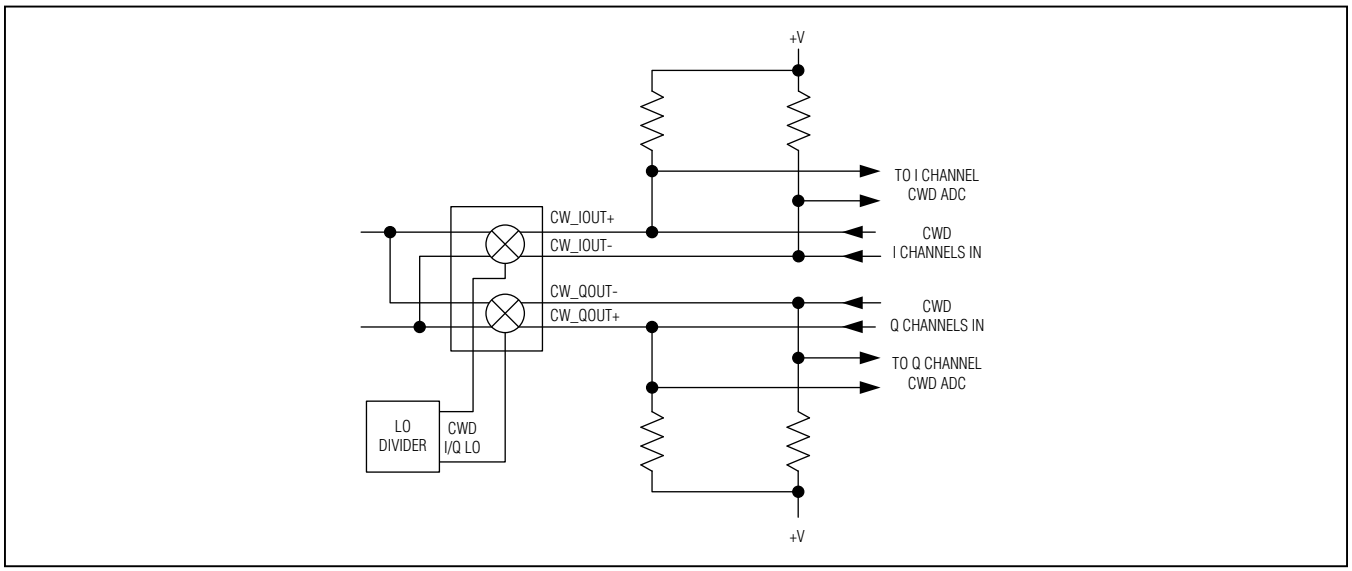


Figure 10. CWD Output Beamforming Example

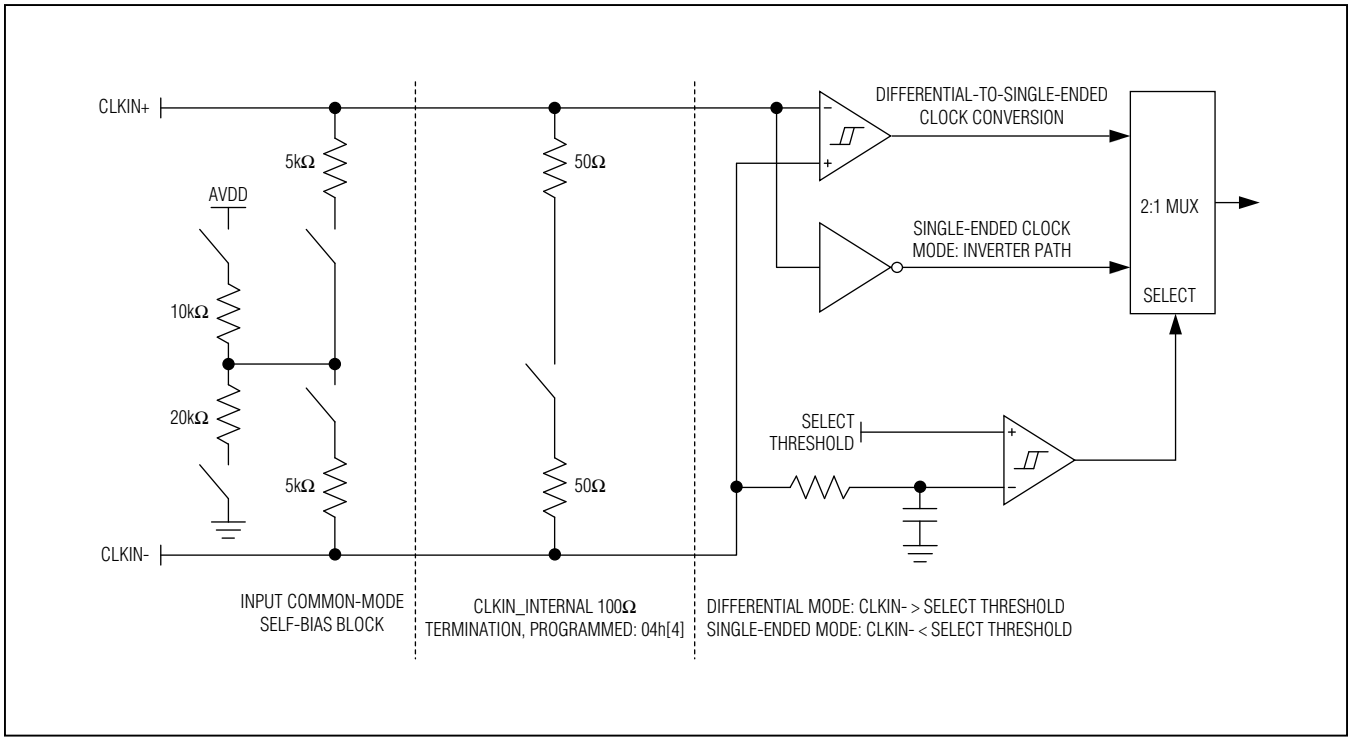


Figure 11. Simplified Clock Input Schematic

Power-Down and Low-Power Mode

The device can also be powered down with the SHDN pin. Set SHDN to 1.8V to place the device in power-down mode. In power-down mode, the device draws a total supply current less than 0µA from the 5V and 3.3V supplies and less than 0.4mA from the 1.8V supplies. Set SHDN to logic-low for normal operation.

A low-power mode is available to lower the required power for CWD operation. When selected, the complex mixers operate at lower quiescent currents. Note that operation in this mode slightly reduces the dynamic performance of the device. Table 8 shows the logic function of the standard operating modes.

In addition to power-down mode, the device can be placed into a reduced-power Standby or Nap mode, which allows for rapid power-up in VGA mode. Nap mode is accessible by setting the SHDN pin to 1.8V, with the ADC_NAP_SHDN1 and AFE_NAP_SHDN1 registers set to 1 (see Table 8). Nap mode is not meant to be used in conjunction with CWD mode; valid CWD power states are normal CWD low-power and power-down modes. Although no device damage occurs, programming the device for Nap mode and setting the SHDN pin high can create invalid signal outputs in CWD mode.

Programmable, Digital Highpass 2-Pole Filter

Digital Highpass Filter Characteristics

This digital HPF is implemented as the cascade of two identical first-order highpass IIR filter sections (Figure 12). Each section implements the difference equation:

$$y[n] = R \times y[n-1] + x[n] - x[n-1]$$

where x[n] is the input and y[n] is the output. The highpass 3dB corner frequency is established by the filter coefficient (R). Each section can be independently programmed to one of 10 possible values or placed into bypass mode (Table 24). The available filter coefficient values and corresponding cutoff frequency are given in Table 3.

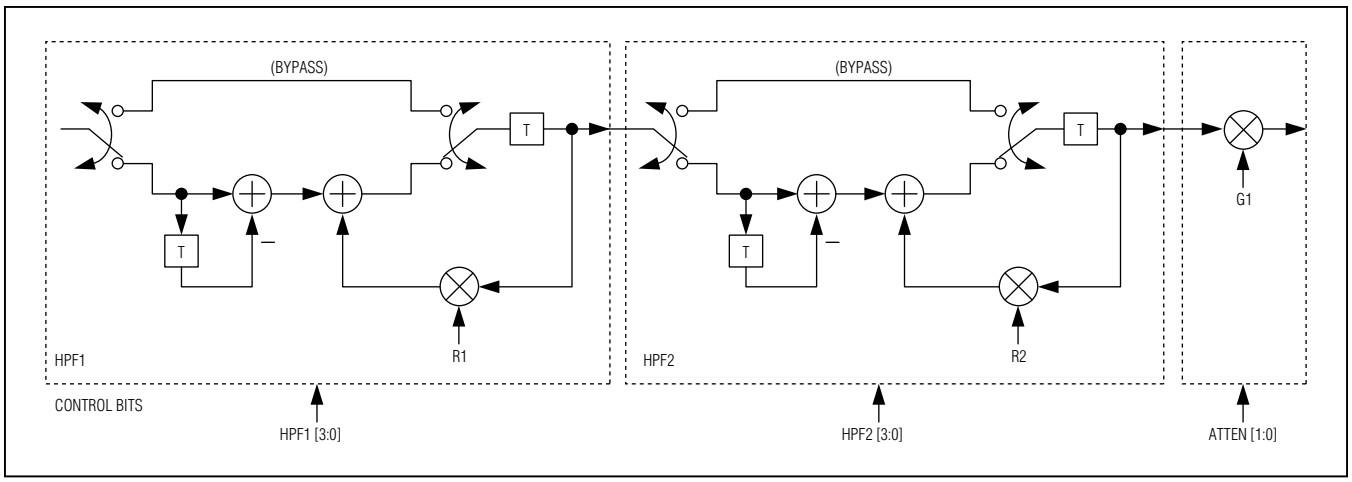


Figure 12. Two-Stage Digital Highpass Filter with 1-Stage Multiplier

Table 3. Digital Filter Cutoff-Frequency Setting

FILTER COEFFICIENT (R)		3dB CUTOFF FREQUENCY(f_S/2)	3dB CUTOFF FREQUENCYMHz (f_S = 50Msps)
ONE-FILTER SECTIONS			
54/64	0.843750	0.046294	1.157
55/64	0.859375	0.041943	1.049
56/64	0.875000	0.037535	0.938
57/64	0.890625	0.033069	0.827
58/64	0.906250	0.028544	0.714
59/64	0.921875	0.023956	0.599
60/64	0.937500	0.019303	0.483
61/64	0.953125	0.014584	0.365
62/64	0.968750	0.009796	0.245
63/64	0.984375	0.004935	0.123
TWO-FILTER SECTIONS			
54/64	0.843750	0.069441	1.736
55/64	0.859375	0.062915	1.573
56/64	0.875000	0.056303	1.408
57/64	0.890625	0.049604	1.240
58/64	0.906250	0.042816	1.070
59/64	0.921875	0.035934	0.898
60/64	0.937500	0.028955	0.724
61/64	0.953125	0.021876	0.547
62/64	0.968750	0.014694	0.367
63/64	0.984375	0.007403	0.185

The digital HPF provides a small-signal gain that depends on the filter coefficient. This effectively reduces slightly the full-scale input range of the ADC. A plot of filter gain vs. filter coefficient is shown in Figure 25. A coarse digital multiplier is incorporated at the output of the filter to provide partial compensation of the digital filter gain. Table 4 provides the recommended gain-compensation settings for different filter cutoff-frequency settings.

The digital filter magnitude, phase, group-delay, and impulse-time response for 1-Stage and 2-Stage configurations are shown in Figure 13 to Figure 24, respectively.

Table 4. Gain-Compensation Settings for Different Filter Cutoff-Frequency Settings

R	FILTER MODE	POLES	f_{3dB} (f_S/2)	GAIN	GAIN (dB)	GAIN COMP (dB)	OVERALL GAIN (dB)
N/A	Bypass	N/A	N/A	1	0	0	0
63/64	Filter	1	0.004935	1	0.0681	0	0.0681
62/64	Filter	1	0.009796	1	0.1368	0	0.1368
61/64	Filter	1	0.014584	1	0.206	0	0.206
60/64	Filter	1	0.019303	1	0.2758	0	0.2758
59/64	Filter	1	0.023956	1	0.3461	0	0.3461
58/64	Filter	1	0.028544	15/16	0.417	-0.5606	-0.1436
57/64	Filter	1	0.033069	15/16	0.4885	-0.5606	-0.0721
56/64	Filter	1	0.037535	15/16	0.5606	-0.5606	0
55/64	Filter	1	0.041943	15/16	0.6333	-0.5606	0.0727
54/64	Filter	1	0.046294	15/16	0.7066	-0.5606	0.146
63/64	Filter	2	0.007403	1	0.1362	0	0.1362
62/64	Filter	2	0.014694	1	0.2736	0	0.2736
61/64	Filter	2	0.021876	15/16	0.412	-0.5606	-0.1486
60/64*	Filter	2	0.028955	15/16	0.5515	-0.5606	-0.0091
59/64	Filter	2	0.035934	15/16	0.6922	-0.5606	0.1316
58/64	Filter	2	0.042816	15/16	0.834	-0.5606	0.2734
57/64	Filter	2	0.049604	7/8	0.977	-1.1598	-0.1828
56/64	Filter	2	0.056303	7/8	1.1211	-1.1598	-0.0387
55/64	Filter	2	0.062915	7/8	1.2665	-1.1598	0.1067
54/64	Filter	2	0.069441	7/8	1.4131	-1.1598	0.2533

**Parts are factory trimmed with this setting. Programming can be changed.*

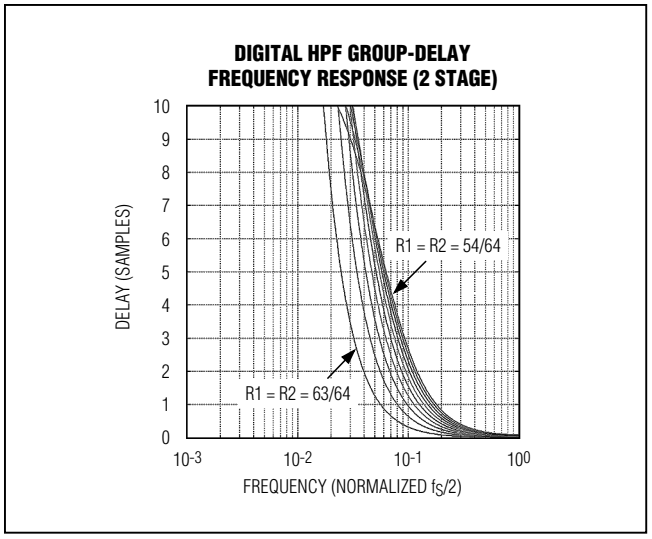


Figure 13. Digital HPF Magnitude Frequency Response (1 Stage)

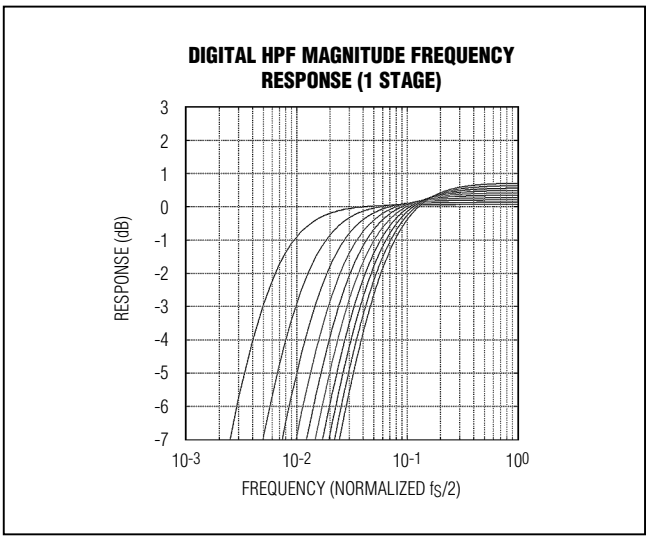


Figure 14. Digital HPF Magnitude Frequency Response (1 Stage) at Corner Frequency

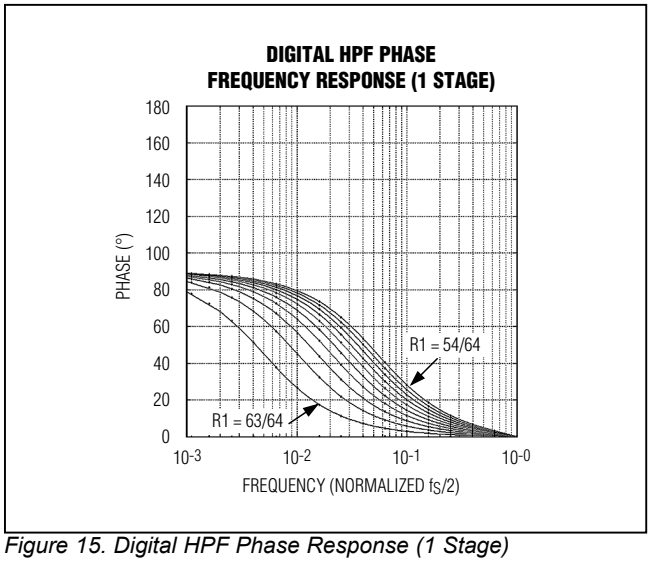


Figure 15. Digital HPF Phase Response (1 Stage)

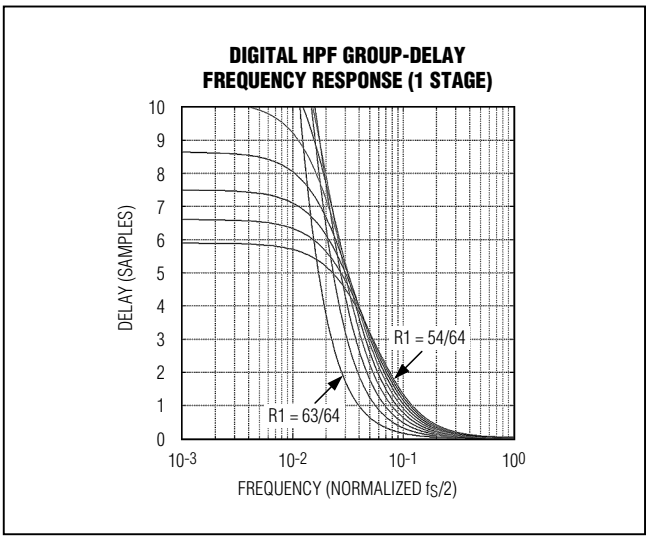


Figure 16. Digital HPF Group-Delay Frequency Response (1 Stage)

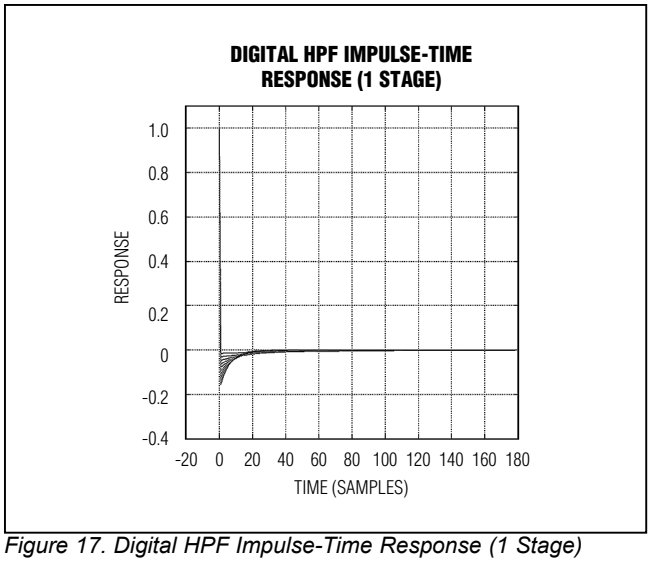


Figure 17. Digital HPF Impulse-Time Response (1 Stage)

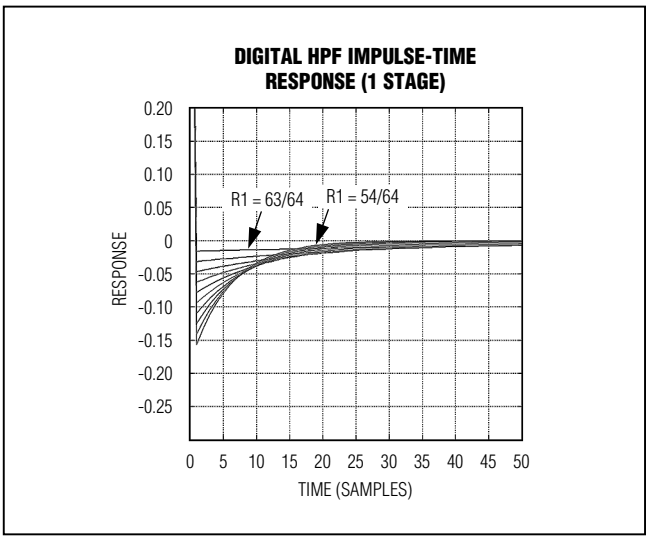


Figure 18. Digital HPF Impulse-Time Response Detailed Plot (1 Stage)

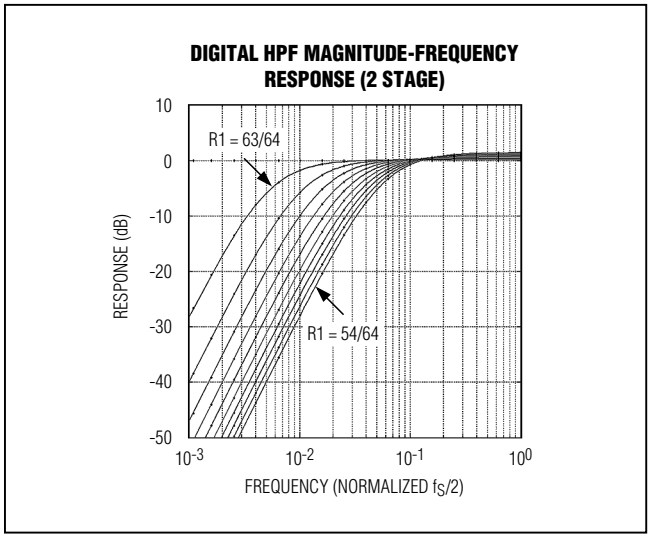


Figure 19. Digital HPF Magnitude Frequency Response (2 Stage)

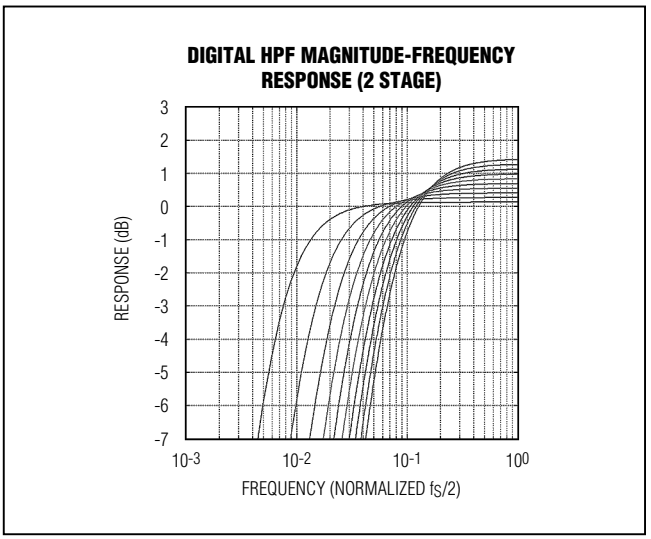


Figure 20. Digital HPF Magnitude Frequency Response (2 Stage) at Corner Frequency

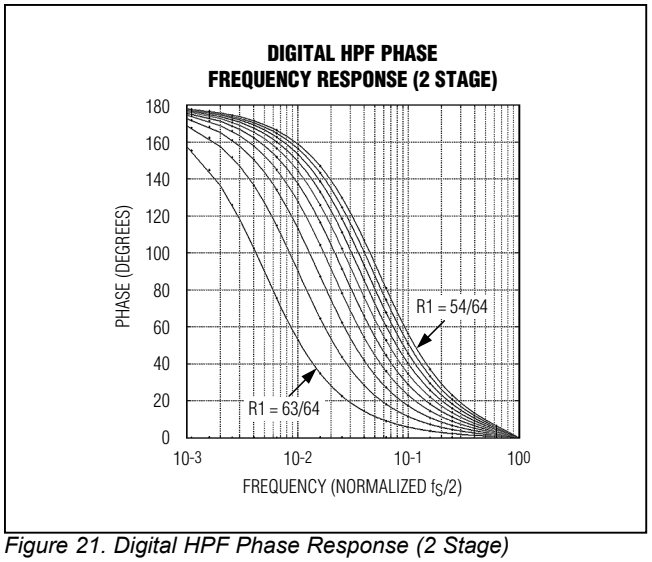


Figure 21. Digital HPF Phase Response (2 Stage)

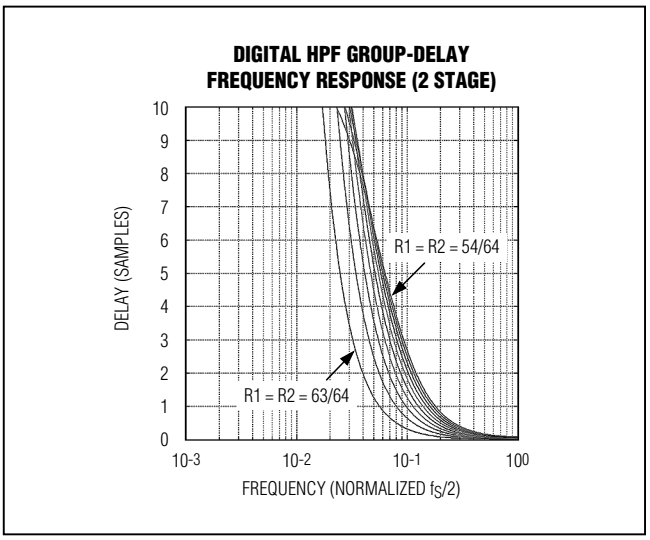


Figure 22. Digital HPF Group-Delay Frequency Response (2 Stage)

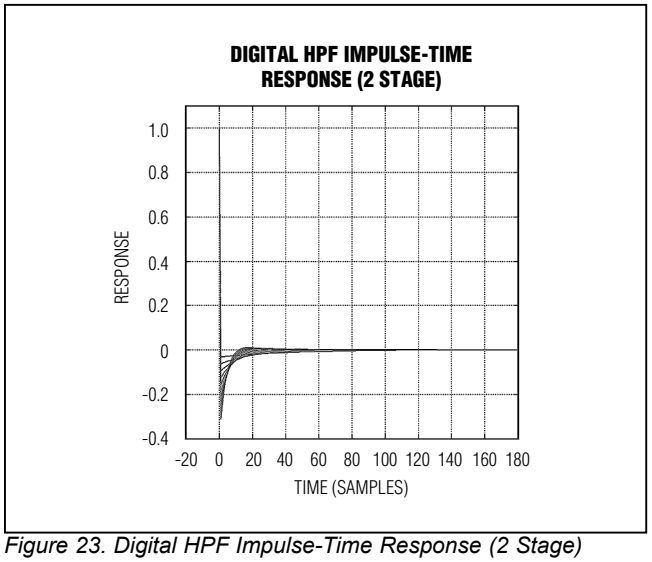


Figure 23. Digital HPF Impulse-Time Response (2 Stage)

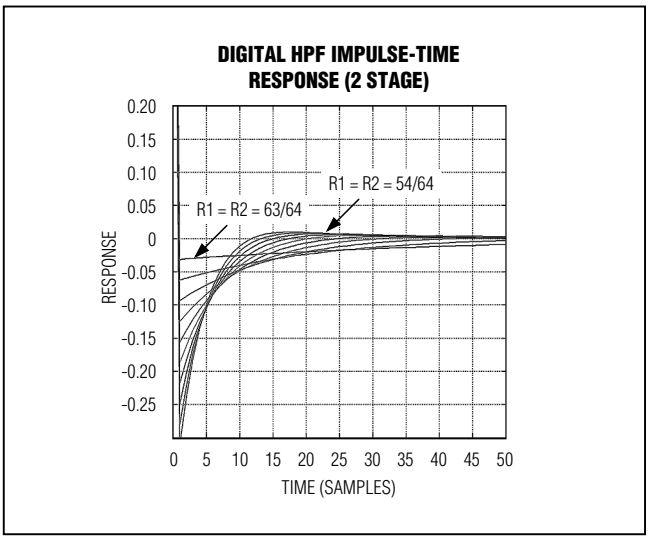


Figure 24. Digital HPF Impulse-Time Response Detailed Plot (2 Stage)

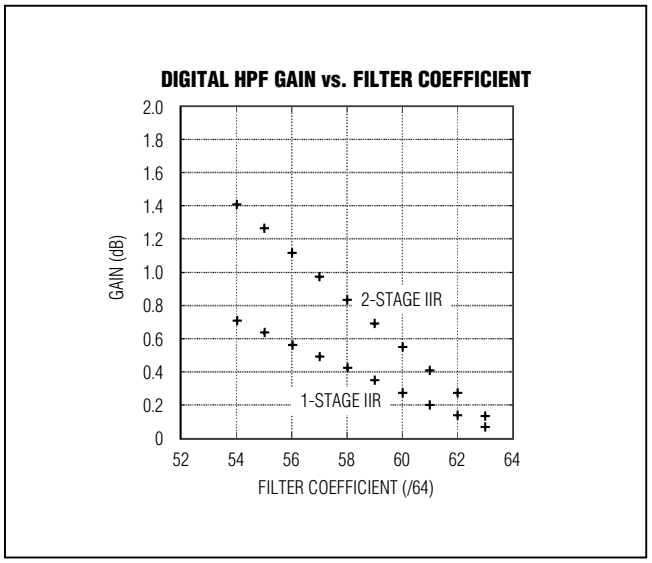


Figure 25. Digital HPF Gain vs. Filter Coefficient

System Timing Requirements

Figure 26 shows the relationship between the analog inputs, input clock, frame-alignment output, serial-clock output, and serial-data outputs. The differential ADC input signal is sampled on the rising edge of the applied clock signal (CLKIN+, CLKIN-), and the resulting data appears at the digital outputs 10.5 clock cycles later. Figure 27 provides a detailed, two-conversion timing diagram of the relationship between inputs and outputs.

Clock Output (CLKOUT+, CLKOUT-)

The ADC provides a differential clock output that consists of CLKOUT+ and CLKOUT-. As shown in Figure 28, the serial-output data is clocked out of the device on both edges of the clock output. The frequency of the output clock is six times (6x) the frequency of the input clock. The Output Data Format and Test Pattern/Digital HPF Select register (01h) allows the phase of the clock output to be adjusted relative to the output data frame (Table 9, Figure 30).

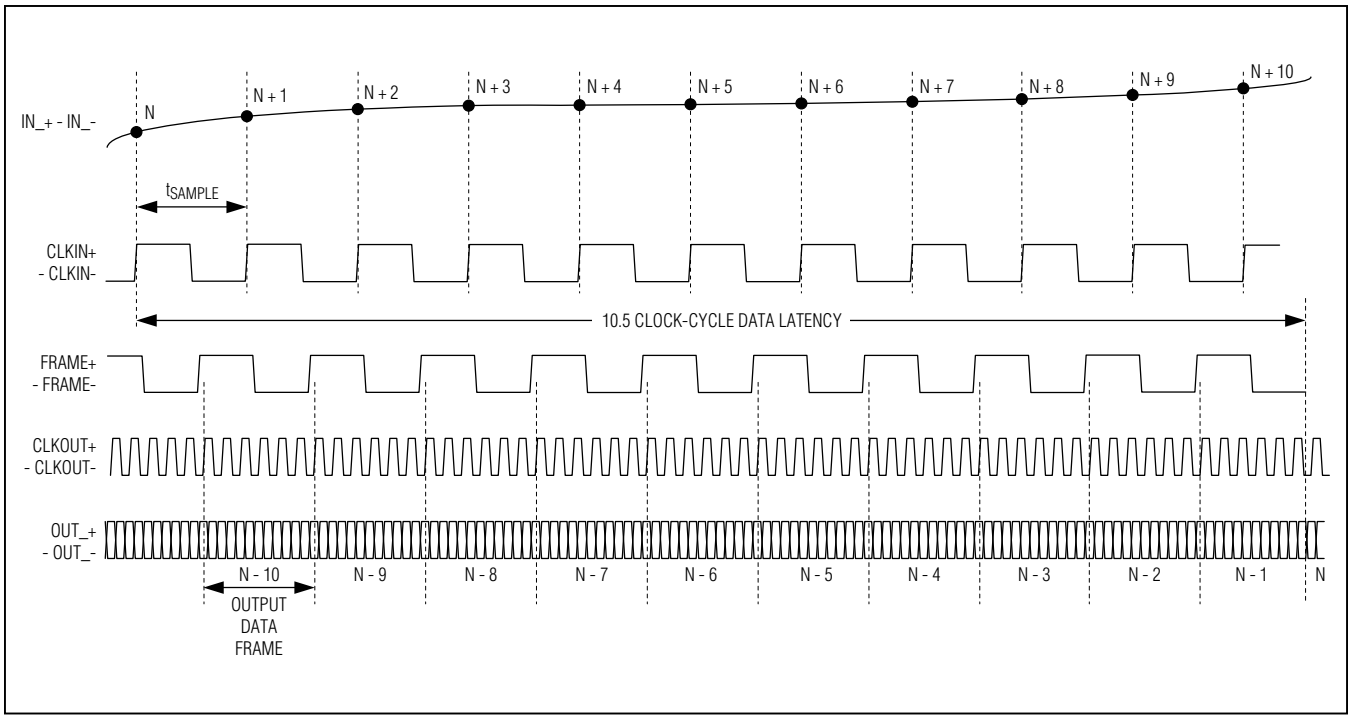


Figure 26. ADC Timing (Overall)

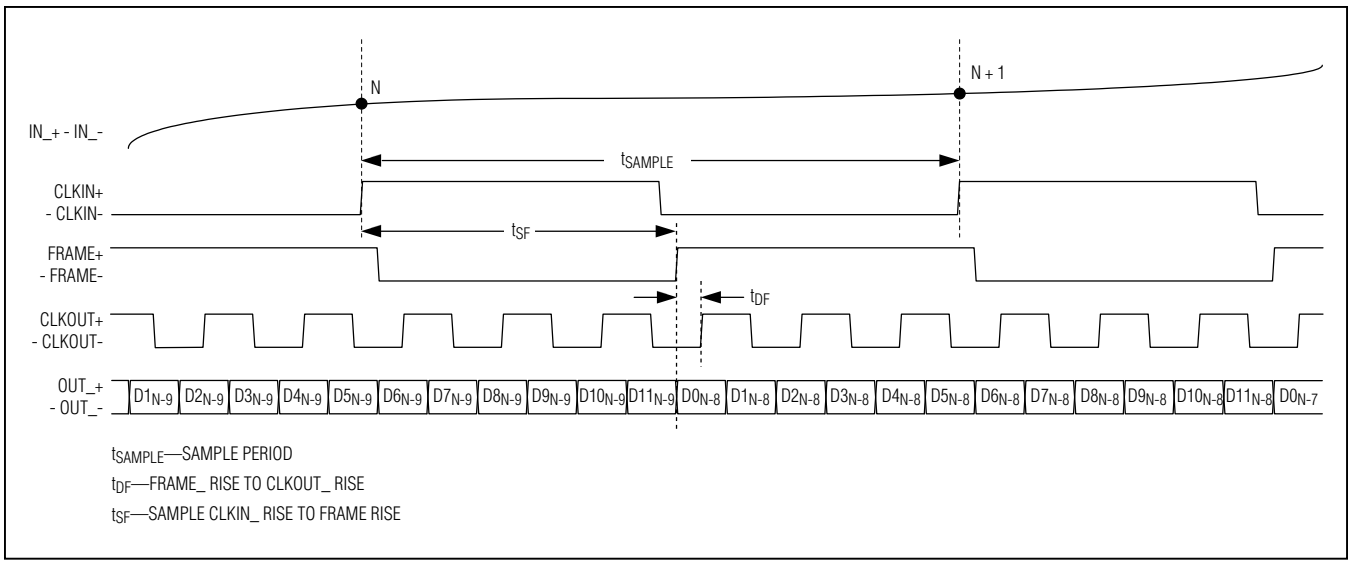


Figure 27. ADC Timing (Detail)

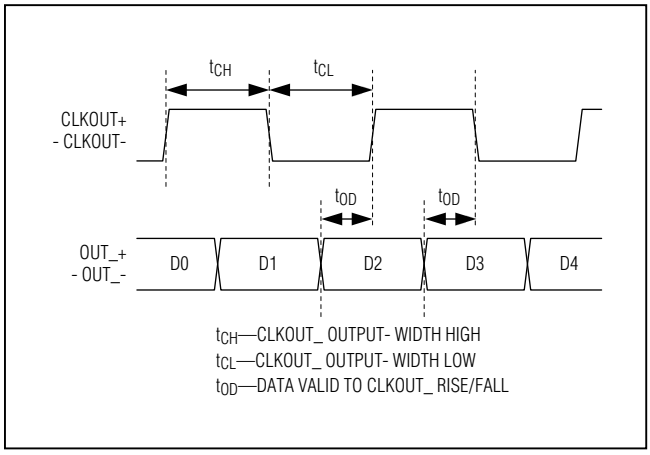


Figure 28. Serial Output Detailed Timing Diagram

Frame-Alignment Output (FRAME+, FRAME-)

The ADC provides a differential frame-alignment signal that consists of FRAME+ and FRAME-. As shown in Figure 27, the rising edge of the frame-alignment signal corresponds to the first bit (D0) of the 12-bit serial-data stream. The frequency of the frame-alignment signal is identical to the frequency of the input clock; however, the duty cycle varies depending on the input clock frequency.

Serial-Output Data (OUT_+, OUT_-)

The ADC provides conversion results through individual differential outputs consisting of OUT_+ and OUT_-. The results are valid 10.5 input clock cycles after a sample is taken. As shown in Figure 28, the output data is clocked out on both edges of the output clock, LSB (D0) first (by default). Figure 27 displays the detailed serial-output timing diagram.

Differential LVDS Digital Outputs

The ADC features programmable, fully differential LVDS digital outputs. By default, the 12-bit data output is transmitted LSB first, in offset binary format. The Output Data Format and Test Pattern/Digital HPF Select register (01h, Table 9) allows customization of the output bit order and data format. The output bit order can be reconfigured to transmit MSB first, and the output data format can be changed to two's complement. Table 10 contains full output data configuration details.

The LVDS outputs feature flexible programming options. First, the output common-mode voltage can be programmed from 0.6V to 1.2V (default) in 200mV steps (Table 17). Use the LVDS Output Driver Level register (02h, Table 13) to adjust the output common-mode voltage.

The LVDS output driver current is also fully programmable through the LVDS Output Driver Management register (03h, Table 18). By default, the output driver current is set to 3.5mA. The output driver current can be adjusted from 0.5mA to 7.5mA in 0.5mA steps (Table 19).

The LVDS output drivers also feature optional internal terminations that can be enabled and adjusted by the LVDS Output Driver Management register (03h, Table 18). By default, the internal output driver termination is disabled. See Table 20 for all possible configurations.

Output Driver Level Tests

The LVDS outputs (data, clock, and frame) can be configured to static logic-level test states through the LVDS Output Driver Level register (02h, Table 13). The complete list of settings for the static logic-level test states can be found in Table 14 to Table 16.

Data Output Test Patterns

The LVDS data outputs can be configured to output several different, recognizable test patterns. Test patterns are enabled and selected using the Output Data Format and Test Pattern/Digital HPF Select register (01h, Table 9). A complete list of test pattern options are listed in Table 11, and custom test pattern details can be found in the custom Test Pattern registers (07h, 08h, 09h) section (including Table 26, Table 29, and Table 30).

Power Management

The SHDN input is used to toggle between two power-management states. Power state 0 corresponds to SHDN = 0, while power state 1 corresponds to SHDN = 1. The PLL Sampling Rate and Power Management register (00h, Table 6) and the Channel Power Management registers (05h and 06h, Table 22 and Table 23) fully define each power-management state. By default, SHDN = 1 shuts down the device, and SHDN = 0 returns the ADCs to full-power operation. Use of the SHDN input is not required for power management.

For either state of SHDN, complete power-management flexibility is provided, including individual ADC channel power-management control, as well as the option of which reduced power-mode to utilize in each power state. The reduced-power modes available are sleep mode and nap mode. The device cannot enter either of these states unless no ADC channels are active in the current power state (Table 8).

In nap mode, the reference, duty-cycle equalizer, and clock-multiplier PLL circuits remain active for rapid wake-up time. In nap mode, the externally applied clock signal must remain active for the duty-cycle equalizer and PLL to remain locked. Typical wake-up time from nap mode is 2µs.

In sleep mode, all circuits are turned off except for the bandgap voltage-generation circuit. All registers retain previously programmed values during sleep mode. Typical wakeup time from sleep mode is 2ms (typ).

Power-On and Reset

The user-programmable register default settings and other factory-programmed settings are stored in a non-volatile memory. Upon device power-up, these values are loaded into the control registers. The operation occurs after the application of a valid supply voltage to AVDD and OVDD, and the presence of an input clock signal. The user-programmed register values are retained as long as the AVDD and OVDD voltages are applied.

A reset condition overwrites all user-programmed registers with the factory-default values. The reset condition occurs on power-up and can be initiated while powered with a software write command (write 5Ah) through the serial-port interface to the Special Function register (10h). The reset time is proportional to the ADC clock period and requires 415µs at 50Msps.

Power-Down and Low-Power (Nap) Mode and Channel Selection

The SHDN pin is a toggle switch between any two power-management states. In most cases, the SHDN = 0 state is on, and the SHDN = 1 state is off. However, complete flexibility is provided, allowing the user to toggle between active and nap, active and sleep, etc. Nap mode is defined as a reduced-power state with rapid wake-up time on the order of 2µs. Sleep mode is a very-low-power mode (~1mW) with a much longer wake-up time on the order of 2ms. The serial port and programmable registers remain active during nap and sleep modes.

CHn_ON_SHDN0 n = [1:8]

1 Channel n is on when the SHDN pin is low.

0 Channel n is off when the SHDN pin is low.

CHn_ON_SHDN1 n = [1:8]

1 Channel n is on when the SHDN pin is high.

0 Channel n is off when the SHDN pin is high.

ADC_NAP_SHDN0

1 ADC in nap mode when all channels are off, or the CWD pin is high and the SHDN pin is low.

0 ADC in sleep mode when all channels are off, or the CWD pin is high and the SHDN pin is low.

ADC_NAP_SHDN1

1 ADC in nap mode when all channels are off, or the CWD pin is high and the SHDN pin is high.

0 ADC in sleep mode when all channels are off, or the CWD pin is high and the SHDN pin is high.

AFE_NAP_SHDN0

1 AFE in nap mode when all channels are off and the SHDN pin is low.

0 AFE in sleep mode when all channels are off and the SHDN pin is low.

AFE_NAP_SHDN1

1 AFE in nap mode when all channels are off and the SHDN pin is high.

0 AFE in sleep mode when all channels are off and the SHDN pin is high.

3-Wire Serial Peripheral Interface (SPI)

The ADC operates as a slave device that sends and receives data through a 3-wire SPI interface. A master device must initiate all data transfers to and from the device. The device uses an active-low SPI chip-select input ($\overline{CS}$) to enable communication with timing controlled through the externally generated SPI clock input (SCLK). All data is sent and received through the bidirectional SPI data line (SDIO). The device has 16 user-programmable control registers and one special-function register, which are accessed and programmed through this interface.

SPI Communication Format

Figure 29 shows an ADC SPI communication cycle. All SPI communication cycles are made up of 2 bytes of data on SDIO and require 16 clock cycles on SCLK to be completed. To initiate an SPI read or write communication cycle, $\overline{CS}$ must first transition from a logic-high to a logic-low state. While $\overline{CS}$ remains low, serial data is clocked in from SDIO on rising edges of SCLK, and clocked out (for a read) on the falling edges of SCLK. When $\overline{CS}$ is high, the device does not respond to SCLK transitions, and no data is read from or written to SDIO. $\overline{CS}$ must transition back to logic-high after each read/write cycle is completed.

The first byte transmitted on SDIO is always provided by the master. The ADC (slave device) clocks in the data from SDIO on each rising edge of SCLK. The first bit received selects whether the communication cycle is a read or a write. Logic 1 selects a read cycle, while logic 0 selects a write cycle. The next 7 bits (MSB first) are the register address for the read or write cycle. The address can indicate any of the 16 user-programmable control registers (00h to 0Fh), or the special-function register (10h, write only). Attempting to read/write with any other address has no effect (Table 3).

The second byte on SDIO is sent to the ADC in the case of a write, or received from the ADC in the case of a read. For a write command, the device continues to clock in the data on SDIO on each rising edge of SCLK. In the case of a read command, the device writes data to SDIO on each falling edge of SCLK. The data byte is transmitted and received MSB first in both cases. The detailed SPI timing requirements are shown in Figure 29.

Output Clock Phase

CLKOUT_PHASE[1:0] default POR is 00. See Figure 30 for various output clock phase configurations.

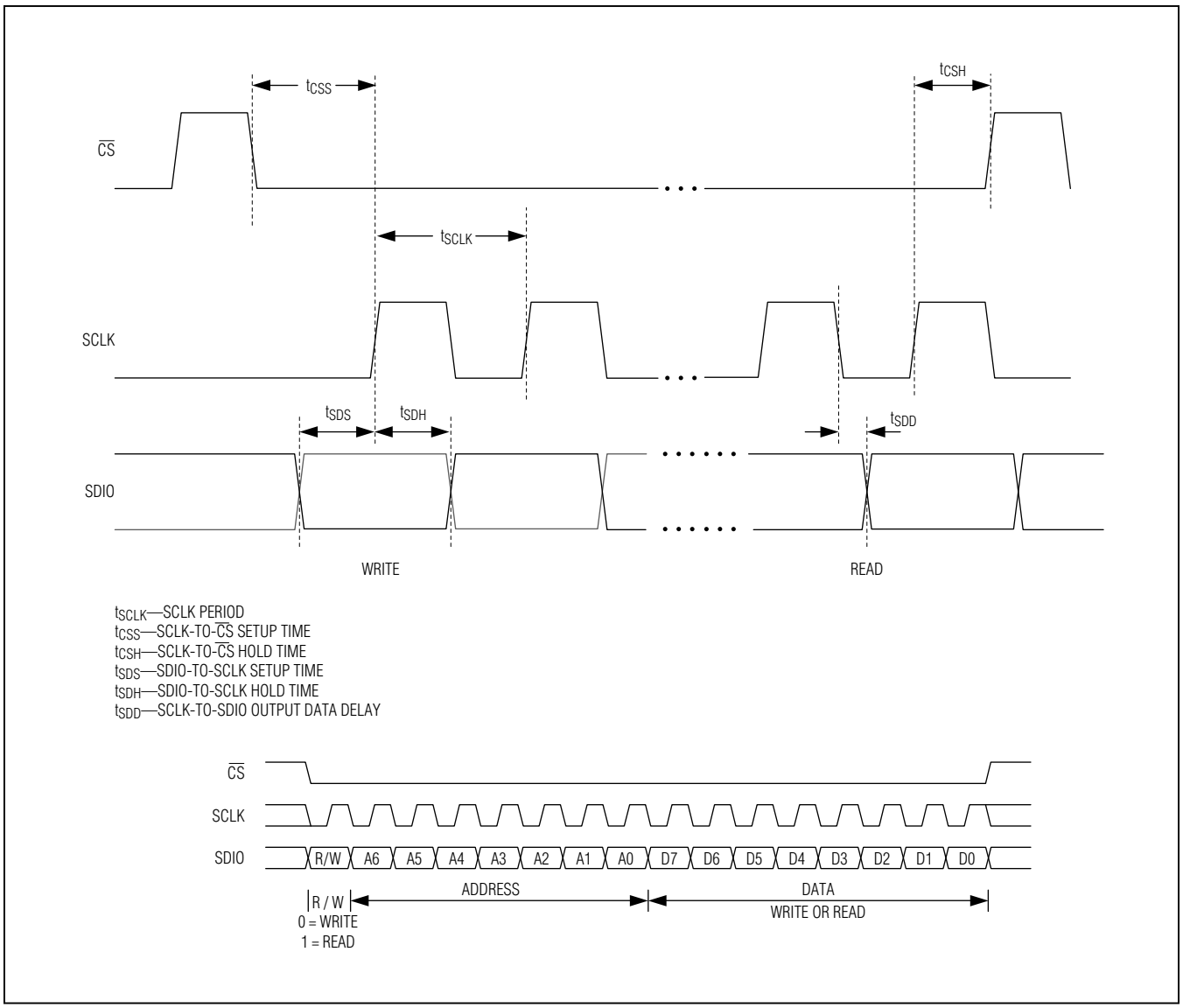


Figure 29. SPI Timing Diagram

Table 5. User-Programmable ADC Control Registers

ADDRESS	READ/WRITE	POR STATE	FUNCTION
00h	R/W	0001 0001	PLL Sampling Rate and Power Management
01h	R/W	0000 0000	Output Data Format and Test Pattern/Digital HPF Select
02h	R/W	0000 0000	LVDS Output Driver Level
03h	R/W	0000 0000	LVDS Output Driver Management
04h	R/W	0000 0000	ADC CLKIN Control
05h	R/W	1111 1111	Channel Power Management: SHDN0
06h	R/W	0000 0000	Channel Power Management: SHDN1
07h	R/W	0100 0100	Digital HPF 1 and 2: -3dB Cutoff/Custom Test Patterns 1
08h	R/W	0101 0110	Digital HPF 1 and 2: ATENuation/Custom Test Patterns 2
09h	R/W	0101 1010	Custom Test Patterns 2 and 1 (4 Most Significant Bits)
0Ah	R/W	0101 1100	AFE Settings
0Bh	R/W	0000 0000	CW Beamformer 1
0Ch	R/W	0000 0000	CW Beamformer 2
0Dh	R/W	0000 0000	CW Beamformer 3
0Eh	R/W	0000 0000	CW Beamformer 4
0Fh	R/W	0000 0000	CW Beamformer 5
10h	R/W	N/A	Special Function

Table 6. PLL Sampling Rate and Power Management (00h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	PLL[2:0]			AFE_NAP_SHDN1	AFE_NAP_SHDN0	ADC_NAP_SHDN1	ADC_NAP_SHDN0

Table 7. PLL Frequency-Control Settings (00h[6:4])

CLOCK MULTIPLIER SETTING			MINIMUM SAMPLING FREQUENCY (MHz)	MAXIMUM SAMPLING FREQUENCY (MHz)
PLL[2]	PLL[1]	PLL[0]		
0	0	0	Not used	
0	0	1	39	50
0	1	0	28.5	39
0	1	1	25	28.8
1	X	X	Not used	

X = Don't care.

Table 8. Power-Management Programming

PINS		REGISTERS						DESCRIPTION
SHDN	CWD	CHn_ON_SHDN0 n = [1:8]	CHn_ON_SHDN1 n = [1:8]	ADC_NAP_SHDN0	ADC_NAP_SHDN1	AFE_NAP_SHDN0	AFE_NAP_SHDN1	
DEFAULT REGISTER MODES								
0	0	11111111	00000000	0	1	0	1	8 channels active (VGA mode)
0	1	11111111	00000000	0	1	0	1	CW Doppler mode (ADC in nap mode)
1	0	11111111	00000000	0	1	0	1	Nap mode (ADC and AFE)
1	1	11111111	00000000	0	1	0	1	CW Doppler mode (ADC in nap mode)
PROGRAMMED REGISTER MODES								
0	0	Not all zero	XXXXXXXX	X	X	X	X	1 or more channels active (VGA mode)
0	0	00000000	XXXXXXXX	0	X	0	X	Sleep mode (ADC and AFE)
0	0	00000000	XXXXXXXX	0	X	1	X	ADC sleep/AFE nap
0	0	00000000	XXXXXXXX	1	X	0	X	ADC nap/AFE sleep
0	0	00000000	XXXXXXXX	1	X	1	X	Nap mode (ADC and AFE)
0	1	XXXXXXXX	XXXXXXXX	0	X	X	X	CW Doppler mode (ADC in sleep mode)
0	1	XXXXXXXX	XXXXXXXX	1	X	X	X	CW Doppler mode (ADC in nap mode)
1	0	XXXXXXXX	Not all zero	X	X	X	X	1 or more channels active (VGA mode)
1	0	XXXXXXXX	00000000	X	0	X	0	Sleep mode (ADC and AFE)
1	0	XXXXXXXX	00000000	X	0	X	1	ADC sleep/AFE nap
1	0	XXXXXXXX	00000000	X	1	X	0	ADC nap/AFE sleep
1	0	XXXXXXXX	00000000	X	1	X	1	Nap mode (ADC and AFE)
1	1	XXXXXXXX	XXXXXXXX	X	0	X	X	CW Doppler mode (ADC in sleep mode)
1	1	XXXXXXXX	XXXXXXXX	X	1	X	X	CW Doppler mode (ADC in nap mode)

X = Don't care.

Table 9. Output Data Format and Test Pattern/Digital HPF Select (01h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TEST_PATTERN[2:0]			TEST_DATA	CLKOUT_PHASE[1:0]		DATA_FORMAT	BIT_ORDER

Table 10. LVDS Output Data Format Programming (01h[1:0])

DATA_FORMAT	BIT_ORDER	LVDS OUTPUT DATA FORMAT
0	0	Offset binary, LSB first (default
0	1	Offset binary, MSB first
1	0	Two's complement, LSB first
1	1	Two's complement, MSB first

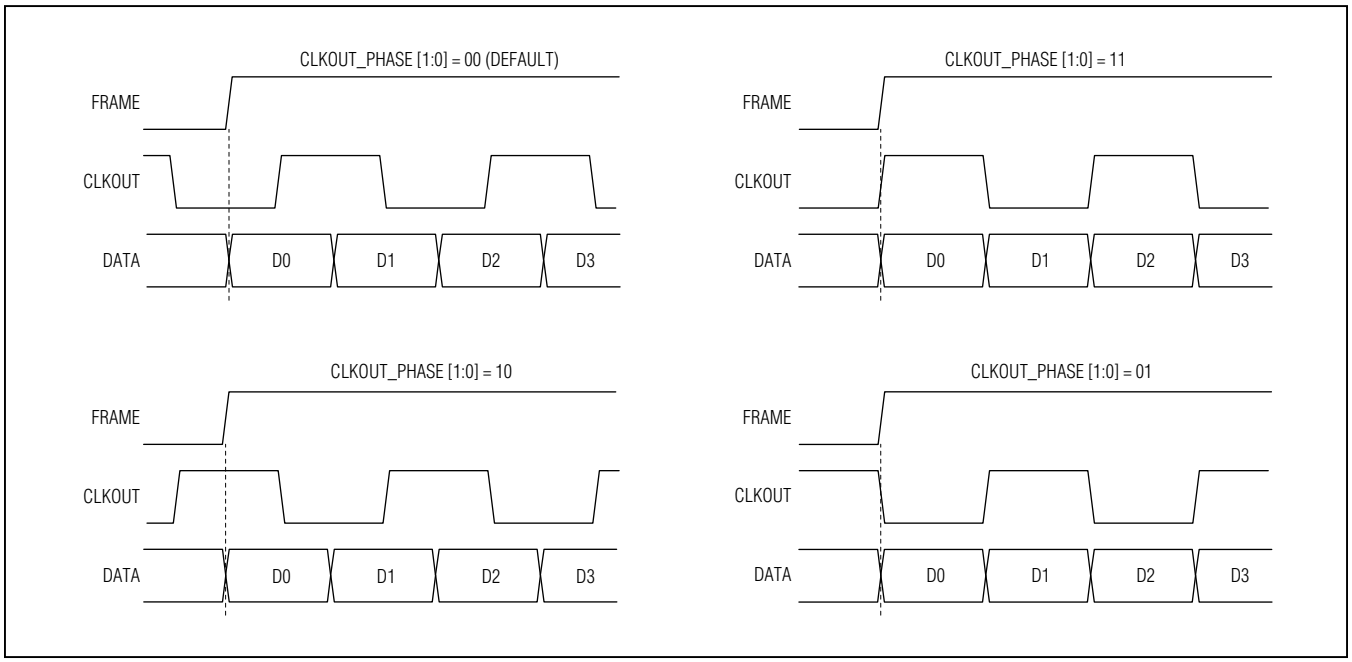


Figure 30. Output Clock Phase

Custom Test Pattern

When custom test pattern is selected (TEST_PATTERN[2:0] = 010), the output alternates between BITS_CUSTOM1[11:0] and BITS_CUSTOM2[11:0]. If a single repeating word is desired, program BITS_CUSTOM2[11:0] to the same value as BITS_CUSTOM1[11:0].

Table 11. Test Pattern Programming and Digital Highpass Filter Selection

TEST_DATA	TEST_PATTERN[2:0]			TEST PATTERN FORMAT
0	X	X	X	Disabled, normal operation with digital HPF selected (default)
1	0	0	0	Data skew (010101010101), repeats every frame
1	0	0	1	Data sync (111111000000), repeats every frame
1	0	1	0	Custom test pattern, repeats every 2 frames
1	0	1	1	Ramping pattern from 0 to 4095 (repeats)
1	1	0	0	Pseudorandom data pattern, short sequence (2^9)
1	1	0	1	Pseudorandom data pattern, long sequence (2^{23})
1	1	1	X	Not used

X = Don't care.

Table 12. Pseudorandom Data Test Pattern

SEQUENCE	INITIAL VALUE	FIRST 3 SAMPLES
Short (2^9)	0x0df	0xdf9, 0x353, 0x301
Long (2^{23})	0x29b80a	0x591, 0xfd7, 0x0a3

Note: *When custom test pattern is selected (TEST_PATTERN[2:0] = 100) the output is a short (2^9) PN sequence. A long (2^{23}) sequence output is provided when TEST_PATTERN[2:0] = 101.*

Table 13. LVDS Output Driver Level (02h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LVDS_CM[1:0]		TEST_FRAME_LEVEL[1:0]		TEST_CLKOUT_LEVEL[1:0]		TEST_DATA_LEVEL[1:0]	

Table 14. Test Data (OUT_) Level Programming

TEST_DATA_LEVEL[1:0]		DATA (OUT_) OUTPUT
X	0	Normal data output
0	1	Output low (static)
1	1	Output high (static)

X = Don't care.

Table 15. Test CLKOUT_ Level Programming

TEST_CLKOUT_LEVEL[1:0]		CLKOUT_ OUTPUT
X	0	Normal CLKOUT_ output
0	1	Output low (static)
1	1	Output high (static)

X = Don't care.

Table 16. Test FRAME Level Programming

TEST_FRAME_LEVEL[1:0]		FRAME OUTPUT
X	0	Normal FRAME output
0	1	Output low (static)
1	1	Output high (static)

X = Don't care.

Table 17. LVDS Output Common-Mode Voltage Adjustment

LVDS_CM[1:0]		LVDS OUTPUT COMMON-MODE VOLTAGE (V)
0	0	1.2 (default)
0	1	1.0
1	0	0.8
1	1	0.6

Table 18. LVDS Output Driver Management (03h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	LVDS_TERM[2:0]			LVDS_IADJ[3:0]			

Table 19. LVDS Output Drive Current Configuration

LVDS_IADJ[3:0]				LVDS CURRENT (mA)
0	0	0	0	3.5mA, 350mV at 100Ω (default)
0	0	0	1	0.5
0	0	1	0	1.0
0	0	1	1	1.5
0	1	0	0	2.0
0	1	0	1	2.5
0	1	1	0	3.0
0	1	1	1	3.5
1	0	0	0	4.0
1	0	0	1	4.5
1	0	1	0	5.0
1	0	1	1	5.5
1	1	0	0	6.0
1	1	0	1	6.5
1	1	1	0	7.0
1	1	1	1	7.5

Note: *Selectable LVDS drive current fully selectable from 0.5mA to 7.5mA in 0.5mA increments (3.5mA default). Supports ANSI-644 and IEEE 1596.3.*

Table 20. LVDS Output Driver Internal Termination Configuration

LVDS_TERM[2:0]			LVDS INTERNAL TERMINATION (Ω)
0	0	0	—
0	0	1	800
0	1	0	400
0	1	1	267
1	0	0	200
1	0	1	160
1	1	0	133
1	1	1	100

Table 21. CLKIN Termination Control (04h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	CLKIN_TERM	—	—	—	0*

Always program this bit to 0.

Clock Input Termination

CLKIN_TERM = 0: 100Ω not selected.

CLKIN_TERM = 1: Switches in 100Ω across differential clock inputs.

Table 22. Channel Power Management: SHDN0 (05h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CH8_SHDN0	CH7_SHDN0	CH6_SHDN0	CH5_SHDN0	CH4_SHDN0	CH3_SHDN0	CH2_SHDN0	CH1_SHDN0

Table 23. Channel Power Management: SHDN1 (06h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CH8_SHDN1	CH7_SHDN1	CH6_SHDN1	CH5_SHDN1	CH4_SHDN1	CH3_SHDN1	CH2_SHDN1	CH1_SHDN1

Table 24. Digital Highpass Filter Control Coefficients (07h; If TEST_DATA 01[4]) = 0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HPF2[3:0]				HPF1[3:0]			

Table 25. Digital Highpass Filter Configuration

HPF1[3:0], HPF2[3:0]				R1/R2	FILTER MODE
0	0	0	0	N/A	Bypass
0	0	0	1	63/64	Filter; f_{3dB} = 0.004935, $f_S/2$
0	0	1	0	62/64	Filter; f_{3dB} = 0.009796, $f_S/2$
0	0	1	1	61/64	Filter; f_{3dB} = 0.014584, $f_S/2$
0	1	0	0	60/64	Filter; f_{3dB} = 0.019303, $f_S/2$
0	1	0	1	59/64	Filter; f_{3dB} = 0.023956, $f_S/2$
0	1	1	0	58/64	Filter; f_{3dB} = 0.028544, $f_S/2$
0	1	1	1	57/64	Filter; f_{3dB} = 0.033069, $f_S/2$
1	0	0	0	56/64	Filter; f_{3dB} = 0.037535, $f_S/2$
1	0	0	1	55/64	Filter; f_{3dB} = 0.041943, $f_S/2$
1	0	1	0	54/64	Filter; f_{3dB} = 0.046294, $f_S/2$
1	0	1	1	—	Bypass
1	1	0	0	—	Bypass
1	1	0	1	—	Bypass
1	1	1	0	—	Bypass
1	1	1	1	—	Bypass

Table 26. Custom Test Pattern 1 (07h; If TEST_DATA 01[4]) = 1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BITS_CUSTOM1[7:0]							

Table 27. Digital Highpass Filter Attenuation (08h; If TEST_DATA 01[4]) = 0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	—	—	—	ATEN[1:0]	

Table 28. Digital Highpass Filter Attenuation

ATEN[1:0]		GAIN	GAIN (dB)
0	0	1	0
0	1	1	0
1	0	15/16	-0.58
1	1	7/8	-1.16

Table 29. Custom Test Pattern 2 (08h; If TEST_DATA 01[4]) = 1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BITS_CUSTOM2[7:0]							

Table 30. Custom Test Pattern 3 (09h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BITS_CUSTOM2[11:8]				BITS_CUSTOM1[11:8]			

Table 31. AFE Settings (0Ah)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AFE_RIN[0:2]			AFE_LNA_GAIN	AFE_BW[0:1]		CWD_POWER_MODE	AFE_OCLAMP

Table 32. AFE Input Impedance and LNA Gain Control

AFE_LNA_GAIN	AFE_RIN[0:2]			INPUT RESISTANCE (Ω)	LNA GAIN (dB)
0	0	0	0	100	12.5
0	1	0	0	200	12.5
0	0	1	0	400	12.5
0	1	1	0	1000	12.5
0	X	X	1	External R	12.5
1	0	0	0	50	18.5
1	1	0	0	100	18.5
1	0	1	0	200	18.5
1	1	1	0	500	18.5
1	X	X	1	External R	18.5

X = Don't care.

Table 33. AFE AAF Filter Bandwidth Control

AFE_BW[0:1]		BANDWIDTH (MHz)
0	0	9
0	1	10
1	0	15
1	1	18

Table 34. CWD Power Mode

CWD_POWER_MODE	CWD POWER MODE
0	Full power (default, nominal)
1	Low power

Table 35. VGA Output Clamp Control

AFE_OCLAMP	VGA OUTPUT CLAMP
0	No clamp (default, nominal)
1	Clamp active

Table 36. CW Beamformer 1 (0Bh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH2[1:3]			CW_SHDN_CH1	CW_PHASE_CH1[0:3]			

Table 37. CW Beamformer 2 (0Ch)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH4[3]	CW_SHDN_CH3	CW_PHASE_CH3[0:3]				CW_SHDN_CH2	CW_PHASE_CH2[0]

Table 38. CW Beamformer 3 (0Dh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH5[0:3]				CW_S HDN_CH4	CW_PHASE_CH4[0:2]		

Table 39. CW Beamformer 4 (0Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH7[2:3]		CW_SHDN_CH6	CW_PHASE_CH6[0:3]				CW_SHDN_CH5

Table 40. CW Beamformer 5 (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_SHDN_CH8	CW_PHASE_CH8[0:3]				CW_SHDN_CH7	CW_PHASE_CH7[0:1]	

Table 41. Phase Rotation Bit Weight

CW_PHASE_CHn[0:3]				PHASE
-22.5	-180	-90	-45	Degrees

Table 42. Phase Rotation Summary

CW_PHASE_CHn[0:3]				PHASE (DEGREES)
-22.5	-180	-90	-45	
0	0	0	0	0
0	0	0	1	337.5
0	0	1	0	180
0	0	1	1	157.5
0	1	0	0	270
0	1	0	1	247.5
0	1	1	0	90
0	1	1	1	67.5
1	0	0	0	315
1	0	0	1	292.5
1	0	1	0	135
1	0	1	1	112.5
1	1	0	0	225
1	1	0	1	202.5
1	1	1	0	45
1	1	1	1	22.5

CW Doppler Mode Control

CW_SHDN_CHn is set to 0 in normal operation (default). Set it to 1 for power-down channel n when in CW Doppler mode.

Note: The transfer data to AFE procedure described in the AFE Programming and Data Transfer section should be performed twice when setting any CW_SHDN_CHn bits from 0 to 1 to enable a CW Doppler channel(s). This procedure only applies to the CW_SHDN_CHn bits; all other bits are transferred to the AFE in a single operation.

Table 43. Special Function Register (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS7	STATUS6	STATUS5	STATUS4	STATUS3	STATUS2	STATUS1	STATUS0

Table 44. Status Byte (Reads from 10h)

STATUS BIT NO.	READ VALUE	DESCRIPTION
7	0	Reserved
6	0	1 = AFE load in progress; 0 = load complete
5	0 or 1	1 = ROM read in progress
4	0 or 1	1 = ROM read completed, and register data is valid (checksum ok)
3	0	Reserved
2	1	Reserved
1	0 or 1	Reserved
0	0 or 1	1 = Duty-cycle equalizer DLL is locked

Table 45. SPI Commands (Writes to 10h)

COMMAND	WRITE DATA	DESCRIPTION
Soft Reset	5Ah	Initiates software reset
Transfer data to AFE	AEh	Initiates transfer of data in ADC registers 0Ah to 0Fh to AFE

Note: *All commands are issued by writing SPI address 10h.*

Soft Reset

Software reset allows the user to reset the part through writes to the serial port. A soft reset can be performed by writing the reset code 5Ah to address 10h. Upon initiation of soft reset, the fuse memory is read and loaded into the SPI registers. See the 3-Wire Serial Peripheral Interface (SPI) section for further detail. The reset is self-clearing, subsequent serial-port write(s) are not needed to clear the reset condition.

AFE Programming and Data Transfer

The internal analog front-end (AFE) and ADC are programmed through a common serial-port interface. There are 48 user-programmable bits in the ADC that store AFE control information. These bits are written to registers 0Ah to 0Fh in the ADC, and transferred to the AFE shift registers when AEh is written to register 10h. The user must provide at least 50 clock cycles on SCLK after this control word is written to complete the data transfer to the AFE. To verify that the data has been transferred to the AFE, poll address 10h until bit 6 is 0. As a final step, write 00h to address 10h. Changes in registers 0Ah to 0Fh do not take effect in the AFE until this transfer is complete.

CWD Beamformer Programming and Clocking

Programming of the CWD beamformer occurs in the following sequence:

1) During normal CWD mode, the mixer clock (LO+, LO-) is on. LOON is high.
2) Shut off the mixer clock (LO+, LO-) or pull LOON low to start the programming sequence.
3) Write the phase and channel shutdown information into the proper control registers.
4) Transfer the phase information from the control registers to the AFE (see above) and wait for the write to complete. Turn on the mixer clock and set LOON to high to start beamforming (the AFE shift registers can also be written with the mixer clock running and LOON set low). If turning on the mixer clock source, the clock must turn on such that it starts at the beginning of a mixer clock cycle. A narrow glitch on the mixer clock is not acceptable and could cause metastability in the I/Q phase dividers. If using the LOON control to turn on the mixer clock, the LOON signal must be synchronous to the LO clock, and it must meet the minimum setup time specification.

5) To program new CWD phase information, turn off the mixer clock and/or set LOON low and repeat steps 1–5.

6) For switching between VGA and CWD modes without reprogramming the SPI registers (fast mode switching): When changing from CWD mode to VGA mode, nothing needs to be done to maintain the AFE programming settings. When switching from VGA mode to CWD mode, the user must provide a $\overline{CS}$ pulse after the CWD pin goes high to initialize the CWD beamformer phase registers. This pulse must occur 100ns or more after the rising edge of the CWD pin, and must be at least 80ns in width.

Applications Information

Layout Concerns

The device provides several GND connections underneath package for improved thermal performance. Do not run traces under the package to avoid possible short circuits. To aid heat dissipation, connect GND to similarly sized pads on the component side of the PCB. These pads should be connected through to the solder-side copper by several plated holes to a large heat-spreading copper area to conduct heat away from the device.

The devices' high-speed pulser requires low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay particular attention to minimize trace lengths and use sufficient trace width to reduce inductance. Use of surface-mount components is recommended.

Power-Supply Sequencing

When using the embedded FPSs (TEN = low), the devices do not require any power-up/power-down sequence. When external FPSs are used (TEN = high), the conditions $V_{TVGP\_}$ > (V_{TVEE} - 0.6V) and $V_{TVGN\_}$ < (V_{TVCC} + 0.6V) must be satisfied during the entire power-up/power-down transients (see the Electrical Characteristics tables).

Internal ESD protection diodes impose certain restrictions on the power-supply sequence. The V_{CC5} supply should always be greater than the V_{CC3} supply, otherwise, excessive current can flow and cause damage. The AVDD and OVDD supplies are internally connected through anti-parallel diodes and should always be within 0.3V of each other, otherwise, excessive current can flow and cause damage. The 11V supply used to pulll up the CI+/- and CQ+/- pins must always be greater than the V_{CC5} supply, otherwise, excessive current can flow and cause damage.

Ultasound-Specific IMD3 Specification

Unlike typical communications applications, the two input tones are not equal in magnitude for the ultrasound-specific IMD3 two-tone specification. In this measurement, f_1 represents reflections from tissue and f_2 represents reflections from blood. The latter reflections are typically 25dB lower in magnitude. IM3 performance for the device is measured with the smaller tone at -25dBc in order to more accurately resolve the small IM3 products over the thermal noise floor. The IMD3 product of interest (f_1 - (f_2 - f_1)) presents itself as an undesired Doppler error signal in ultrasound applications (see Figure 31).

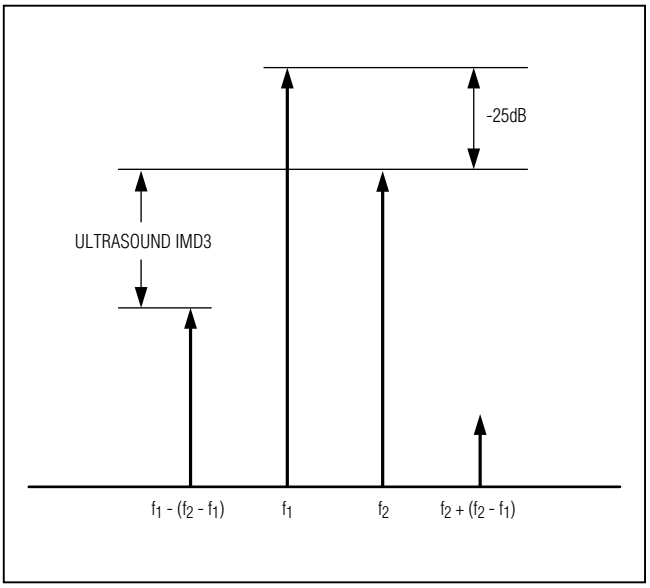


Figure 31. Ultrasound-Specific IMD3

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2082CXD+	0°C to +70°C	336 CSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BCDMOS/BiCMOS/CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
336 CSBGA	X336023M+3	**21-0639**	**90-0388**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—

