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# FCP150N65F

## N-Channel SuperFET® II FRFET® MOSFET

650 V, 24 A, 150 mΩ

### Features

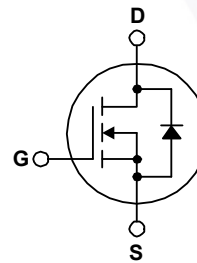
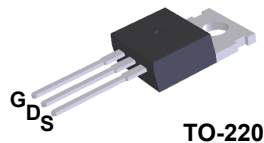
- 700 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 133\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 72\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 361\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- LCD / LED / PDP TV
- Telecom / Server Power Supplies
- Solar Inverter
- AC - DC Power Supply

### Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCP150N65F	Unit
$V_{DSS}$	Drain to Source Voltage	650	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC ( $f > 1\text{ Hz}$ )	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	24
		- Continuous ( $T_C = 100^\circ\text{C}$ )	14.9
$I_{DM}$	Drain Current	- Pulsed (Note 1)	72
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	663	mJ
$I_{AR}$	Avalanche Current (Note 1)	4.7	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	2.98	mJ
$dv/dt$	MOSFET $dv/dt$	100	V/ns
	Peak Diode Recovery $dv/dt$ (Note 3)	50	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	298
		- Derate Above $25^\circ\text{C}$	2.38
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCP150N65F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.42	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

FCP150N65F — N-Channel SuperFET® II FRFET® MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP150N65F	FCP150N65F	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	650	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	700	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.72	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	86	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 2.4\text{ mA}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	-	133	150	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 12\text{ A}$	-	22	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	2810	3737	pF
$C_{oss}$	Output Capacitance		-	91	121	pF
$C_{riss}$	Reverse Transfer Capacitance		-	0.77	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	54	-	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	361	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 12\text{ A}, V_{GS} = 10\text{ V}$	-	72	94	nC
$Q_{gs}$	Gate to Source Gate Charge		-	15	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	31	-
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.69	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 12\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\text{ }\Omega$	-	28	66	ns	
$t_r$	Turn-On Rise Time		-	15	40	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	-	73	156	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	6	22	ns

### Drain-Source Diode Characteristics

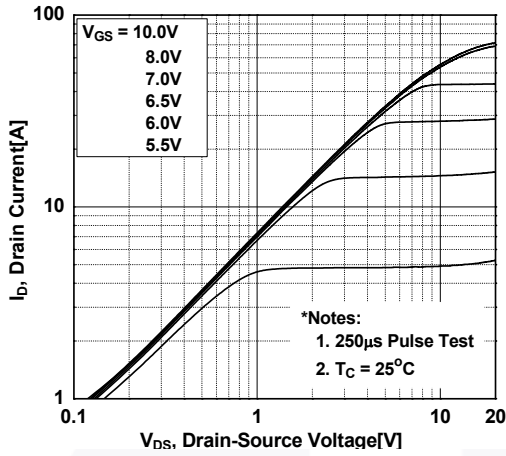
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	24	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	72	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 12\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 12\text{ A}$	-	123	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	597	-	nC

#### Notes:

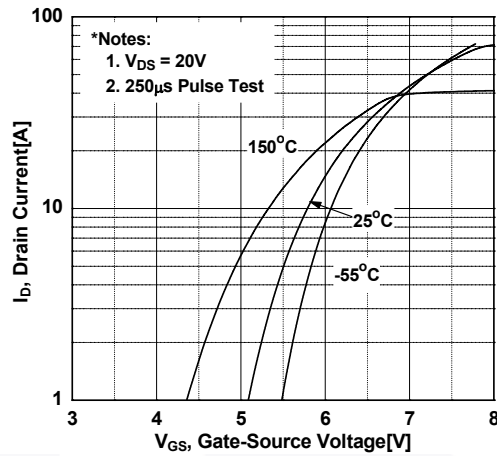
1. Repetitive rating: pulse width limited by maximum junction temperature.
2.  $I_{AS} = 4.7\text{ A}, R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 12\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$ , Starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Performance Characteristics

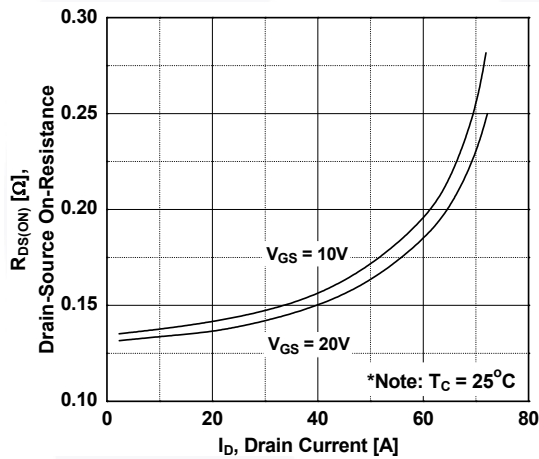
**Figure 1. On-Region Characteristics**



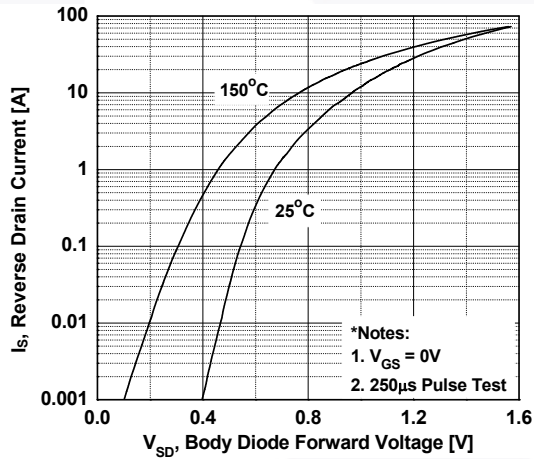
**Figure 2. Transfer Characteristics**



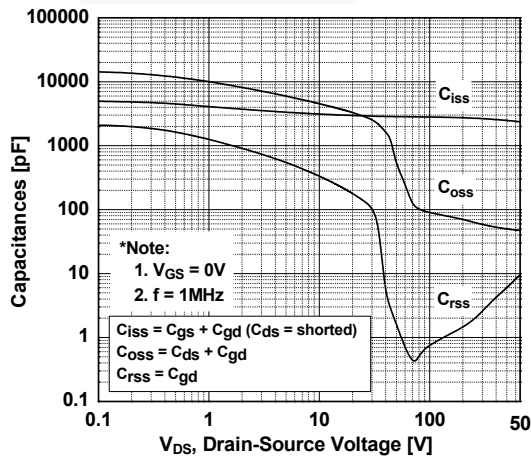
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



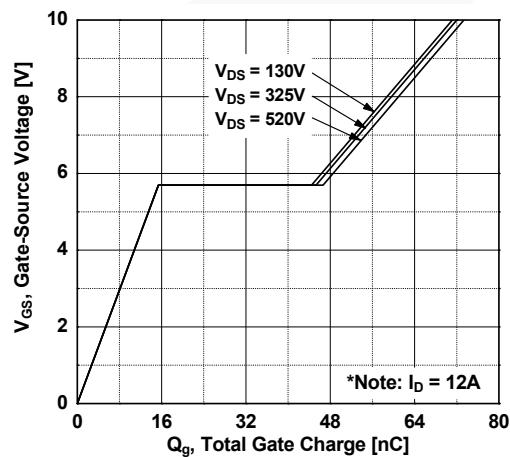
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

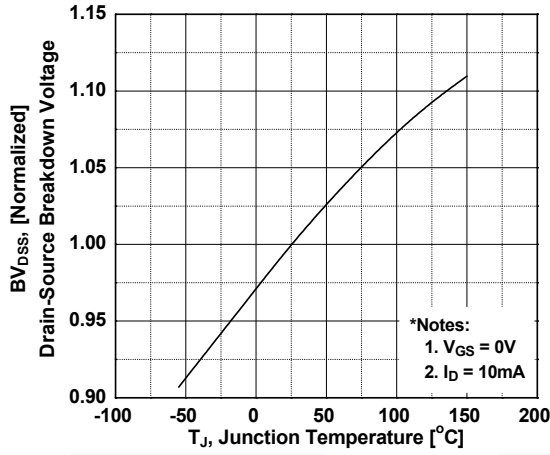


Figure 8. On-Resistance Variation vs. Temperature

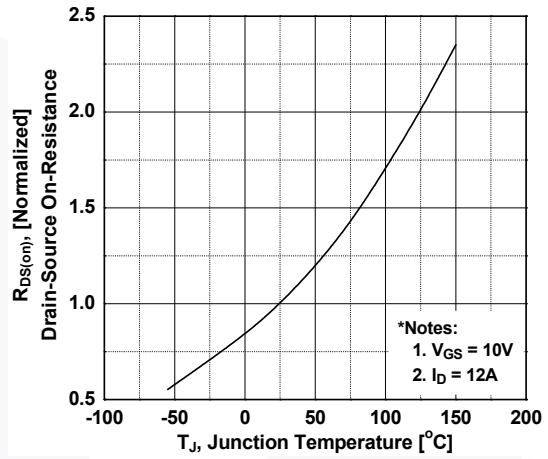


Figure 9. Maximum Safe Operating Area

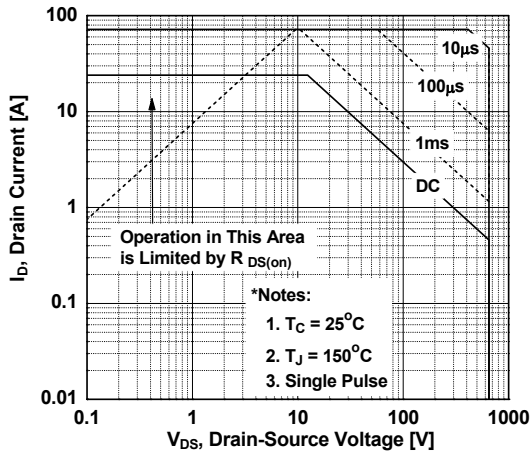


Figure 10. Maximum Drain Current vs. Case Temperature

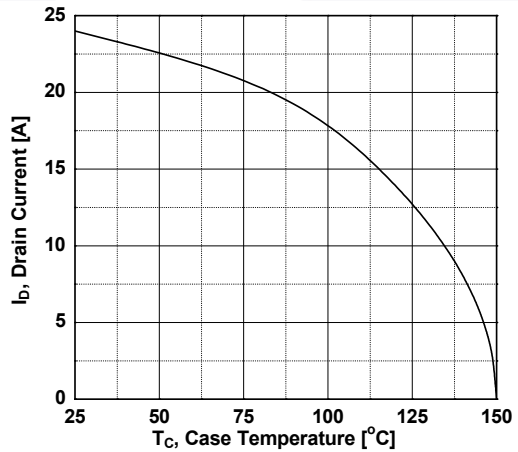
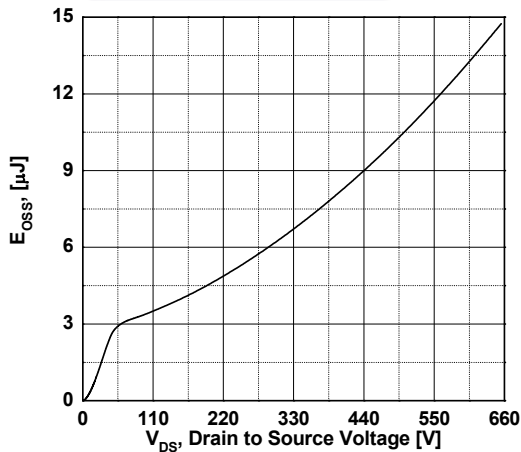
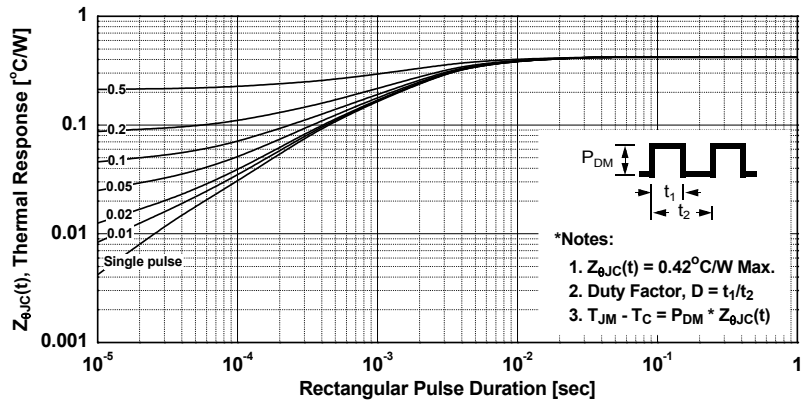


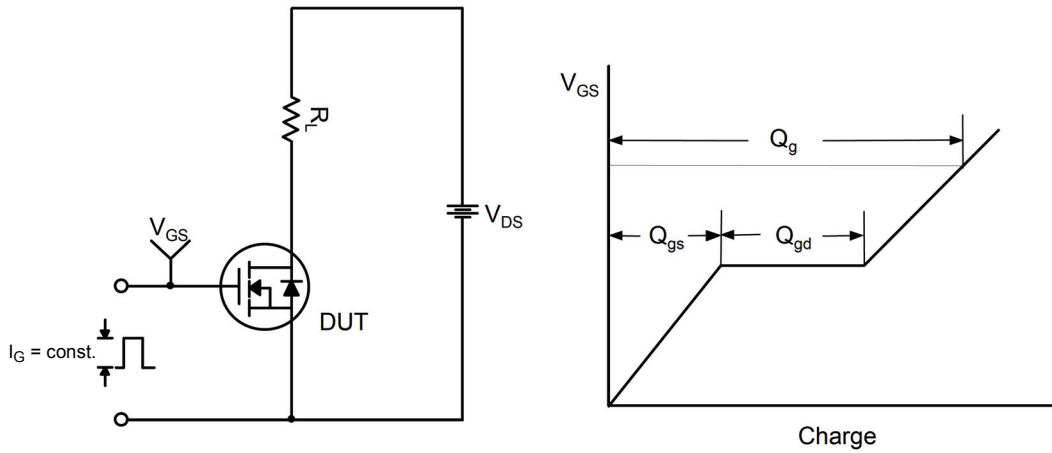
Figure 11. E\_oss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

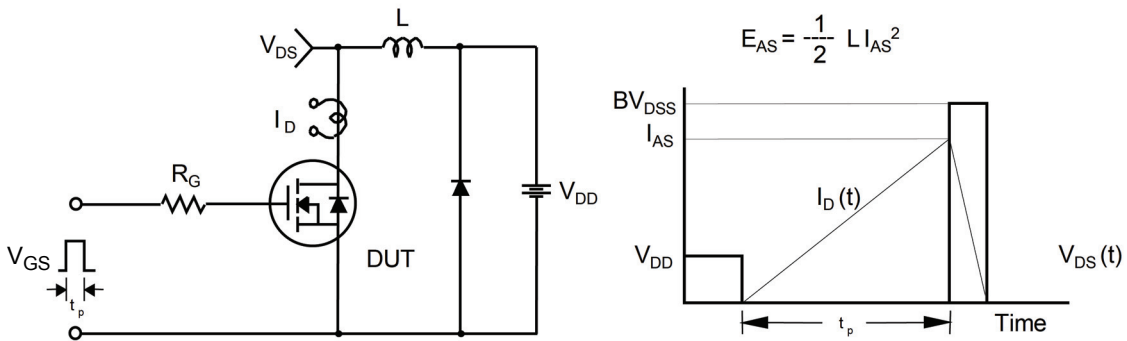




**Figure 13. Gate Charge Test Circuit & Waveform**



**Figure 14. Resistive Switching Test Circuit & Waveforms**



**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**

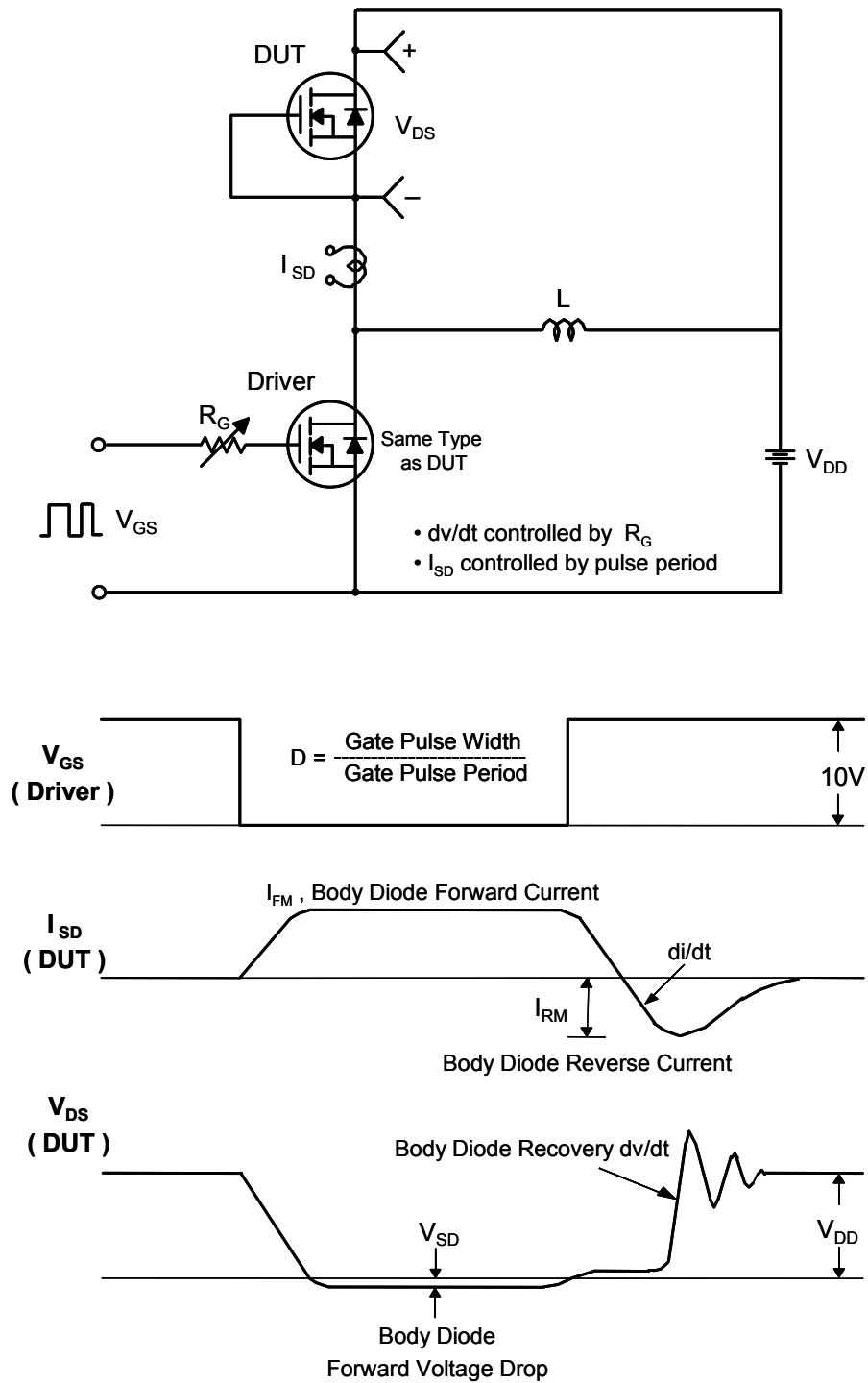
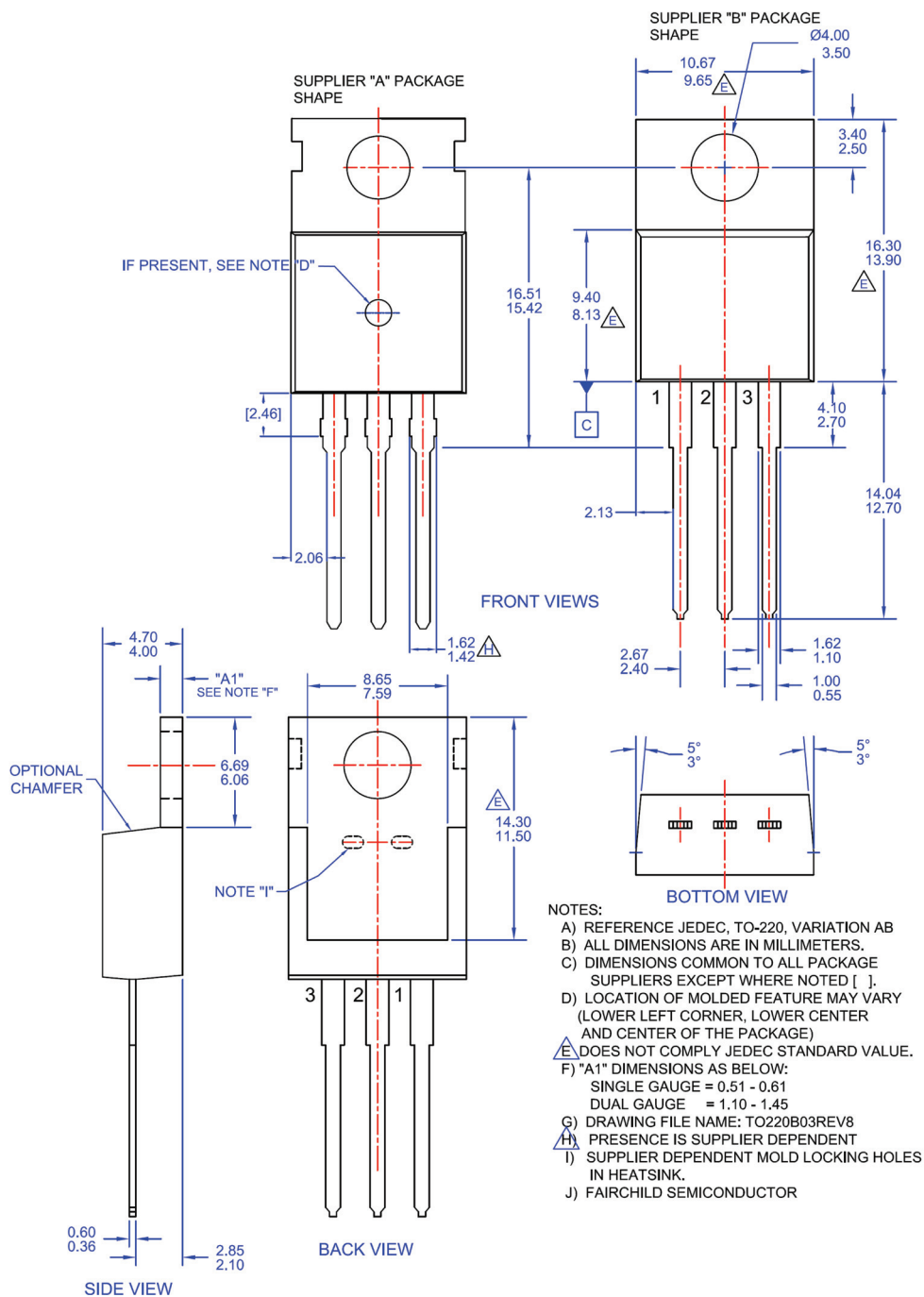


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



## Mechanical Dimensions



**Figure 17. TO-220, Molded, 3-Lead, Jedec Variation AB**

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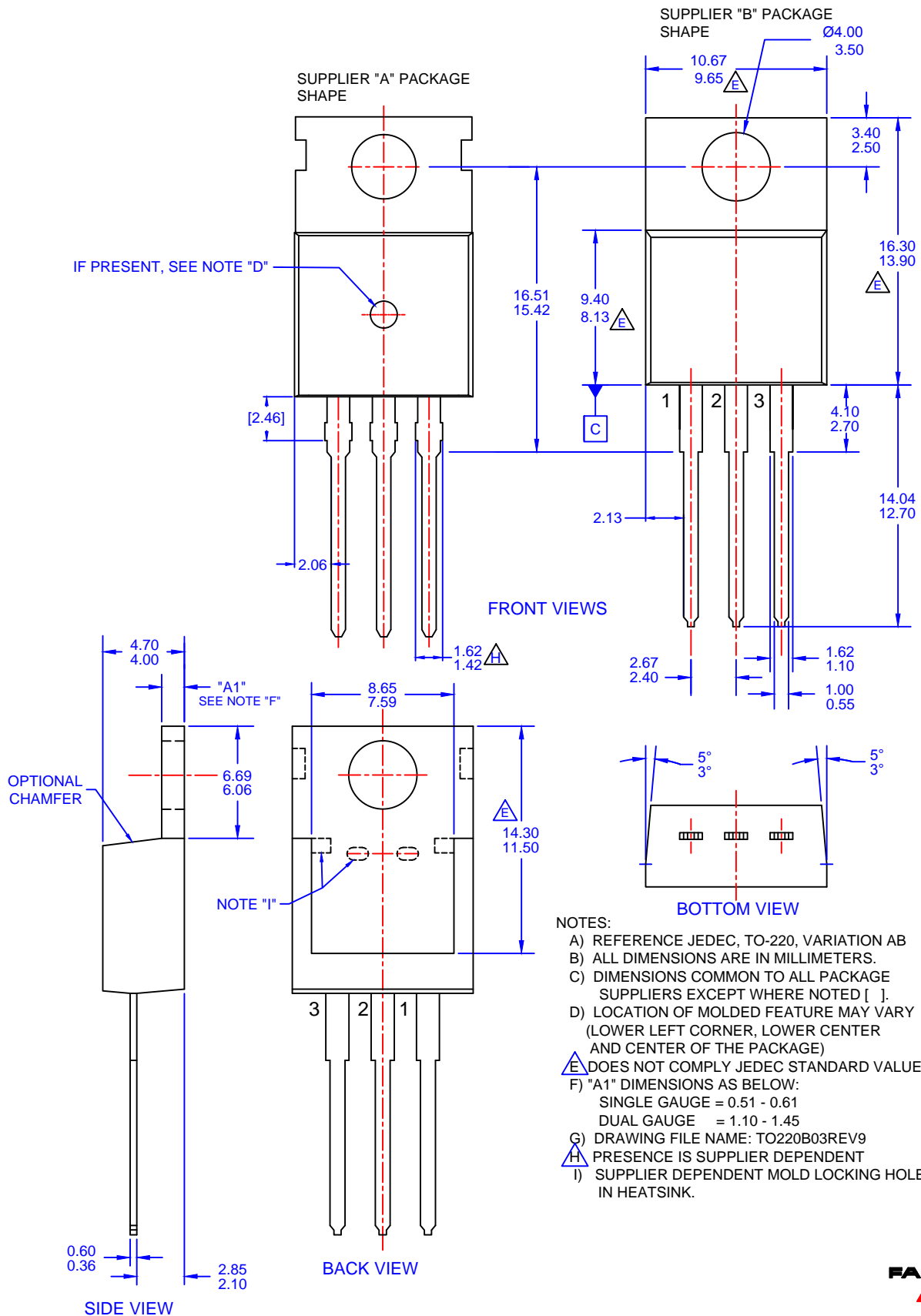
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