PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-PWR/14/8488
Dated 21 May 2014

DPAK Back-End Line relocation from Longgang to Shenzhen (China)

Table 1. Change Implementation Schedule

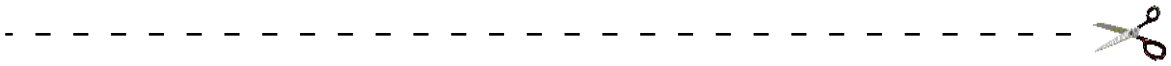
Forecasted implementation date for change	14-May-2014
Forecasted availability date of samples for customer	14-May-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	14-May-2014
Estimated date of changed product first shipment	20-Aug-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly location change, Package assembly process change, Testing location change
Reason for change	Improve service to Customers
Description of the change	Continuing in the already announced plan of consolidating assembly and testing activities, please be informed that we're going to transfer the Assembly/Testing DPAK line for selected Power BIPOLAR Transistors, currently produced in Longgang to Shenzhen (China). DPAK device products, manufactured in Shenzhen (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples.
Change Product Identification	"GK" marked on the package
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-PWR/14/8488**
Please sign and return to STMicroelectronics Sales Office	**Dated 21 May 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Continuing in the already announced plan of consolidating assembly and testing activities, please be informed that we're going to transfer the Assembly/Testing DPAK line for selected Power BIPOLAR Transistors, currently produced in Longgang to Shenzhen (China). DPAK device products, manufactured in Shenzhen (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples.

The involved product series and affected packages are listed in the table below:

Product Family Description	Package	Commercial Product / Series
Power BIPOLAR Transistors	DPAK	STDxxx

Any other Product related to the above series, manufactured in ST Shenzhen, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 20-2014.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Description	Package	Part Number - Test Vehicle
Power BIPOLAR Transistors	DPAK	STD13003T4

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power BIPOLAR Transistors	From Week 34-2014

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipment may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of Power BIPOLAR Transistors produced in ST Shenzhen will be ensured by the Q.A. number and plant code identification “GK” marked on the package.

Sincerely Yours.

Reliability Report

DPAK Back-End Line relocation from Longgang to Shenzhen (China) for selected Power BIPOLAR Transistors.

General Information	
Product Lines:	BV77
Product Families:	Power BIPOLAR
P/Ns:	STD13003T4
Lot1: **Lot2:**	U329037 (TOURS) W338T9Y (AMK)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	DPAK
Silicon Process techn.:	Power BIPOLAR

Locations	
Wafer Diffusion Plants:	*Tours (France)* *Ang Mo Kio (Singapore)*
EWS Plants:	*Tours (France)* *Ang Mo Kio (Singapore)*
Assembly and testing plant:	*ST Shenzhen (China)*
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	May2014	6	A. Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for assembly and testing transfer from the ST plant of Longgang to ST Shenzhen for selected Power BIPOLAR Transistors related to the products housed in DPAK package.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

NPN Power BIPOLAR

4.2 Construction note

D.U.T.:STD13003T4 LINE: BV77 PACKAGE: DPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	Lot1: Tours (France) Lot2: Ang Mo Kio (Singapore)
Technology	Power BIPOLAR NPN
Die finishing back side	Lot1: Ti/Ni/Au Tours (France) Lot2: Ti/Ni/Ag Ang Mo Kio (Singapore)
Die size	1320 x 1390 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Lot1: Tours (France) Lot2: Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Cu
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STD13003T4	BV77	Power BIPOLAR (Tours)
2		BV77	Power BIPOLAR (AMK)

5.2 Reliability test plan summary

D.U.T.: STD13003T4 LINE: BV77 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		Note
						Lot 1 TOURS	Lot 2 AMK	
Die Oriented Tests								
HTRB	N	JESD22 A-108	Tj = 150°C, BIAS=560V	154	168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	
Package Oriented Tests								
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	462	Final	0/231	0/231	
AC	Y	JESD22	Pa=2Atm / Ta=121°C	154	96 H	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	154	100 cy	0/77	0/77	
					200 cy	0/77	0/77	
					500 cy	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS=100V	154	168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented Tests		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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