Notification Number:	20230208003.0	Notification Date:	February 15, 2023
Title:	Datasheet for DS90UB954-Q1 and DS90UB936-Q1		
Customer Contact:	Notification Manager	Dept:	Quality Services

Change Type: Electrical Specification

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DS90UB954-Q1
SNLS570C – AUGUST 2017 – REVISED JANUARY 2023

Changes from Revision B (December 2018) to Revision C (January 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed all instances of legacy terminology to controller and target..... 1
- Revised the PDB pin voltage for normal operation..... 5
- Changed the VDD11 pin descriptions for clarity..... 5
- Added a link to Design Requirements under the RIN pins..... 5
- Updated the V_{IH} and V_{IL} specifications of pins PDB, XIN/REFCLK, and VDD_SEL..... 11
- Removed the mention of CSI-2 non-synchronous clocking mode..... 27
- Changed the bits that need to be modified for Clock Mode 28
- Changed the names of registers CAM_INT_RISE_STS and CAM_INT_FALL_STS to SEN_INT_RISE_STS and SEN_INT_FALL_STS..... 35
- Removed the mention of setting the REF_CLK_MODE bit as it is a reserved bit..... 44
- Fixed typos in the internal FrameSync calculations..... 47
- Rewrote the basic synchronized forwarding code example to set both sensors to use CSI-2 serializers..... 49
- Added in that V_{VDDIO} must match V_{I2C} 55
- Removed the mention of 'PDB' from register 0x0D..... 76
- Changed BCC_Config Register[2:0] binary setting value 0b111 to reserved..... 100
- Changed PORT_CONFIG2[5] default value to 0x1..... 114
- Changed suggested ferrite beads for 4G FPD-Link PoC Network from 1500 kΩ to 1.5 kΩ 140
- Changed PoC network impedance recommendation from 2kΩ to 1kΩ..... 140
- Updated the PoC description..... 140
- Removed the insertion and return loss values from the table on Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks..... 140
- Added a note to explain the differences between the decoupling capacitors..... 144
- Changed the value of the capacitor for pin VDD11_CSI from 1-µF to 10-µF in the diagram where VDD_SEL = HIGH..... 144
- Moved the additional notes in the typical application diagram from the picture to below the diagram..... 144

- Added a note to clarify the power-up sequence between VDD18 and VDDIO..... 149
- Removed T0 and T2 from power-up sequence..... 149
- Added a note to clarify that a hard reset is optional in the power-up sequence..... 149
- Added in T7, the PDB to I2C ready delay, to the power-up sequence..... 149
- Changed the pull-up resistor for PDB from 33-kΩ to 10-kΩ..... 150

TEXAS INSTRUMENTS

DS90UB936-Q1
SNLS571C – MARCH 2018 – REVISED JANUARY 2023

Changes from Revision B (June 2018) to Revision C (January 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed all instances of legacy terminology to controller and target..... 1
- Updated the list of compatible devices to include the DS90UB953-Q1..... 1
- Revised the PDB pin voltage for normal operation..... 4
- Changed the VDD11 pin descriptions for clarity..... 4
- Added a link to Design Requirements under the RIN pins..... 4
- Updated the V_{IH} and V_{IL} specifications of pins PDB, XIN/REFCLK, and VDD_SEL..... 10
- Removed the mention of CSI-2 non-synchronous clocking mode..... 26
- Changed the bits that need to be modified for Clock Mode 27
- Removed the mention of setting the REF_CLK_MODE bit as it is a reserved bit..... 42
- Fixed typos in the internal FrameSync calculations..... 46
- Rewrote the basic synchronized forwarding code example to set both sensors to use CSI-2 serializers..... 48
- Added in that V_{VDDIO} must match V_{I2C} 54
- Removed the mention of 'PDB' from register 0x0D..... 75
- Changed BCC_Config Register[2:0] binary setting value 0b111 to reserved..... 99
- Changed PORT_CONFIG2[5] default value to 0x1..... 113
- Changed suggested ferrite beads for 4G FPD-Link PoC Network from 1500 kΩ to 1.5 kΩ 139
- Changed PoC network impedance recommendation from 2kΩ to 1kΩ..... 139
- Updated the PoC description..... 139
- Removed the insertion and return loss values from the table on Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks..... 139
- Added a note to explain the differences between the decoupling capacitors..... 143
- Changed the value of the capacitor for pin VDD11_CSI from 1-µF to 10-µF in the diagram where VDD_SEL = HIGH..... 143
- Moved the additional notes in the typical application diagram from the picture to below the diagram..... 143
- Added a note to clarify the power-up sequence between VDD18 and VDDIO..... 148
- Removed T0 and T2 from power-up sequence..... 148
- Added a note to clarify that a hard reset is optional in the power-up sequence..... 148
- Added in T7, the PDB to I2C ready delay, to the power-up sequence..... 148
- Changed the pull-up resistor for PDB from 33-kΩ to 10-kΩ..... 149

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UB954-Q1	SNLS570B	SNLS570C
DS90UB936-Q1	SNLS571B	SNLS571C

The document is not available on the TI website. Please access MySecure for a copy of the full datasheet.

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:

None.

Product Affected:

DS90UB954TRGZRQ1	DS90UB954TRGZTQ1	DS90UB936TRGZRQ1	DS90UB936TRGZTQ1

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